The Belle II pixel vertex detector

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On behalf of the DEPFET Collaboration

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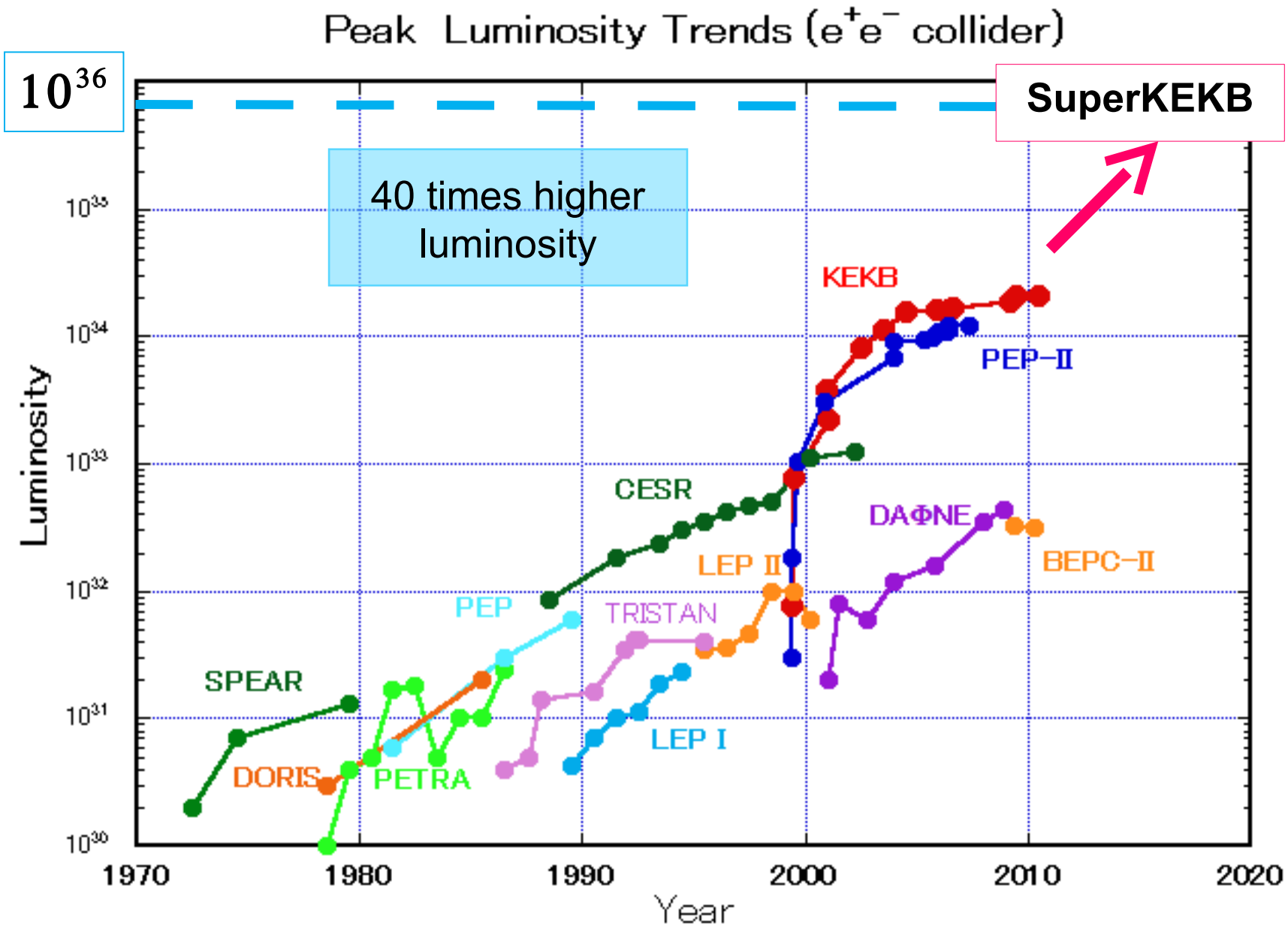
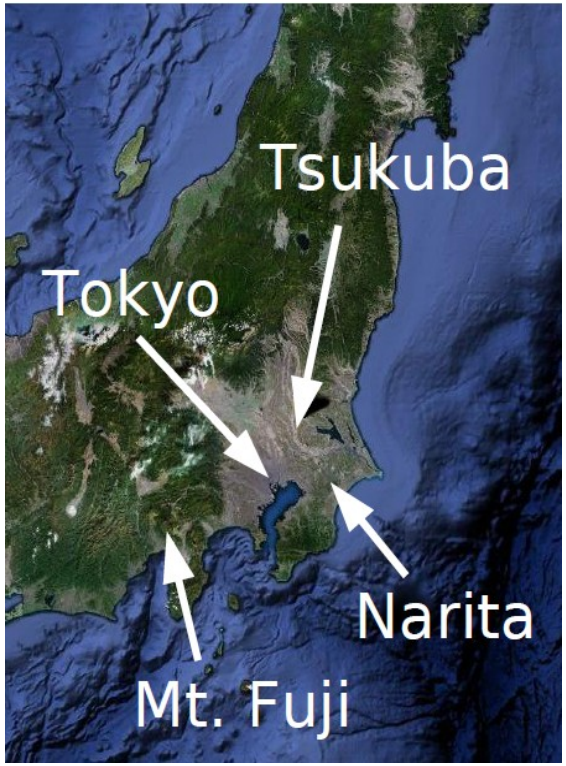
Outline

- *Upgrade KEKB t o Super KEKB*
  - Belle II detector design
- *DEPFET principle*
  - Readout sequence
- *DEPFET ladder design for Belle II*
- *Readout ASICS*
  - DCD
  - Switcher-B
  - DHP
- *Prototyping for Belle II*
- *Test results*
- *Conclusion*

Next generation B-factories



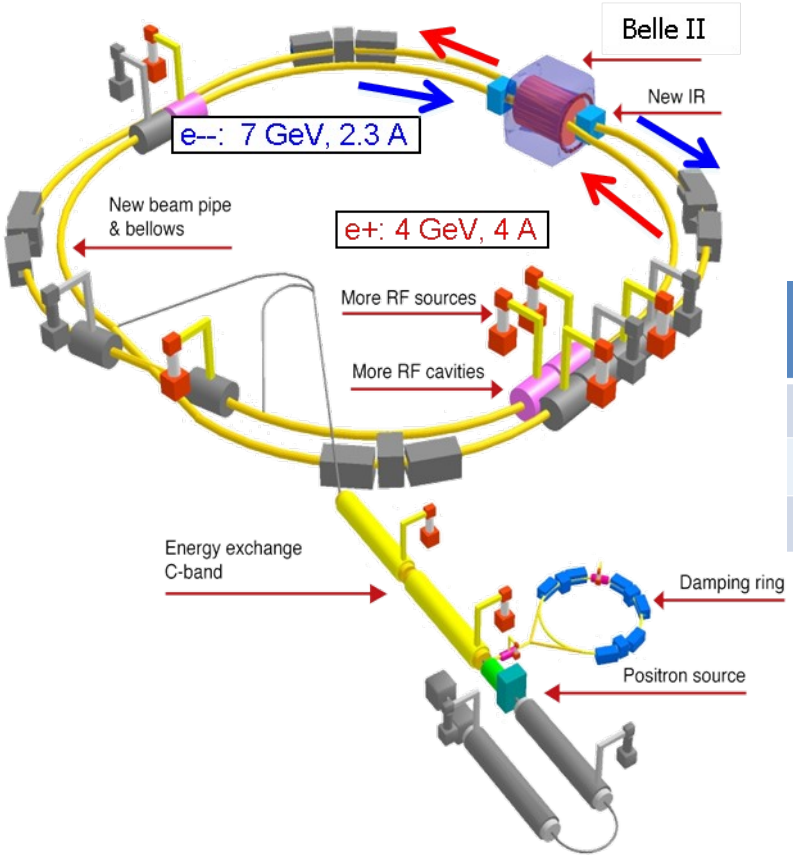
B-factory in Tsukuba, Japan

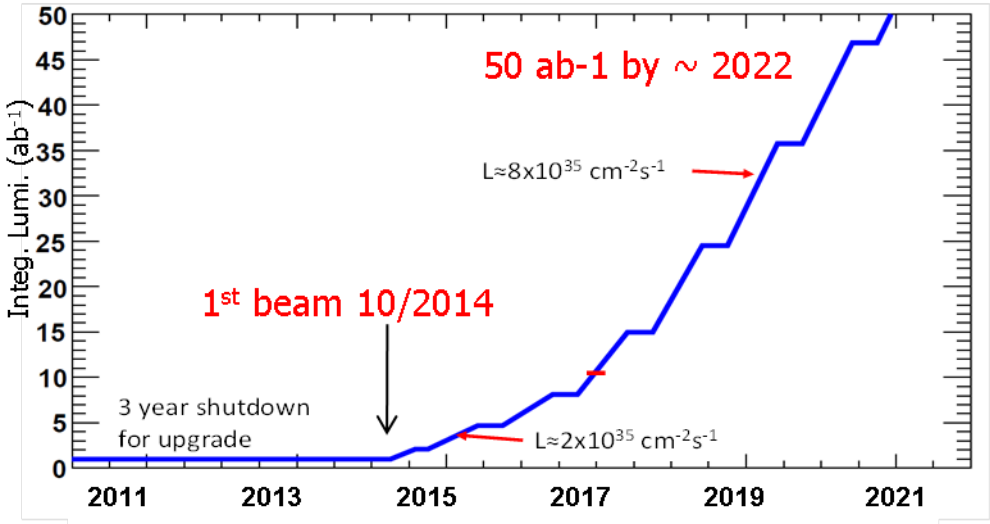


World record luminosity for e+e- colliders: 2.1×10^{34} $cm^{-2}s^{-1}$

KEKB to SuperKEKB

- e^-/e^+, 7 GeV & 4 GeV
- E_cm at Y(4s) resonance, (10.58 GeV)
- goal L = $8x10^{35}$ $cm^{-2}s^{-1}$





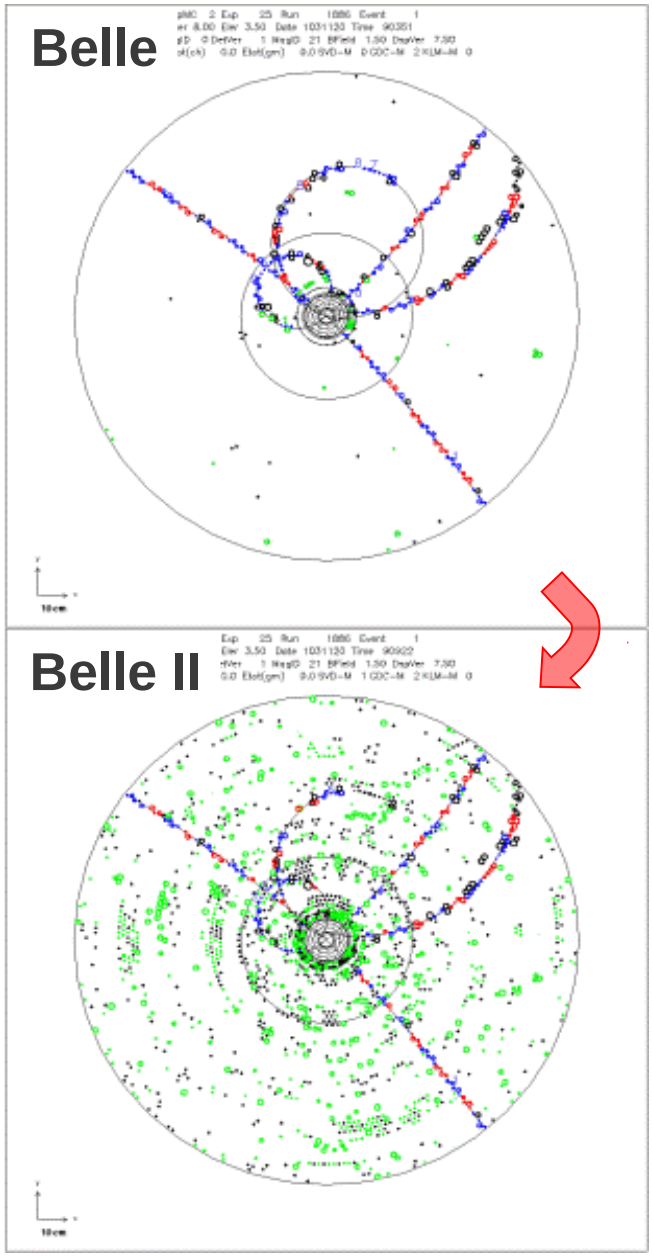
Machine parameter	HER (KEKB)	LER (KEKB)	HER (SuperKEKB)	LER (SuperKEKB)
Vertical beam size	0.94μm	0.94μm	59nm	59nm
Beam current(mA)	1188	1637	2600	3600
luminosity($cm^{-2}s^{-1}$)	$2.1x10^{34}$		$8x10^{35}$	

Smaller beam size & more current:
→ 40x higher luminosity

Requirements for the Belle II detector

- *Higher background (x10-20 compared to Belle)*
  - Radiation damage and occupancy
  - Fake hits
- *Higher event rate*
  - Higher trigger rate (0.5 kHz → 20-30 kHz)
- *The physical goals require a vertex detector with unprecedented performance (~10μm) :*
  - low material budget (<0.2 X_0 per layer)
  - high granularity pixel detector

New pixel vertex detector (PXD) based on DEPFET technology is being developed, using sensor thinned down to 75 μm.



Belle II design

KL and muon detector:
Resistive Plate Counter (barrel)
Scintillator + WLSF + MPPC (end-caps)

EM Calorimeter:
CsI(Tl), waveform sampling (barrel)
Pure CsI + waveform sampling (end-caps)

Particle Identification
Time-of-Propagation counter (barrel)
Prox. focusing Aerogel RICH (fwd)

electron (7GeV)

Beryllium beam pipe
2cm diameter

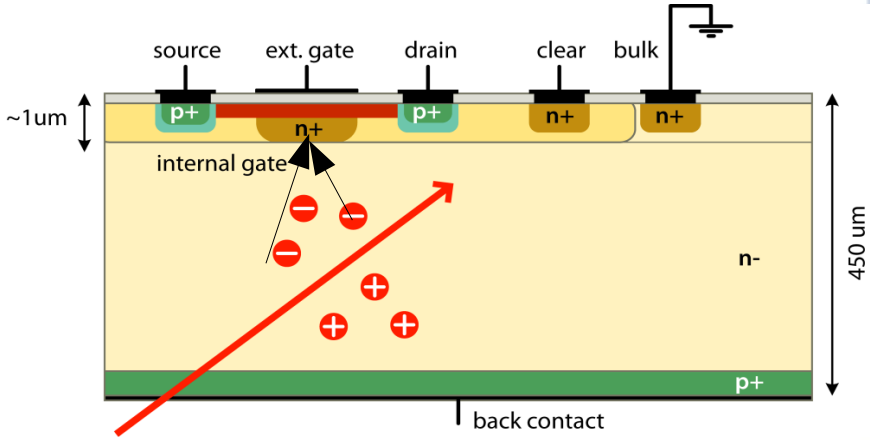
Vertex Detector
2 layers DEPFET + 4 layers DSSD

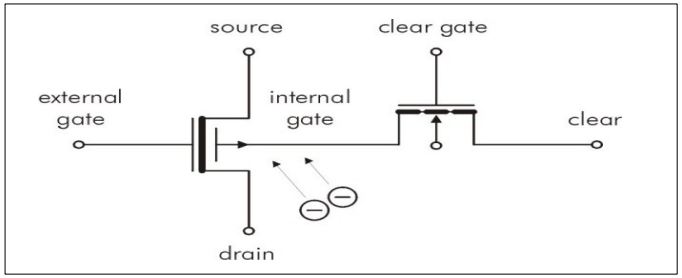
positron (4GeV)

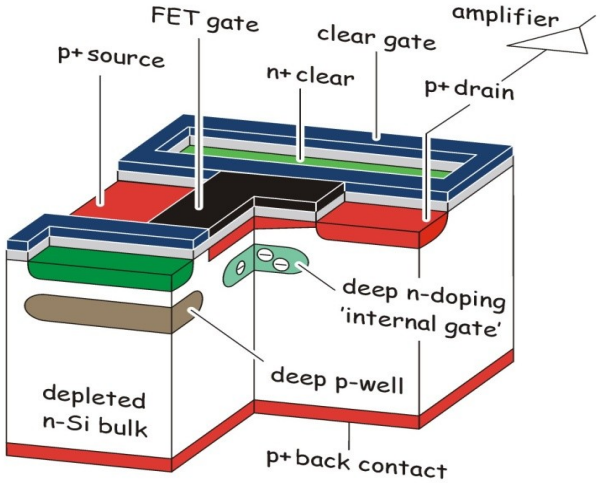
Central Drift Chamber
He(50%):C_2H_6(50%), Small cells, long lever arm, fast electronics

DEPFET principle

- *The DEPFET is an active pixel sensor which integrates a MOSFET into the high resistivity silicon substrate*
  - in-pixel amplification
- *Provides fast charge collection in fully depleted bulk*
  - fast signal rise time (~ns), small cluster size
- *Electrons are collected in "internal gate" - potential minimum for electrons - and modulate transistor current*
  - charge-to-current conversion
- *Transistor can be switched off by external GATE – charge collection still active !*
  - potentially low power device
- *Low readout capacitance – reduces the noise*
- *no stitching, 100% fill factor*
- *no charge transfer needed*
  - faster read out
  - better radiation tolerance
- *Charge from internal gate is removed by the CLEAR contact*

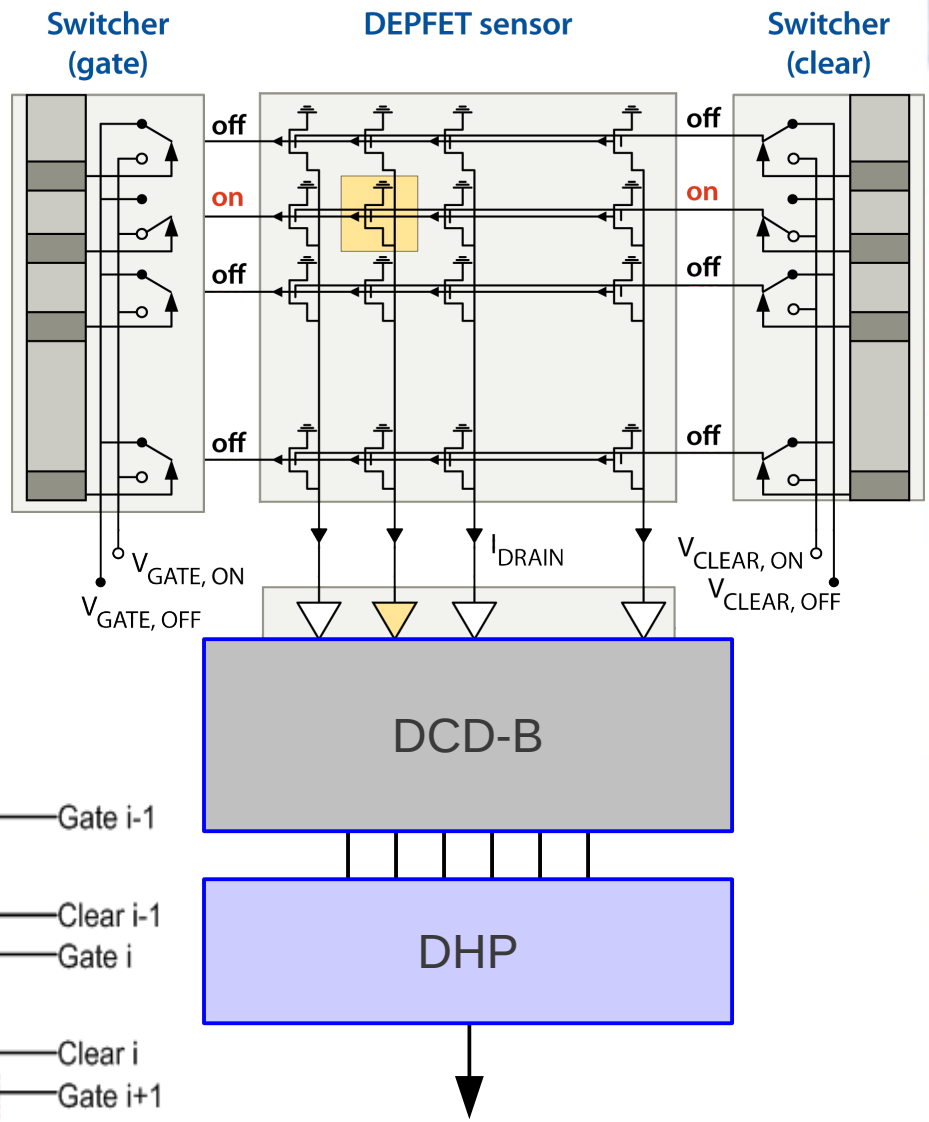


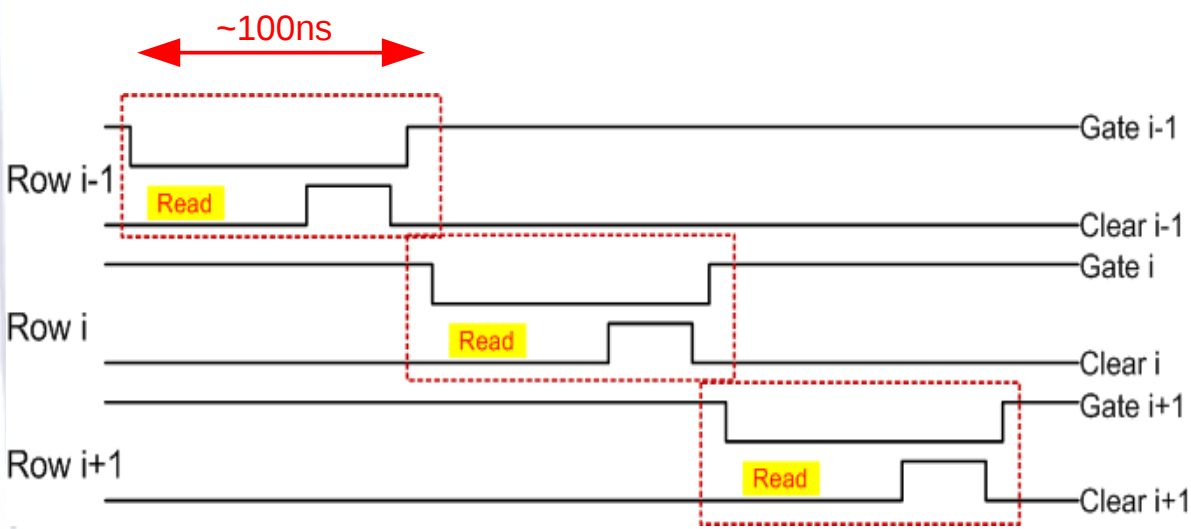




DEPFET readout sequence

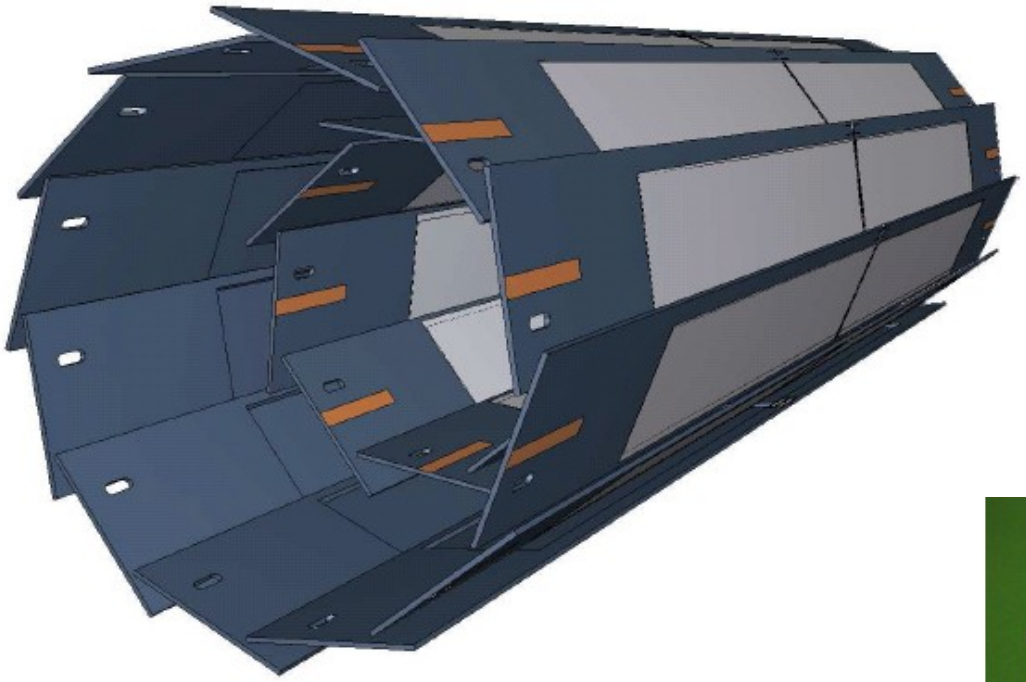
- *Row wise readout (Rolling Shutter)*
- *The SWITCHER chip generates the steering signals for the rows - GATE and CLEAR.*
- *Readout chip processes all columns in parallel*
- *DEPFET readout sequence (single sampling) :*
  1. select row with external gate
  2. readout transistor current
  3. clear charge from internal gate
  4. select next row





PXD geometry for Belle II

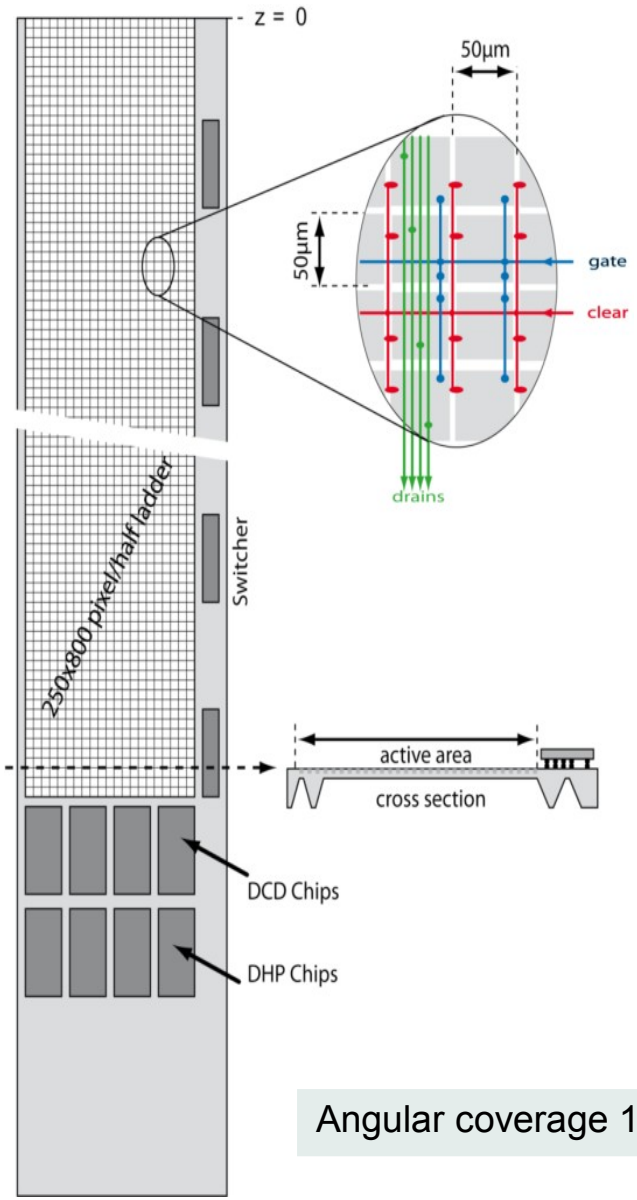
PXD layout in GEANT4



PXD ladder

Mechanical mockup

Belle II ladder



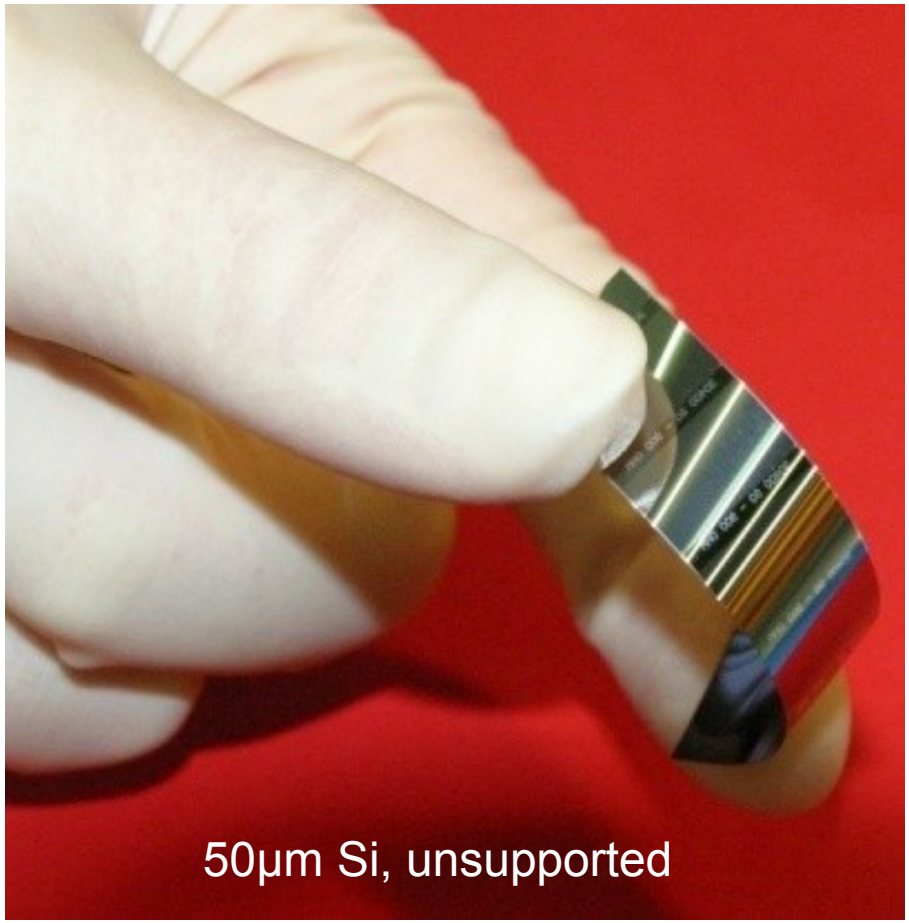
- All silicon module, sensitive area thinned
- Length: 90mm (inner), 123mm (outer)
- 23mm insensitive silicon on both sides
- Insensitive part is used as substrate for ASICs
- ASICs bump bonded to silicon substrate

	Inner layer	Outer layer
# ladders	8	12
Radius	1.4 cm	2.2 cm
Pixel size	50x50 μm^2	50x75 μm^2
# pixels	1600(z)x250(R-ϕ)	1600(z)x250(R-ϕ)
Thickness	75 µm	75 µm
Frame/row rate	50 kHz/10 MHz	50 kHz/10 MHZ

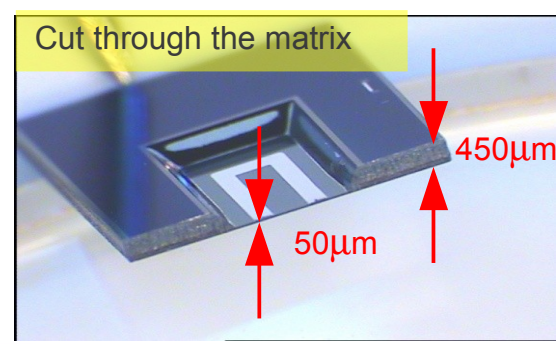
Angular coverage 17°<θ < 155°

Belle II PXD in total ~8 Mpixels

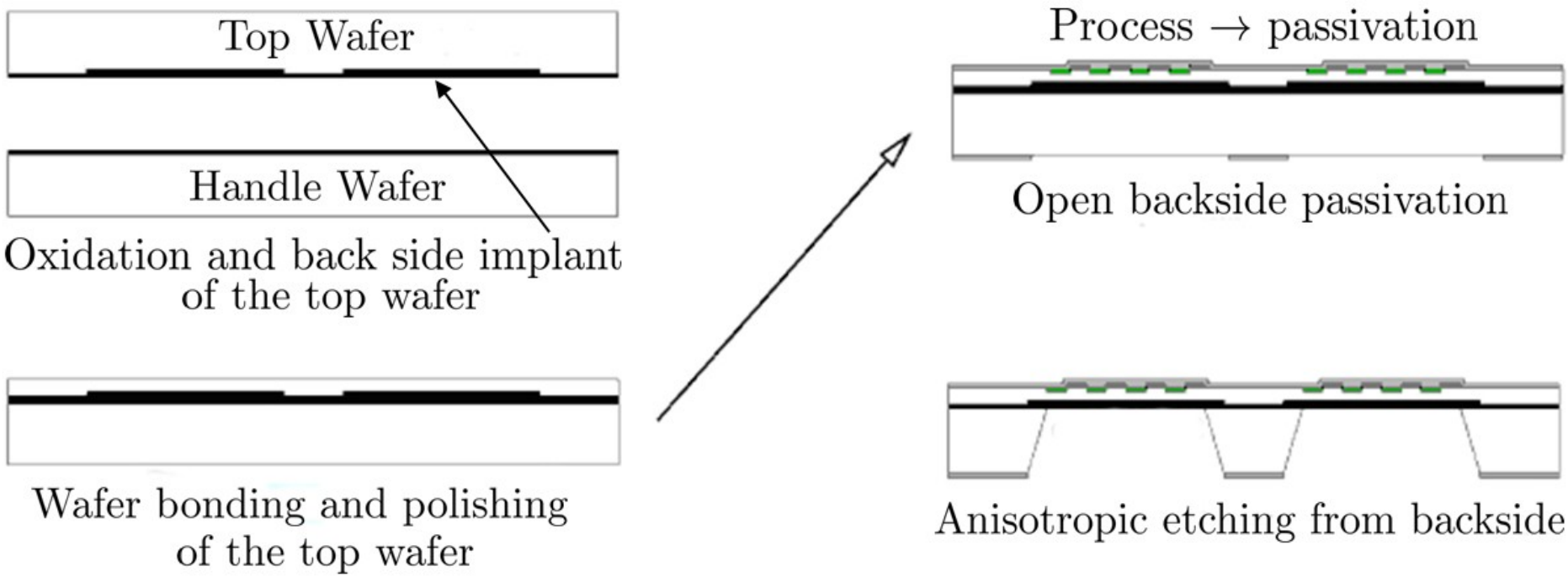
Self-supporting All-Silicon Module



- Half-ladders (modules) are laser-cut
- Modules are supported by a monolithic silicon frame
- Two modules are assembled to one ladder
- overall length is 136 mm (inner) and 169 mm (outer)



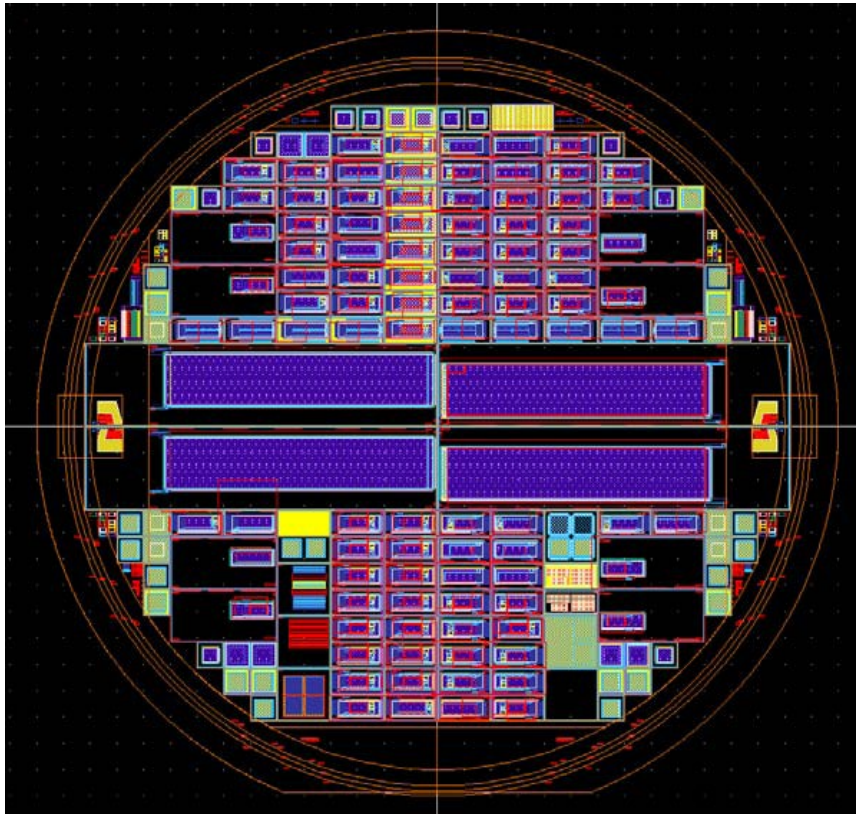
Thin DEPFET – the SOI approach

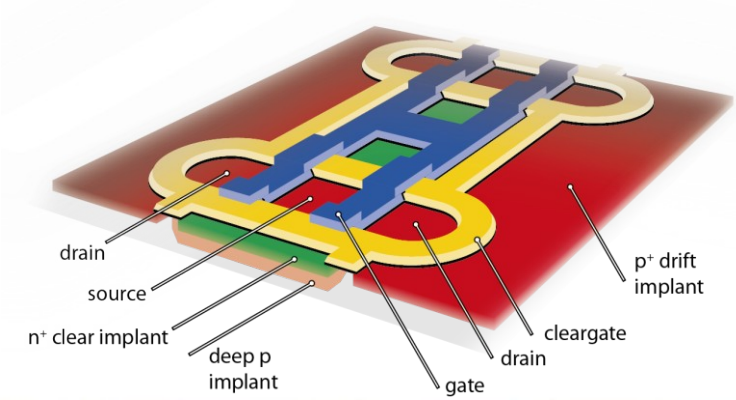


- *The DEPFET thickness becomes a free parameter, adjustable to the needs of the experiment!*
- *Key Process Modules:*
  - Wafer Bonding and thinning of top layer (external)
  - Sensor fabrication on SOI
  - Etching of the Handle Wafer
  - Litho on extreme topographies

PXD6 prototyping

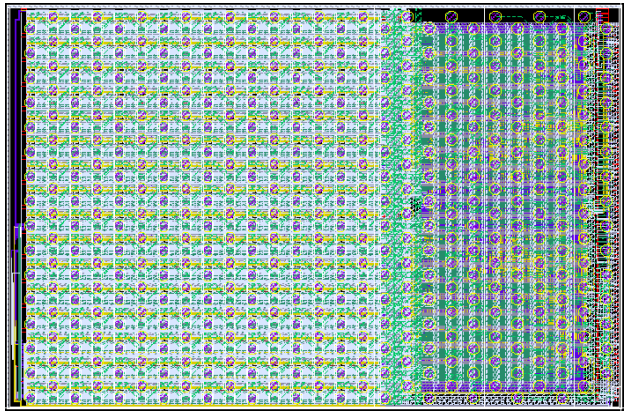
- *8 SOI wafers (50 µm top layer, 400 µm handle wafer)*
  - + 2 reference wafers on std. 450µm material
- *Pixel design and material adapted to 50 µm top layer thickness (Vfd≈15V), extensive device simulations to find the right geometry for the optimal electric field shape*
- *About 100 test matrices in different variations*
  - pixel sizes from 20 µm to 200 µm
  - shorter gate length,
  - improved clear structures,
  - various field shapes..
- *Technology variations on the wafer level (new dry etch techniques..)*
- *4 half-ladders for Belle II with the most promising design options*



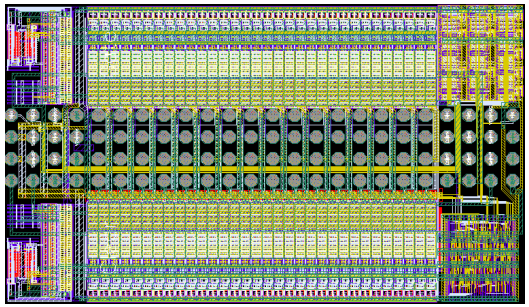


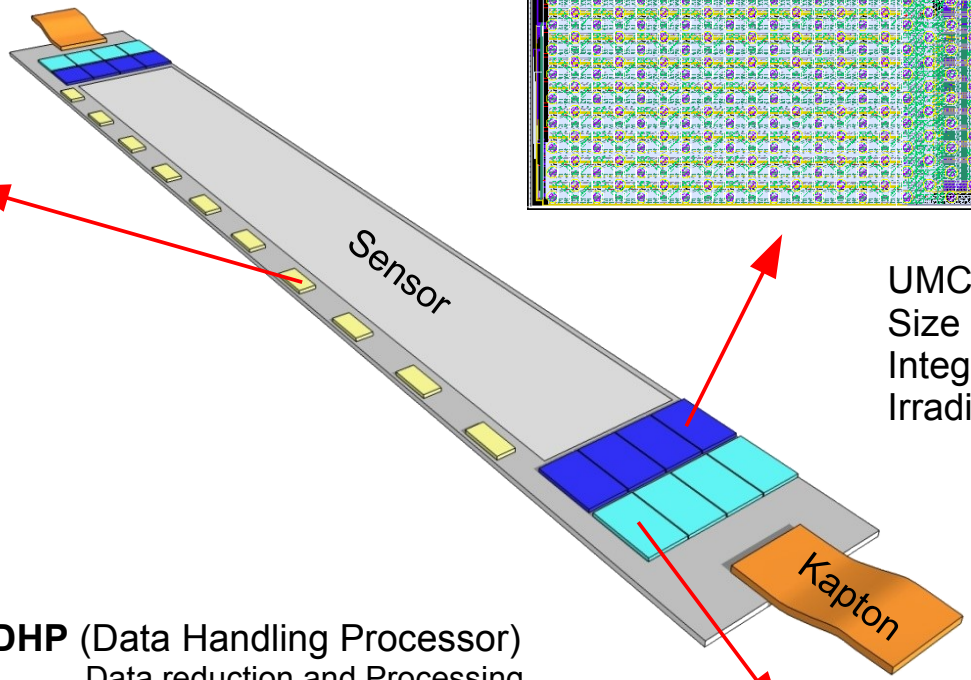
Readout ASICs

DCDB (Drain Current Digitizer for BelleII)
Analog frontend and ADC



SwitcherB
Row control



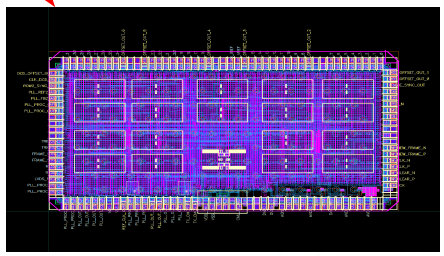


AMS high voltage 0.35µm
Size 3.6 x 2.1 mm^2
Gate and Clear signal
Fast HV up to 30V
Rad. Hard proven (36Mrad)

UMC 180nm
Size 3.3 x 5.0 mm^2
Integrated ADC
Irradiation up to 7Mrad

DHP (Data Handling Processor)
Data reduction and Processing

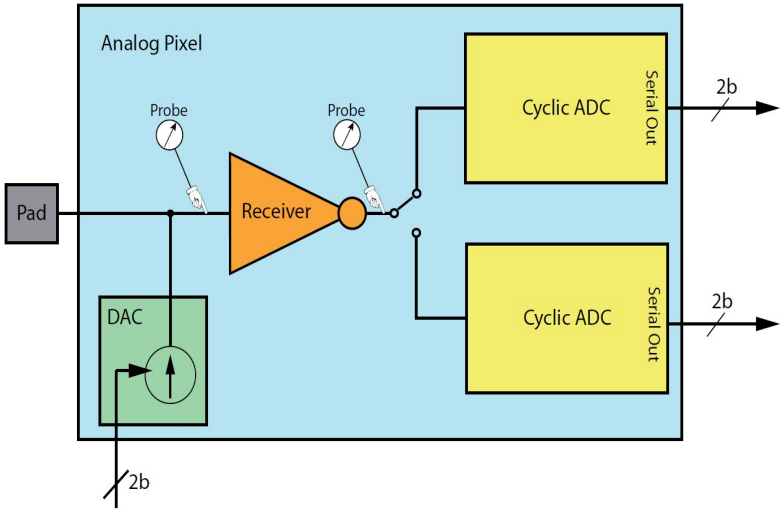
IBM CMOS 90nm → TSMC (65nm)
Stores raw data and pedestals
Common mode and pedestal correction
Data reduction (zero suppression)
Timing signal generation

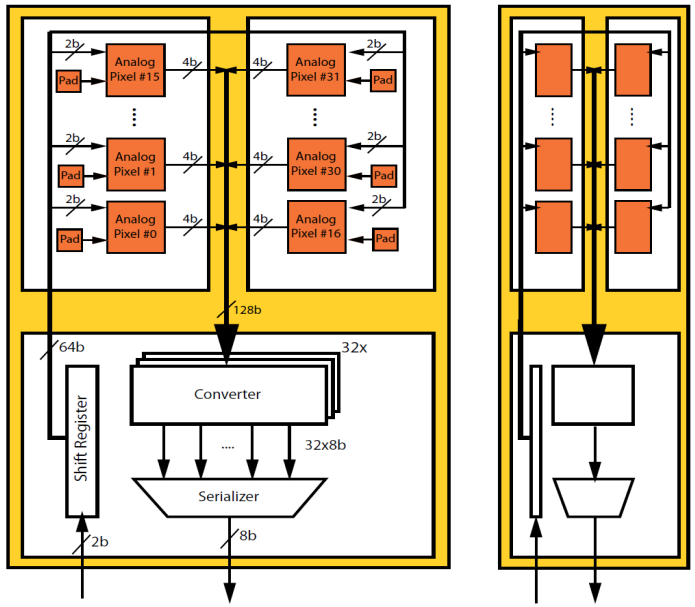


Switcher, DCDB: Heidelberg U.
DHP: Bonn U., Barcelona U.

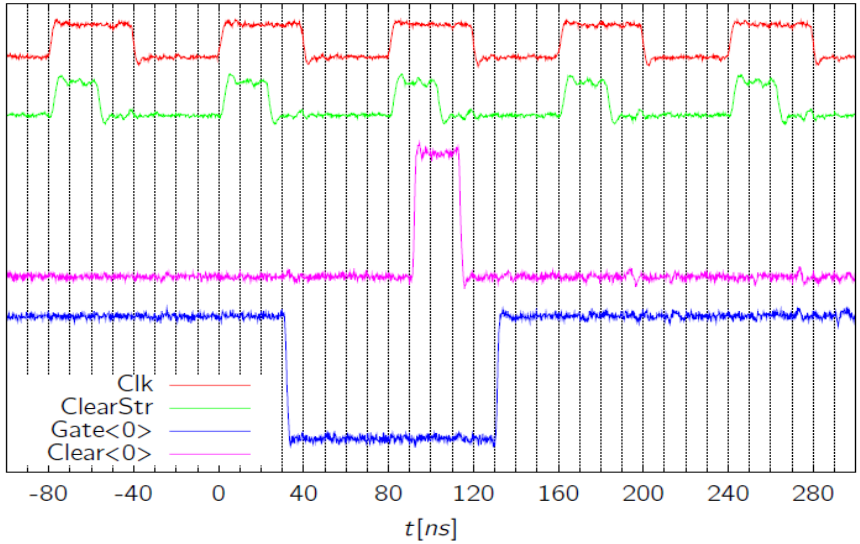
DCDB

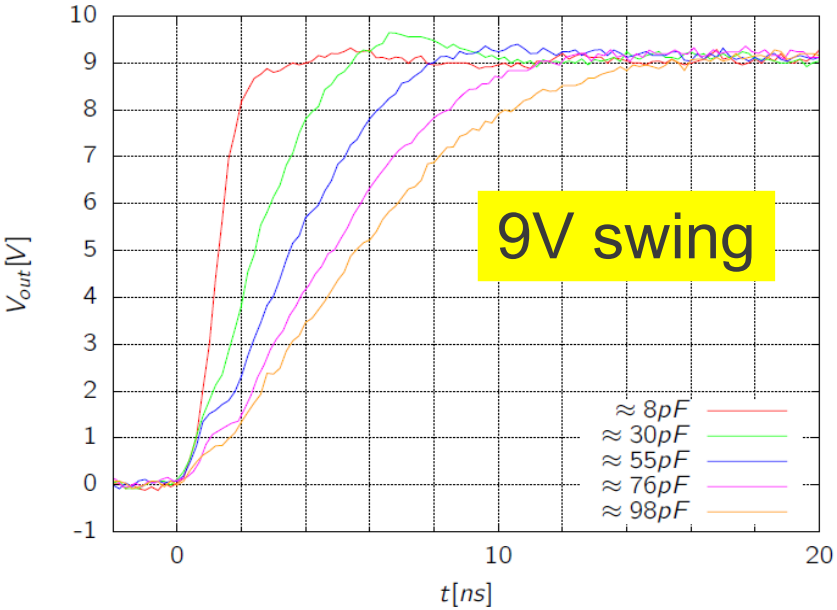
- *Chip size: 3240 µm x 4969 µm*
- *Total: 416 bumps*
  - 256 analog inputs
  - 64 digital outputs (8 times 8-bit at 350 MHz) for ADC codes
- *8-bit ADC precision*
- *Sampling period: ~92 ns (350 MHz)*
- *Every analog channel contains:*
  - Current receiver, based on a trans-impedance amplifier with output resistor, with variable gain and shaping time
  - 8-bit current-mode ADC (two per channel)
- *Global circuits:*
  - Synthesized digital readout block for ADC-data processing, multiplexing and sorting
  - JTAG
- *Single-ended digital outputs for 400 Mbit/s*
- *Supply current:*
  - Analog: 300-500 mA
  - Digital: 300 mA



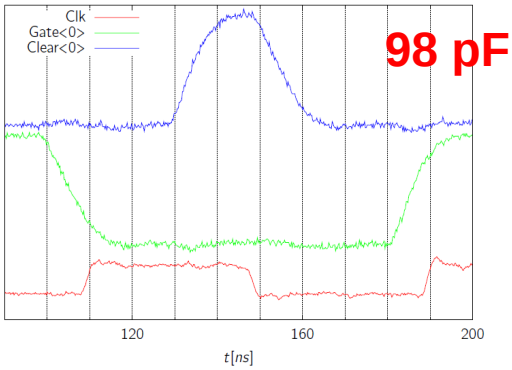


Switcher B

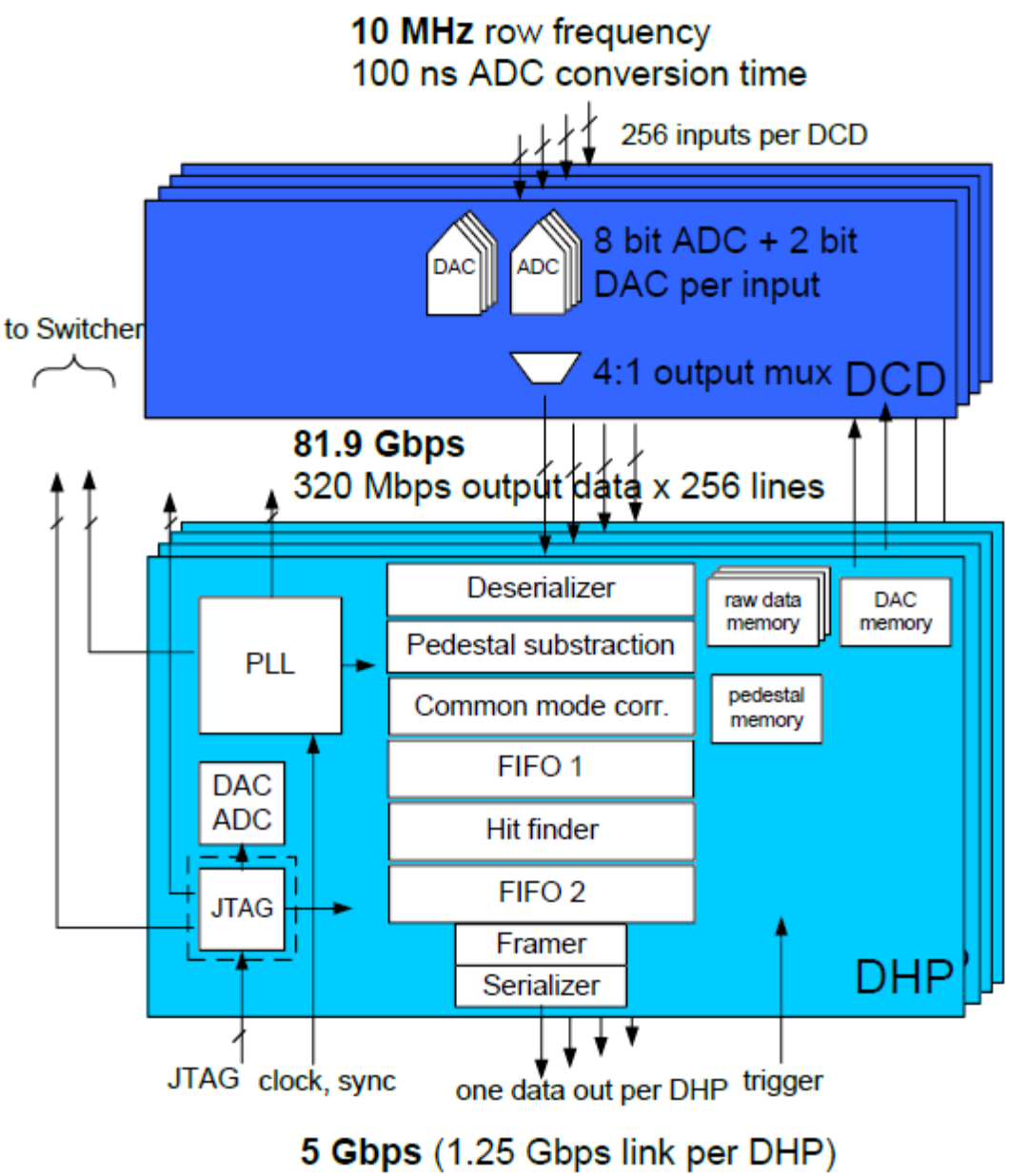




- *Designed size: 2100µm x 3600 µm*
- *32 rows*
  - each row with CLEAR and GATE output
  - shift register to enable rows (LVDS)
  - gate and clear strobe signals (LVDS)
  - sleep and boost states for power saving
- *AMS HV technology (max 50V)*
- *Radiation hard design*
  - Chip works after 24.5Mrad irradiation
- *floating digital 3.3V supply*
- *JTAG slow control and boundary scan*
  - 1.8V capable I/Os
- *Switcher-B working at 80ns row time*

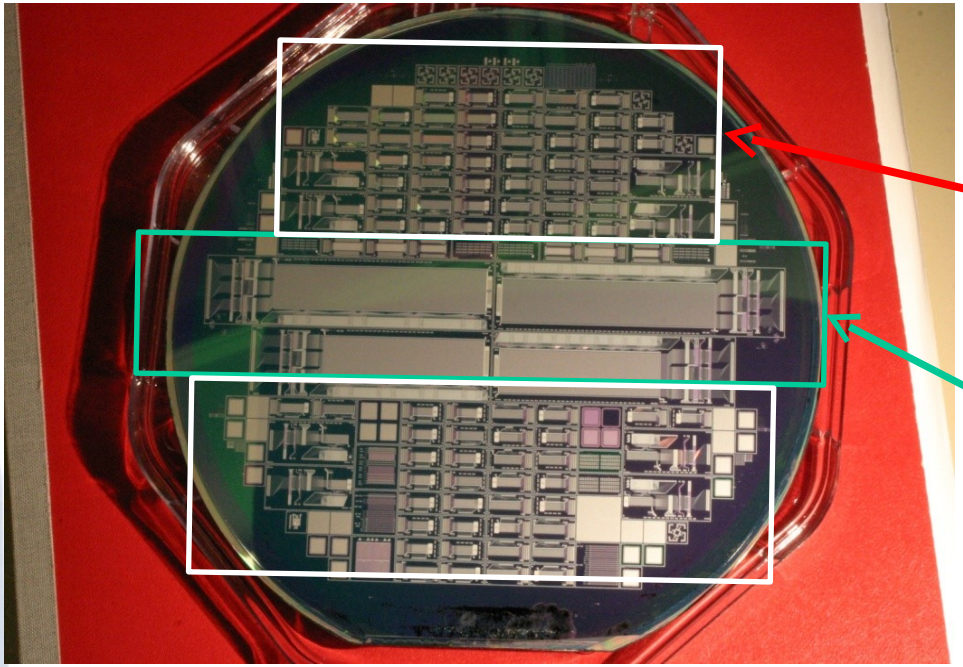


DHP Function Blocks



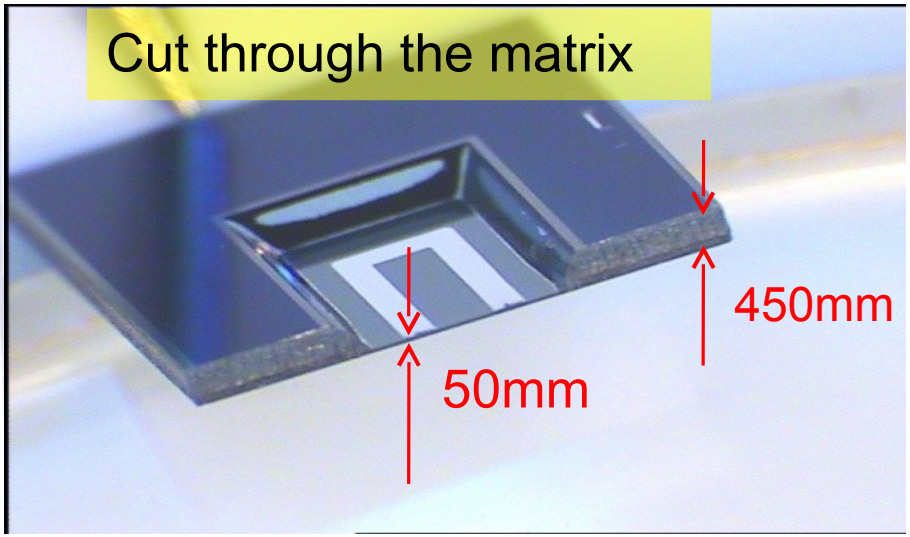
- *64 inputs at 400MHz input rate*
- *50kHz input frame rate*
- *30kHz trigger rate*
- *Receive and write raw data to memories (continuously)*
- *Trigger → read memory and process data*
- *Pedestal subtraction*
  - Static pedestals (update via JTAG)
- *Two pass common mode correction*
  - First pass: all pixels → find hits (biased)
  - Second pass: average w/o hits → zero-supp.
- *Hit finder & de-randomizing FIFOs*
  - 64 inputs (FIFO 1)
  - 1 output (FIFO 2)
- *Framer*
  - Data formatting
  - AURORA protocol
- *Serializer*
  - 20:1 mux
  - CML driver with pre-emphasis @1.5Gbps

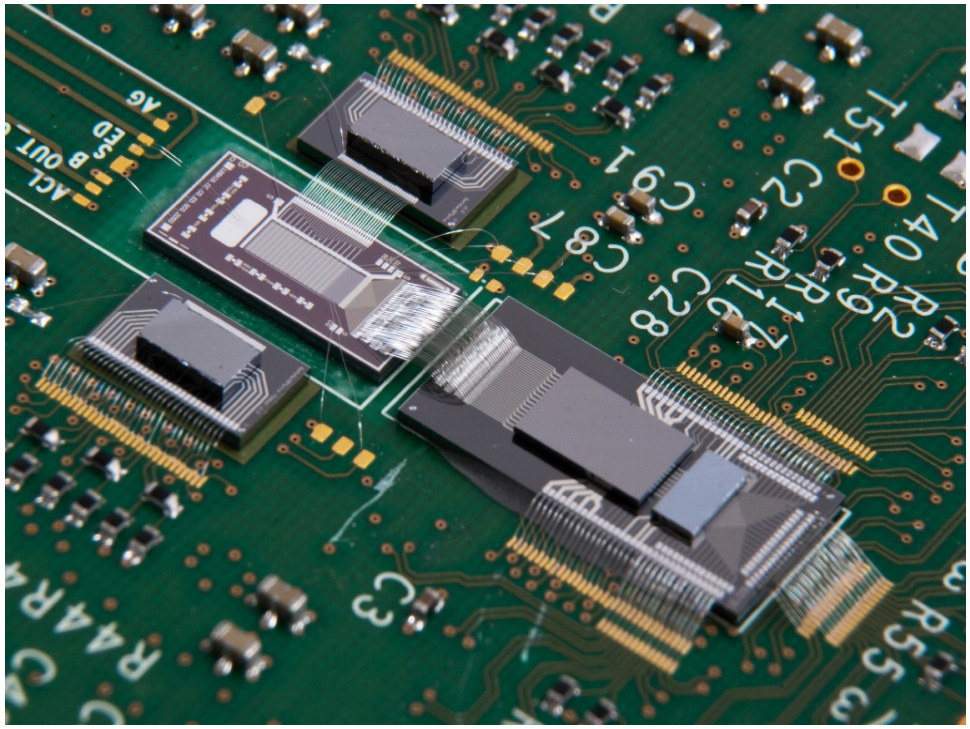
First measurements of thin matrix



Small matrices 32x64 pixels,
different technology variations,
ASIC connection via wire bonding

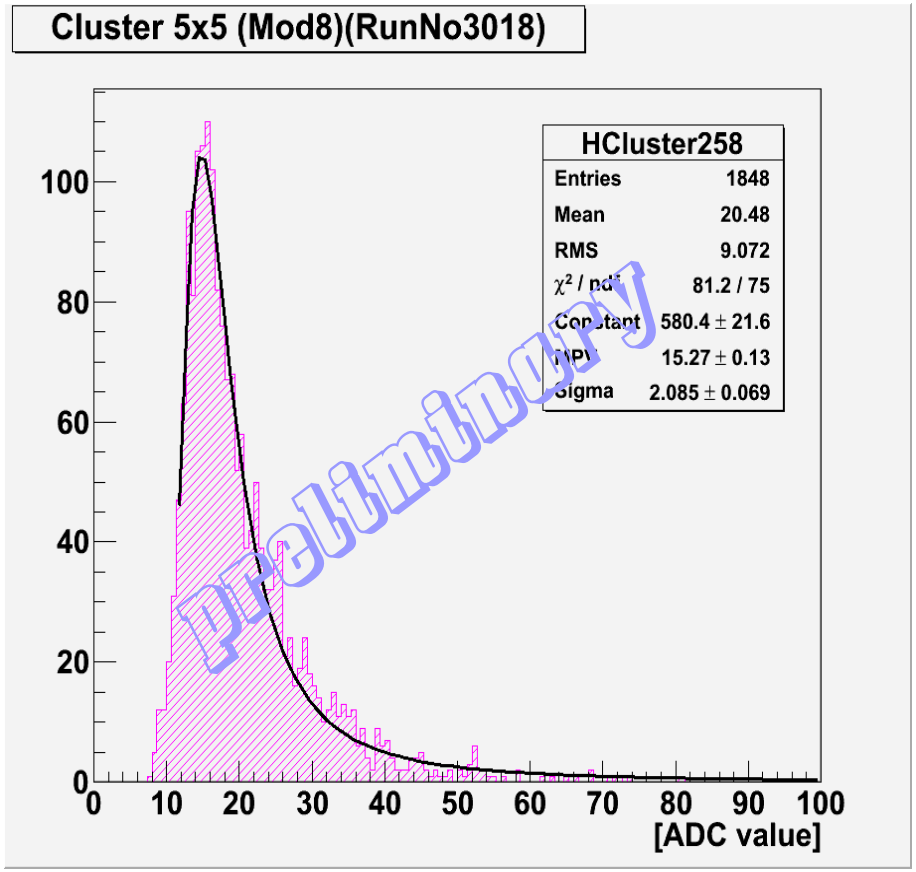
Half ladders 768x120-160 pixels
(~ Belle II geometry)

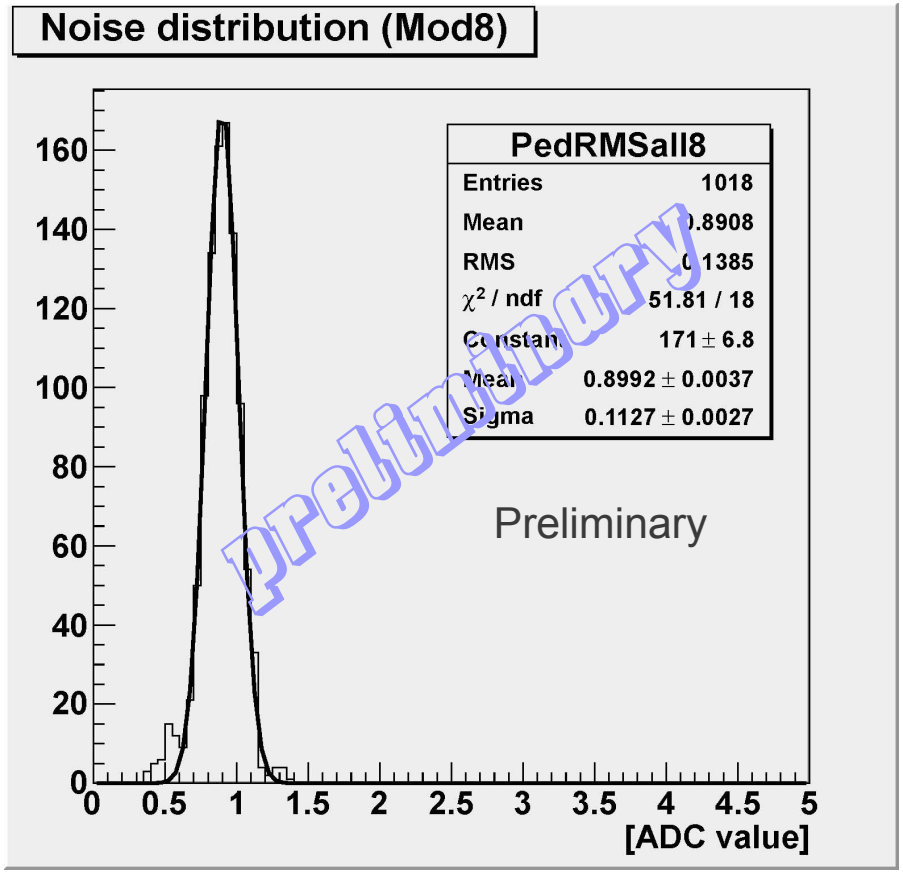




Thin DEPFET & DCDB @ 320 MHz

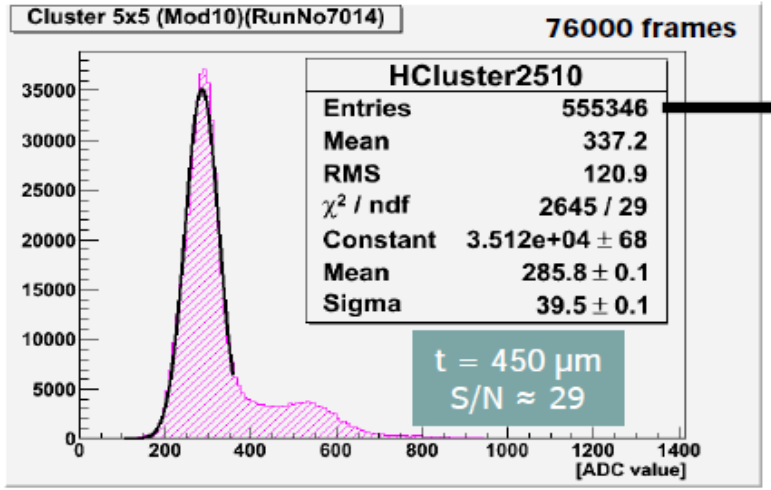
- ^{90}Sr source
- DCD-B readout @ 320 MHz = 100 ns row readout
- S/N = 17 – without optimization of DEPFET voltages



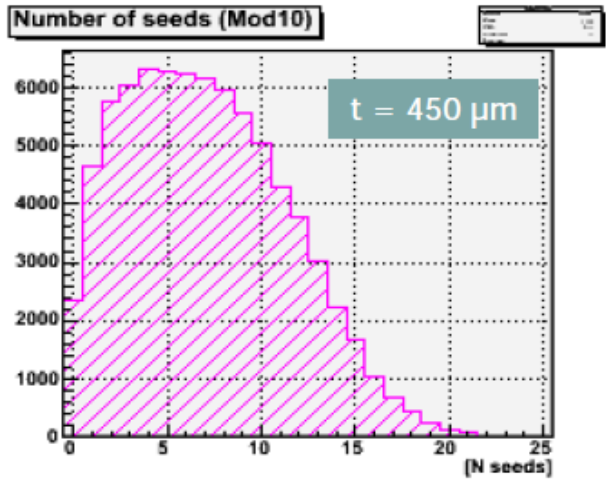


Signal measurements ^{109}Cd

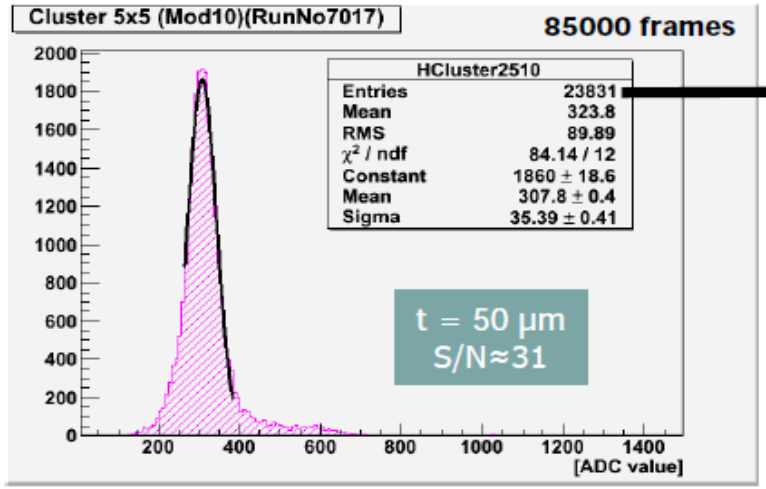
- *2 DUTs: 32x64 pixels Belle II PXD design, L=6 µm, pixel size 50x75 µm2, same design on front (CURO readout chip)*
  - I : 450 µm standard
  - II: 50 µm SOI



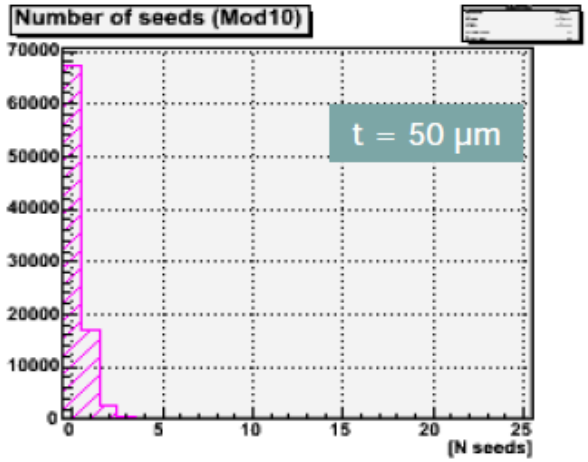
Thick: 7 clusters/frame



- ▷ 22keV photons
- ▷ ~6000 e/h pairs
- ▷ does not depend on t!
- ▷ but count rate is reduced
- ▷ photons just pass w/o conversion

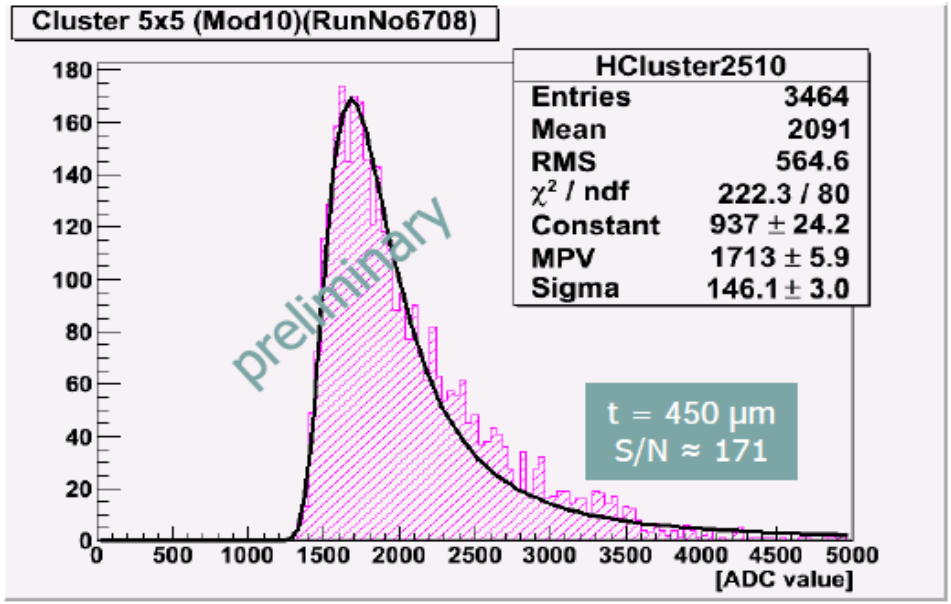


Thin: 0.28 clusters/frame



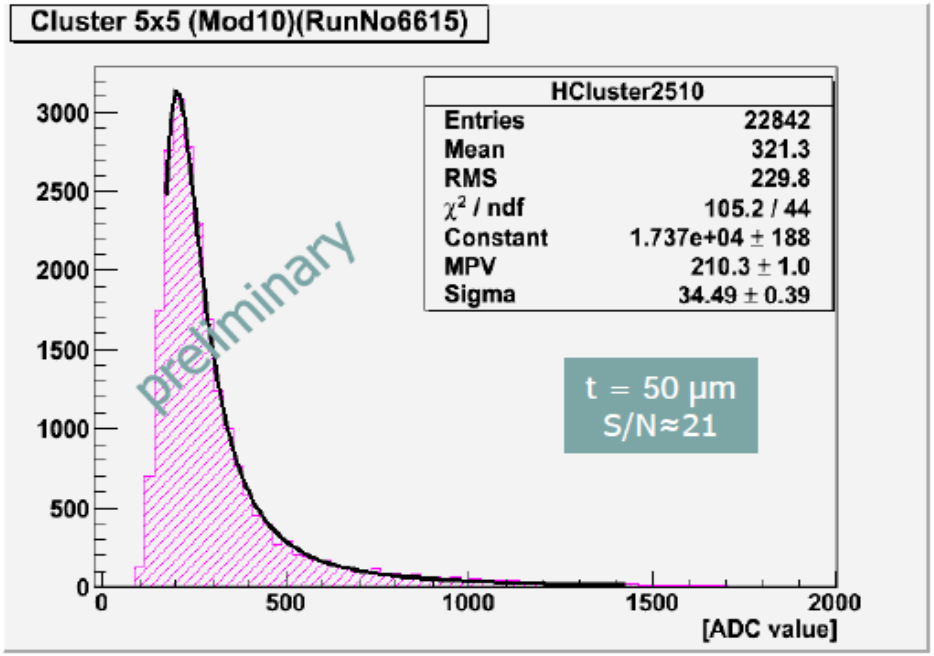
Signal measurements ^{90}Sr

- *2 DUTs: 32x64 pixels Belle II PXD design, L=6 µm, pixel size 50x75 µm2, same design on front, (CURO readout chip)*
  - I : 450 µm standard
  - II: 50 µm SOI



- β source, ~2MeV end energy, close to mip
- photons and LE e⁻ blocked by 4.3 mm plastic
- external scintillator trigger below the sensor

- from Cd90 we know: 1 ADU → 19.8 e⁻
- Sr90 signal with 50µm: 210 ADU → 4164 e⁻
- expect ~80e-/µm for a mip: ~4000 e⁻ for 50µm
- signal(450µm) : signal(50µm): 8.2



Conclusion

- *DEPFET is the baseline technology for Belle II PXD*
- *The high-precision, low mass DEPFET Pixel Detector is in the construction phase*
- *The first thinned sensor prototypes are currently being tested*
  - target read out time of 100ns/row is achieved
  - test shows that thin DEPFET have expected performance.
- *This project gives a strong push for the DEPFET for future e+e- colliders*
  - many techniques developed for Belle II are also applicable at future e+e- colliders

Thank you very much !

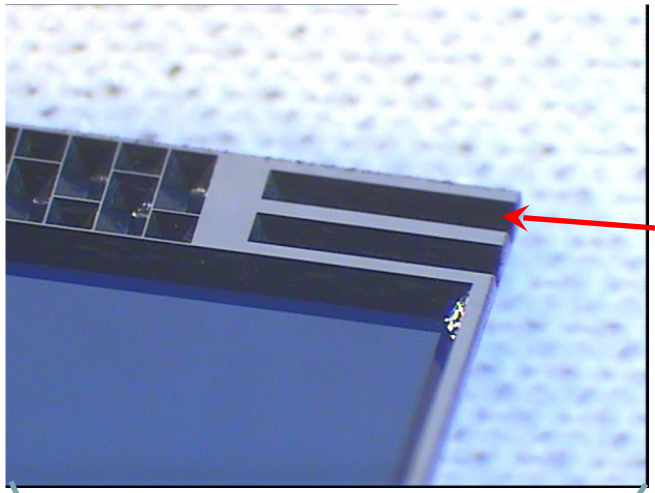
BACKUP slides

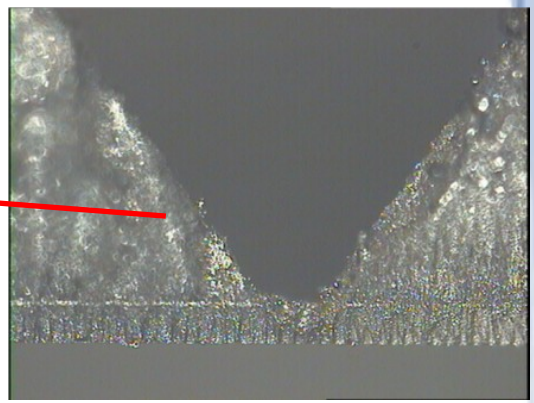
Micro joint between half-ladders

-butt joint between two half-ladders

-reinforced with 3 triangular ceramic inserts at the frame

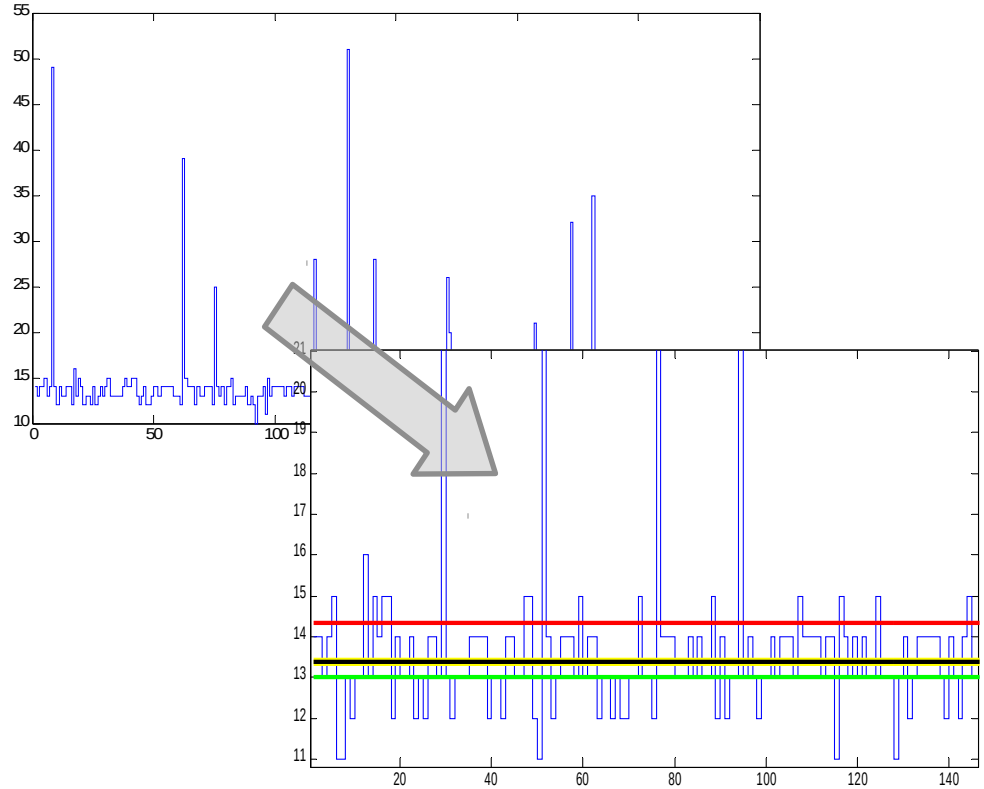
-about 2x300μm dead area per ladder





Common mode calculation

- *Pickup noise, common to all pixels in row*
- *Possible techniques:*
  - Simple average
    - + Easy hardware implementation
    - - Result is biased, especially for high occupancies (can be partially corrected offline)
  - Median estimator
    - + Unbiased
    - - Too resource hungry, difficult to implement in hardware within given constraints
  - Double parse average
    - +Unbiased
    - +Good resource compromise



- $\widetilde{CM} = \frac{\sum a_i}{N}$
- $CM = \frac{\sum \begin{cases} (a_i < \widetilde{CM}) : a_i \\ (a_i \geq \widetilde{CM} + Tr) : \widetilde{CM} \end{cases}}{N}$

the average is:	14.33
the median is:	13
the double average is:	13.38
the true common mode is:	13.4

DHP 0.2 Data Format

- *Frame Header SOF (32 bit): <data type | flags| frame ID>*
  - data type (3 bit): [raw data or 0-supp. data]
  - flags, not used yet (13 bit)
  - frame ID (16 bit)

  ➔ will always be send at start of a new frame, independent of trigger
- *Row Header SOR (16 bit): <flag = 0 | row address | common mode>*
  - flag (1 bit): 0 → row header
  - row address (9 bit)
  - common mode (6 bit)

  ➔ will only be send if hit data for the active row is available
- *Data Word DW (16 bit): <flag = 1 | column address | ADC>*
  - flag (1 bit): 1 → pixel data
  - column address (7 bit)
  - ADC (8 bit)

DHP 0.2 Data Format

- *Typical data stream:*

<SOF n><SOR m><DW i><DW i+x> … <SOR m+y><DW j><DW j+y> …
<SOF n+1> …

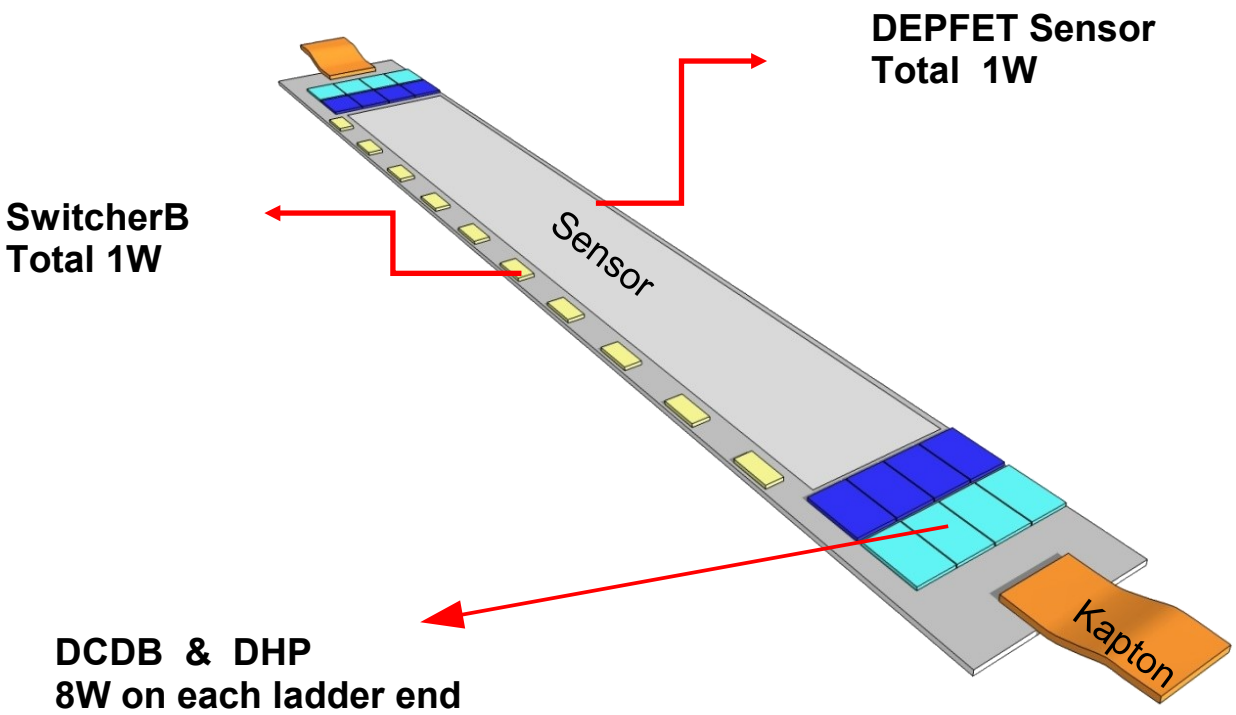
- *SOF will be send for every frame independent of trigger*

- *SOR will be send only if corresponding row contains hits*

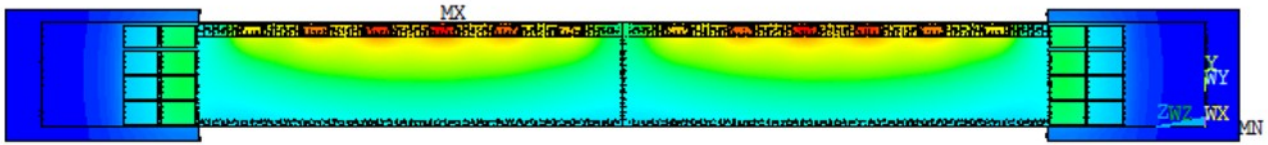
- *Data will be sorted*
  - Frame wise
  - Row wise
  - Column wise

- *Data form different DHPs will not be aligned*
  - Data per DHP (3% occupancy) ≈ 4 kByte

Temperature budget



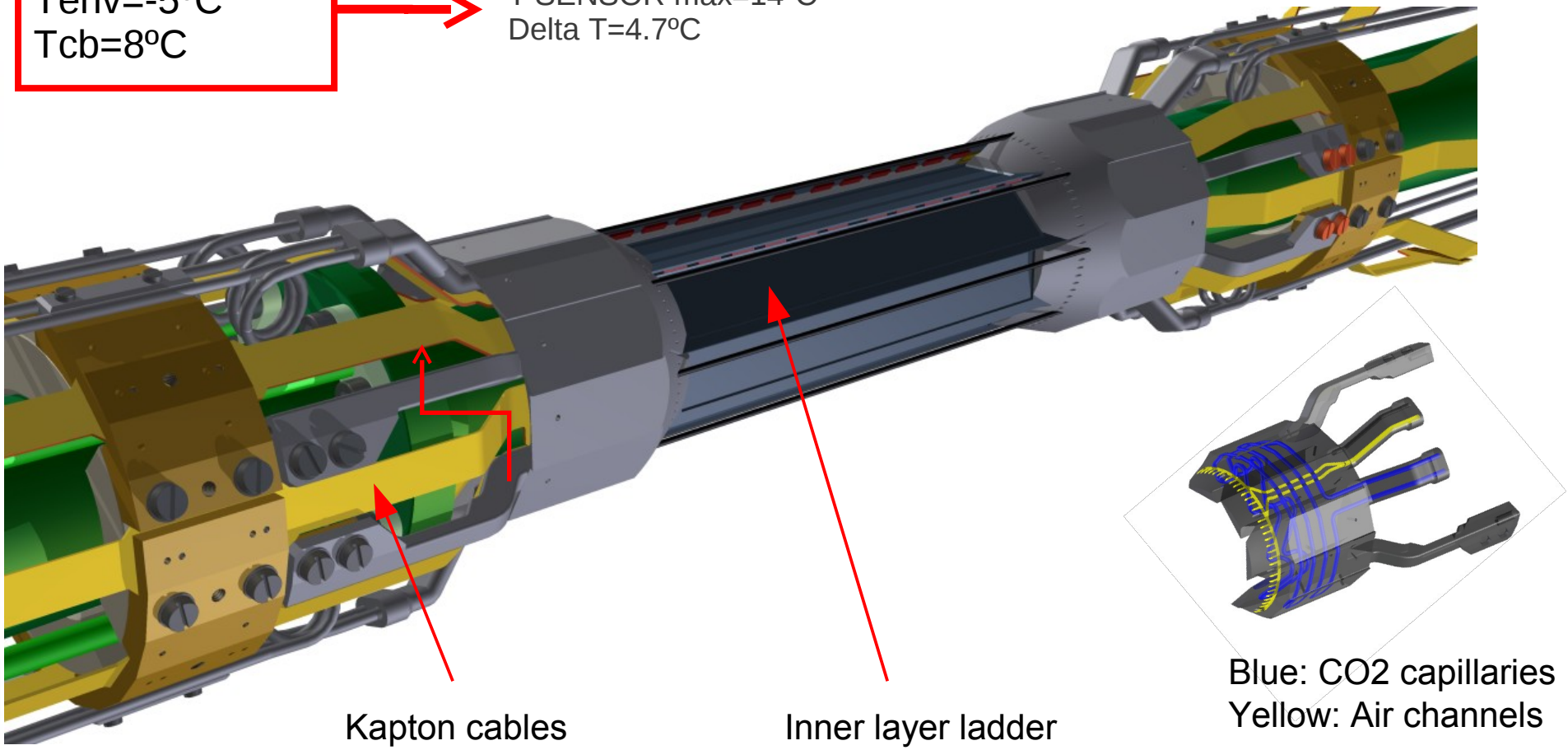
Support & cooling structure



Temperature distribution along the ladder

Tenv=-5ºC
Tcb=8ºC

T SENSOR max=14ºC
Delta T=4.7ºC



Blue: CO2 capillaries
Yellow: Air channels