PAUL SCHERRER INSTITUT

PSI

CMS

Compact Muon Solenoid

Data readout for the CMS pixel detector upgrade

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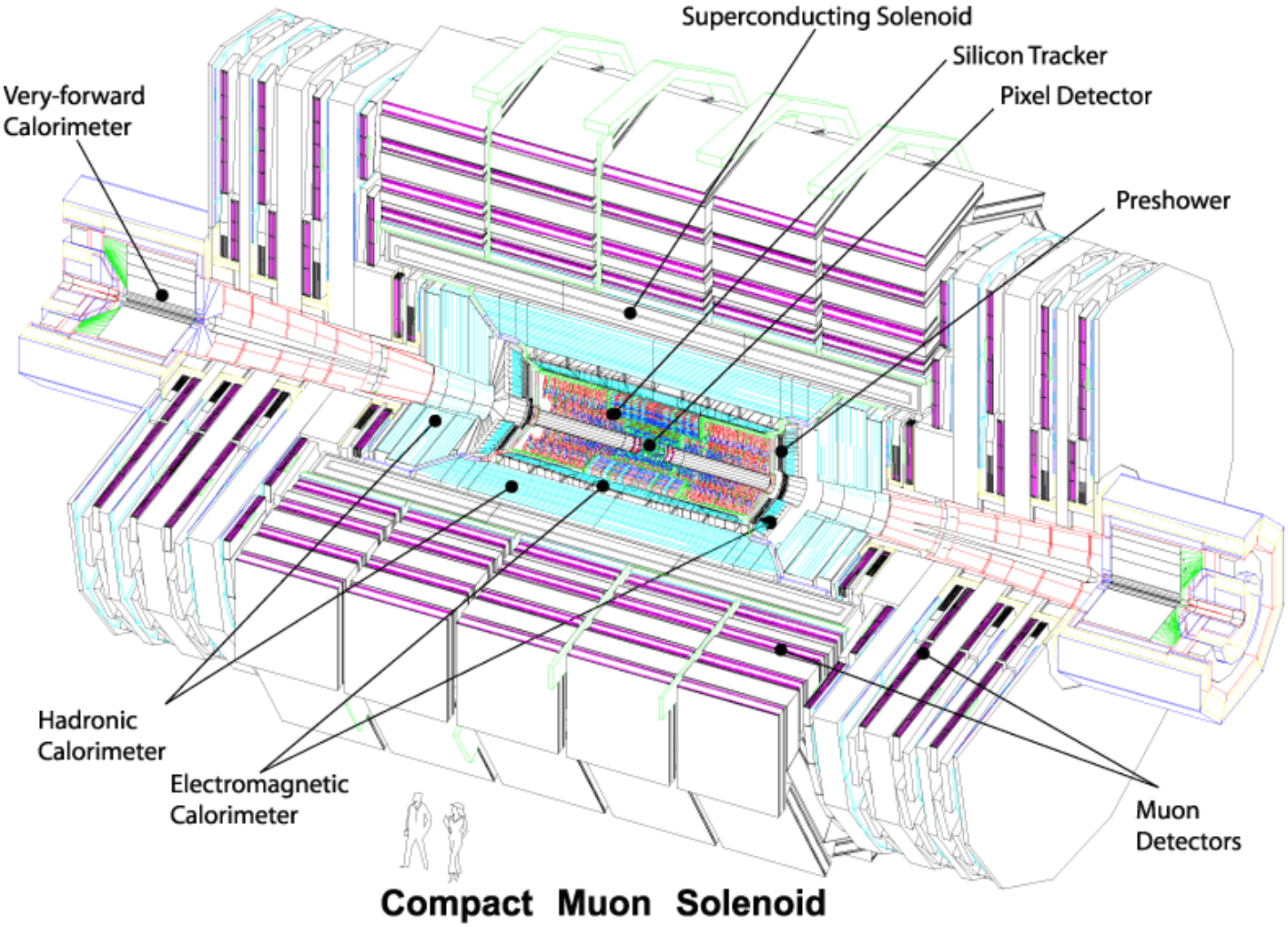
iWoRID 2011, July 6

Content

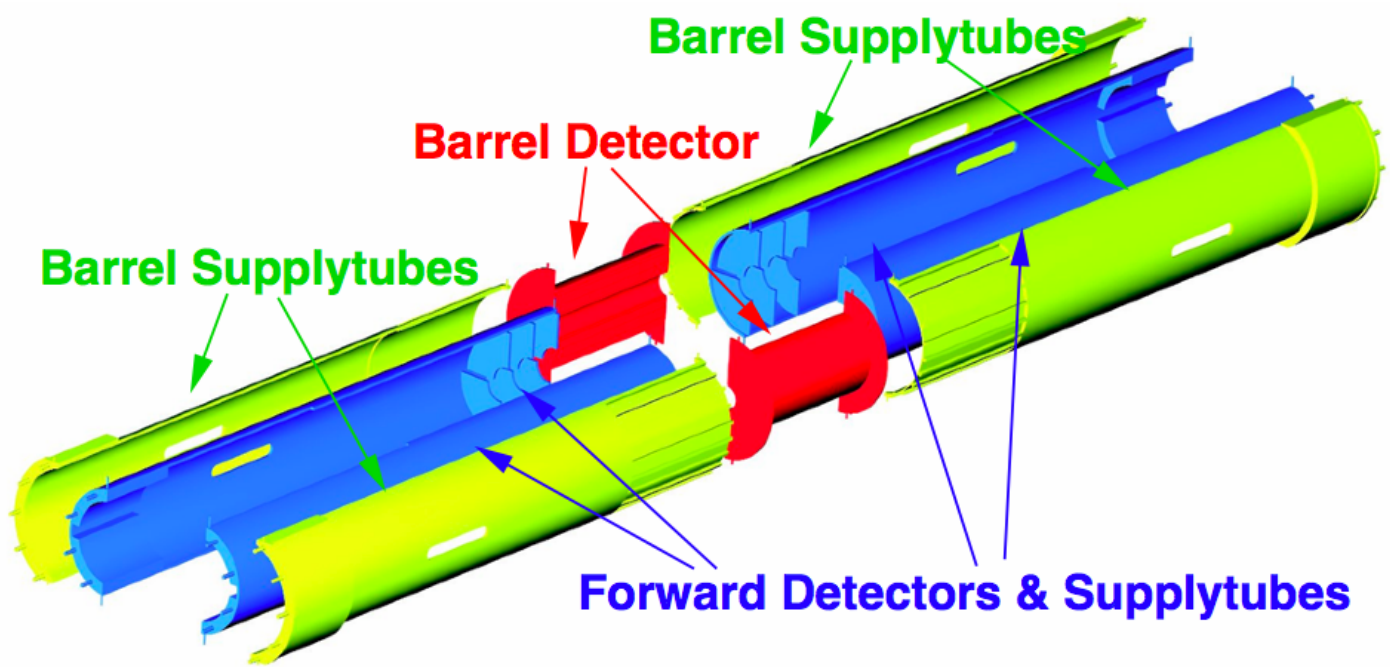
- Reminder: CMS and the pixel detector
- Overview of the pixel detector upgrade project
- Constraints and requirement
- Readout chain
- Module readout
- Readout chip
- Powering

The CMS Detector



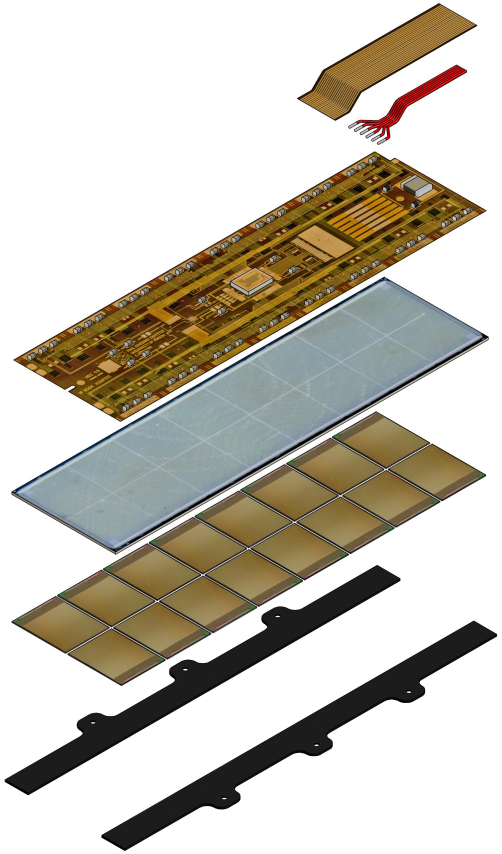
2008 JINST 3 S08004

CMS Pixel System



- Designed for fast insertion (beam pipe bake out)
- Will be done in regular shutdown
- Can be replaced by improved system

Barrel module



Kapton signal cable
Power cable

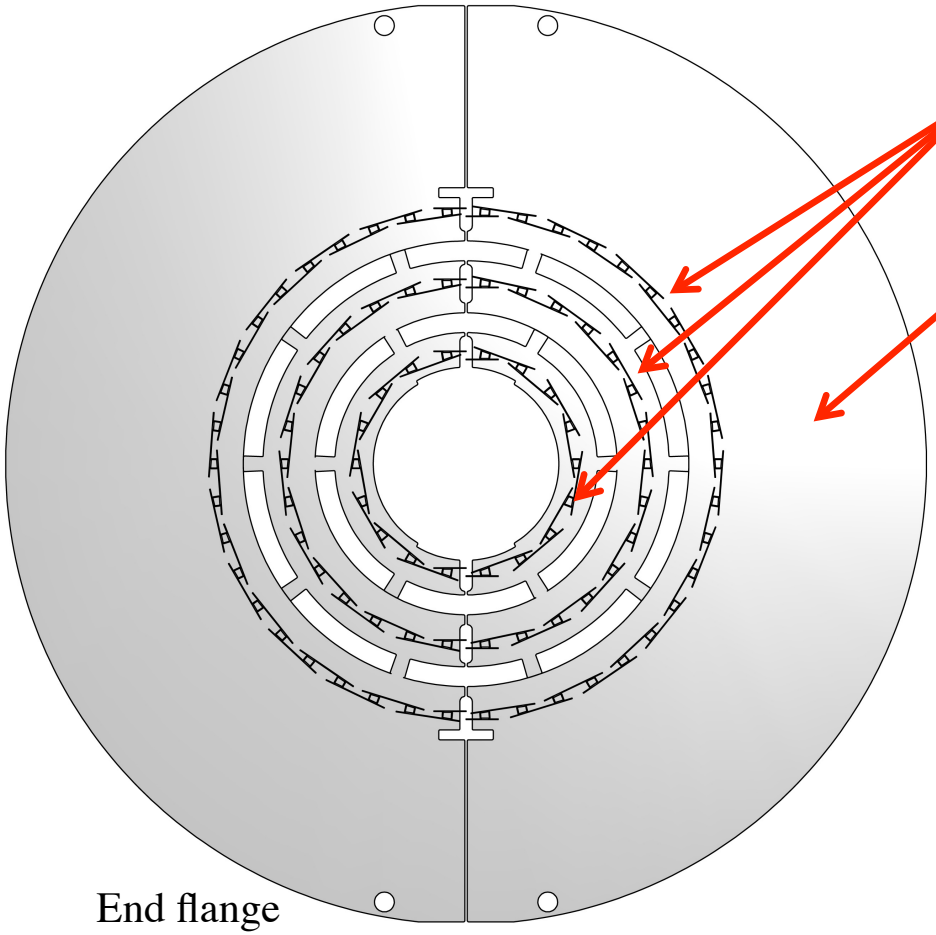
HDI

Sensor

16 readout chips

Mechanical support strips

Present barrel layout



- Two identical half shells
- 3 layers at R = 4.3, 7.2 and 11cm
- Empty volume
  - Strip tracker starts at R = 20cm
  - Track seeding in pixels. Have to extrapolate through ~9cm gap
  - More difficult at higher track rates
- Total area = 0.75 m^2, 784 modules
  - 1 type of full module
  - 2 types of half modules
  - At least 100 different cable lengths

Barrel detector upgrade

Add 4th layer :

- layers @ 39(29?),68,109 & 160 mm
- beam pipe clearance 4(<2) mm
- 8 modules along z (1216 total)
- ‘ultra‘ light support structure
- No large empty volume, excellent pointing precision of track seeds
- Area ≈ 1.21 m^2, 1216 modules (full modules only)

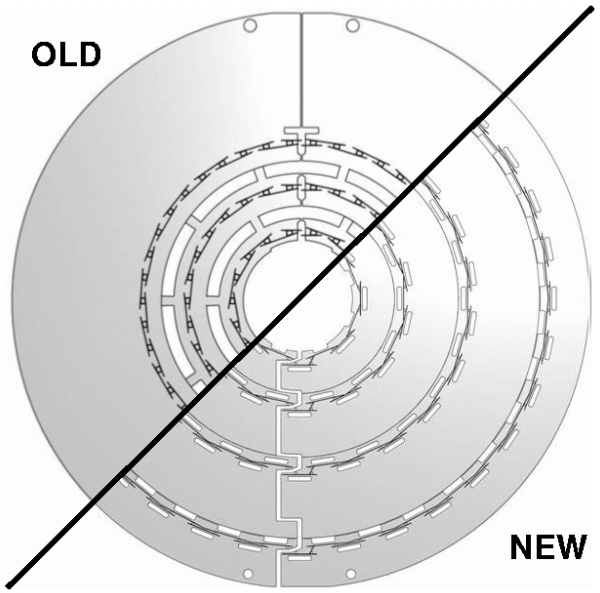
CO_2 based cooling system

→ Less material

→ more robust (standalone) tracking

→ better connection to strip tracker

Barrel detector

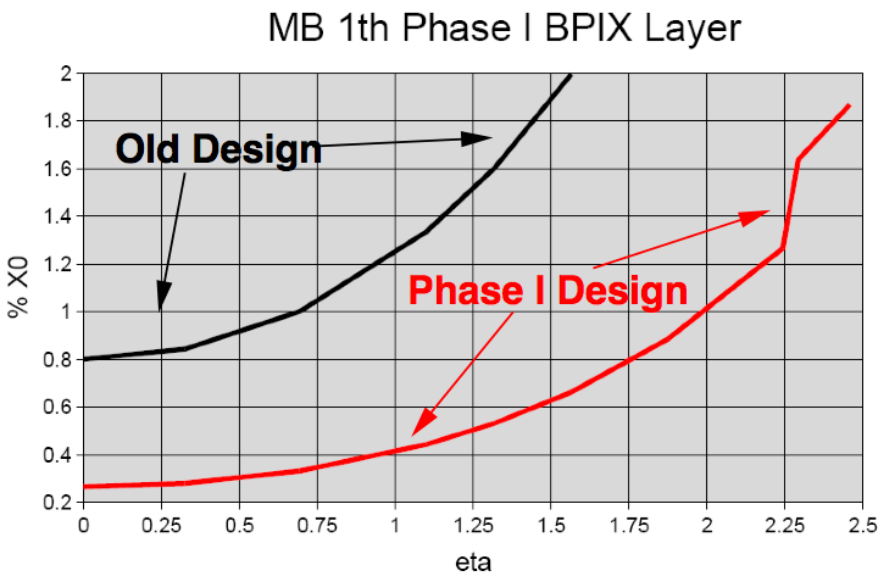


New layer 1 mechanics

Layer 1 prototype:

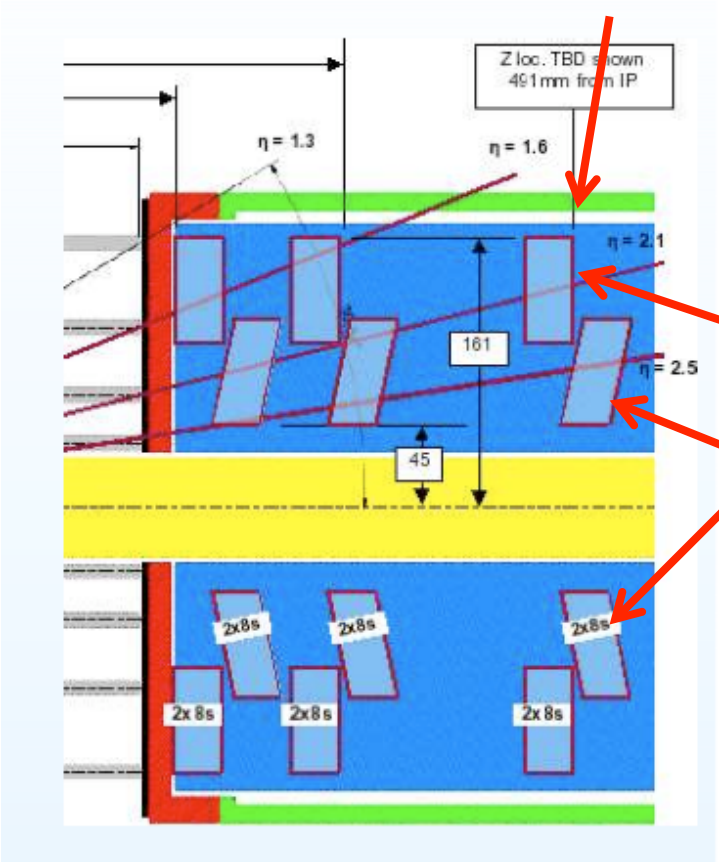
- 200 μm carbon fiber
- 4mm Airex foam
- Stainless steel tubes:
  - 1.5 mm OD, 50μm wall
  - Tube bends: 1.8mm OD, 100μm wall
- tested: ~100 bar & -10°C..10°C

- Factor >3 gain in material budget
  →4 layer system will have 50% of material budget of old 3 layer system



End disk detector upgrade

Add 3rd disk

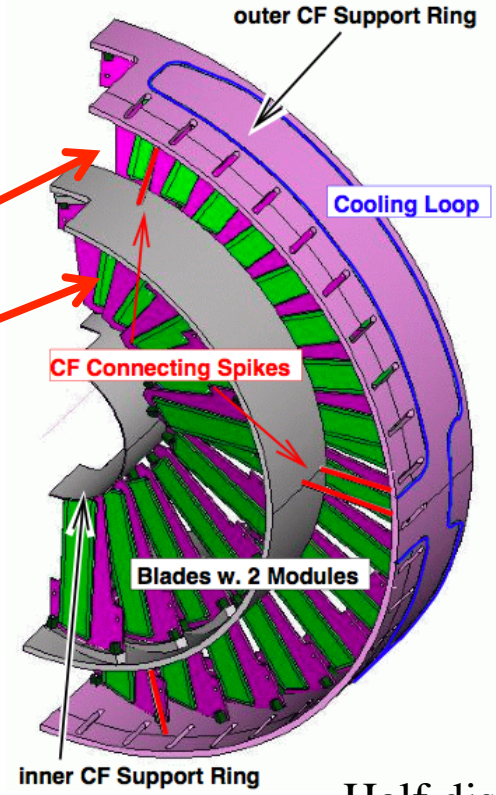


Side view of end disk region

Outer ring

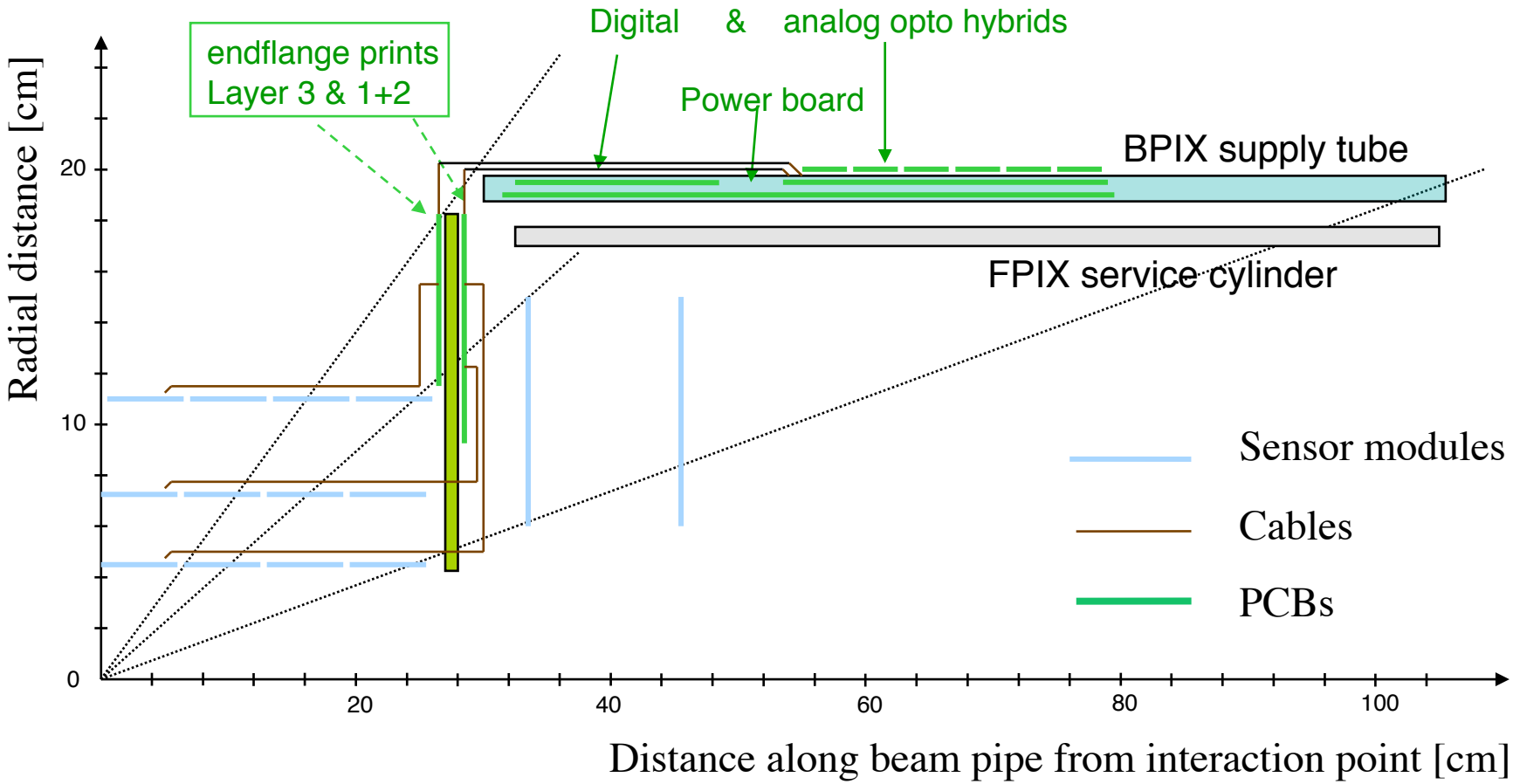
Inner ring

Change disk design from single ring design to two ring design
→ Only one type of modules.
Similat to barrel modules



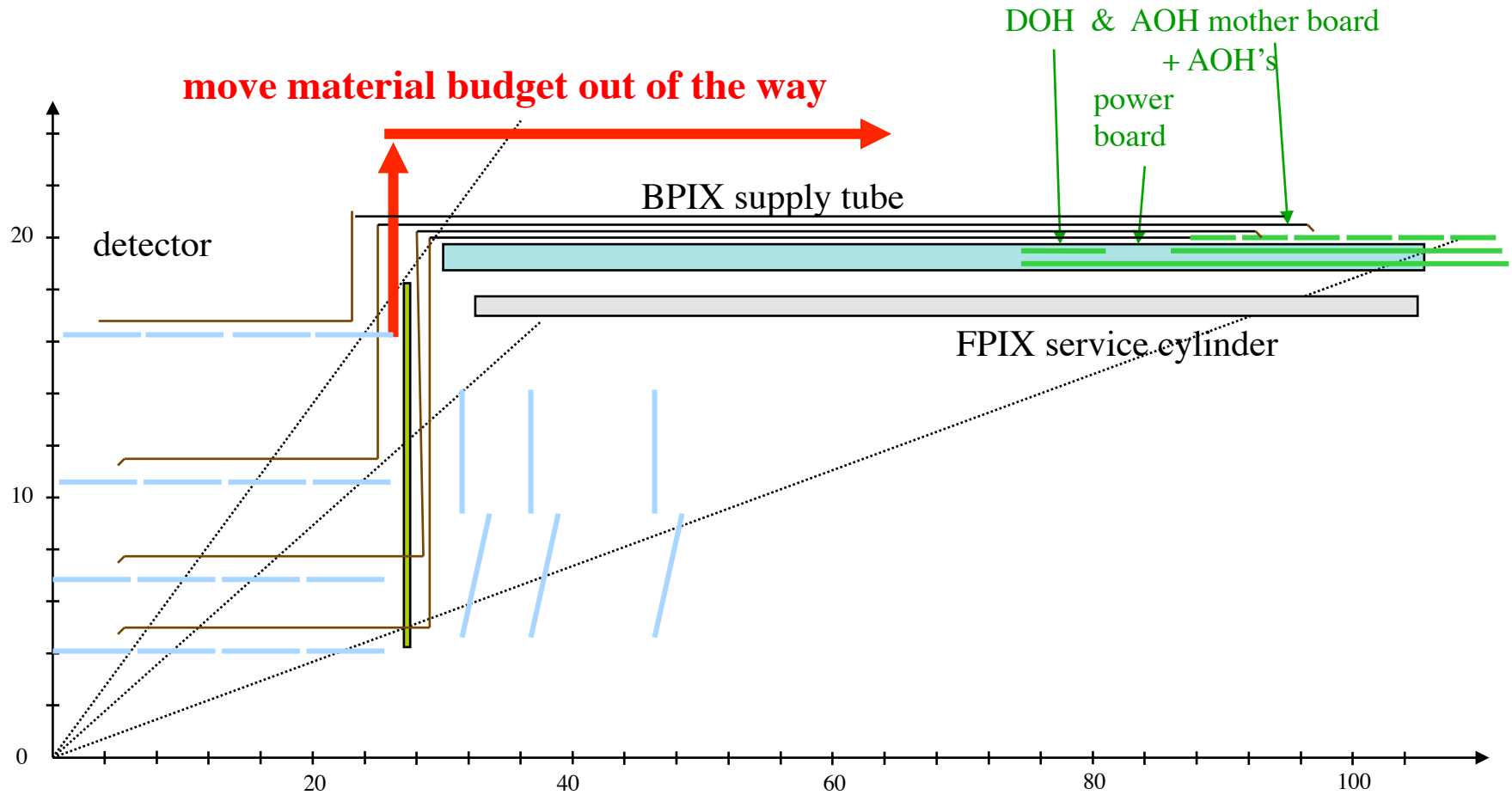
Half disk

Reduction in Services



Reduction in Services

- Modules with long pigtails (1.2m) **CCA μ-twisted pairs** 16x(2x125μ)
- Move DOH & AOH boards back by 50-60cm



Constraints and Requirements

Same/better performance:

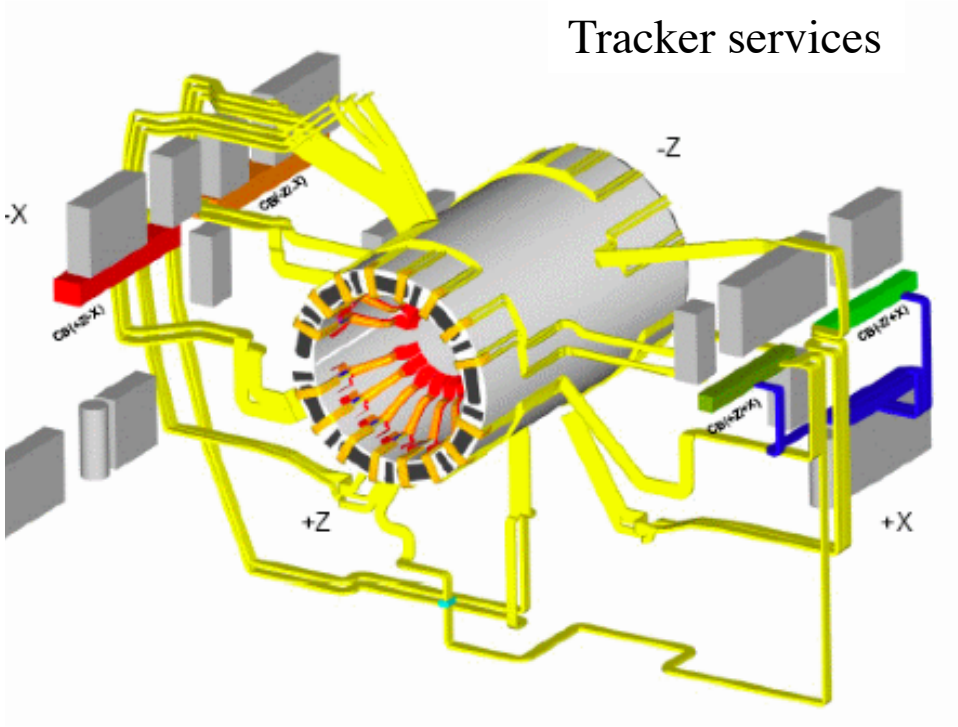
- Higher efficiency at higher rates
- reduce material effects (multiple scattering, photon conversion)

Have to use existing services:

Cooling pipes, power cabling, fibers

But we have **60% more modules**

- data rate → faster readout (digital)
- Power→ DC-DC converters



Short commissioning time:

We are in a competitive physics situation

→ Leave system unchanged as much as possible

- keep ROC core untouched, it is well debugged.
- Keep control links as is. This leaves pixel operation similar to today

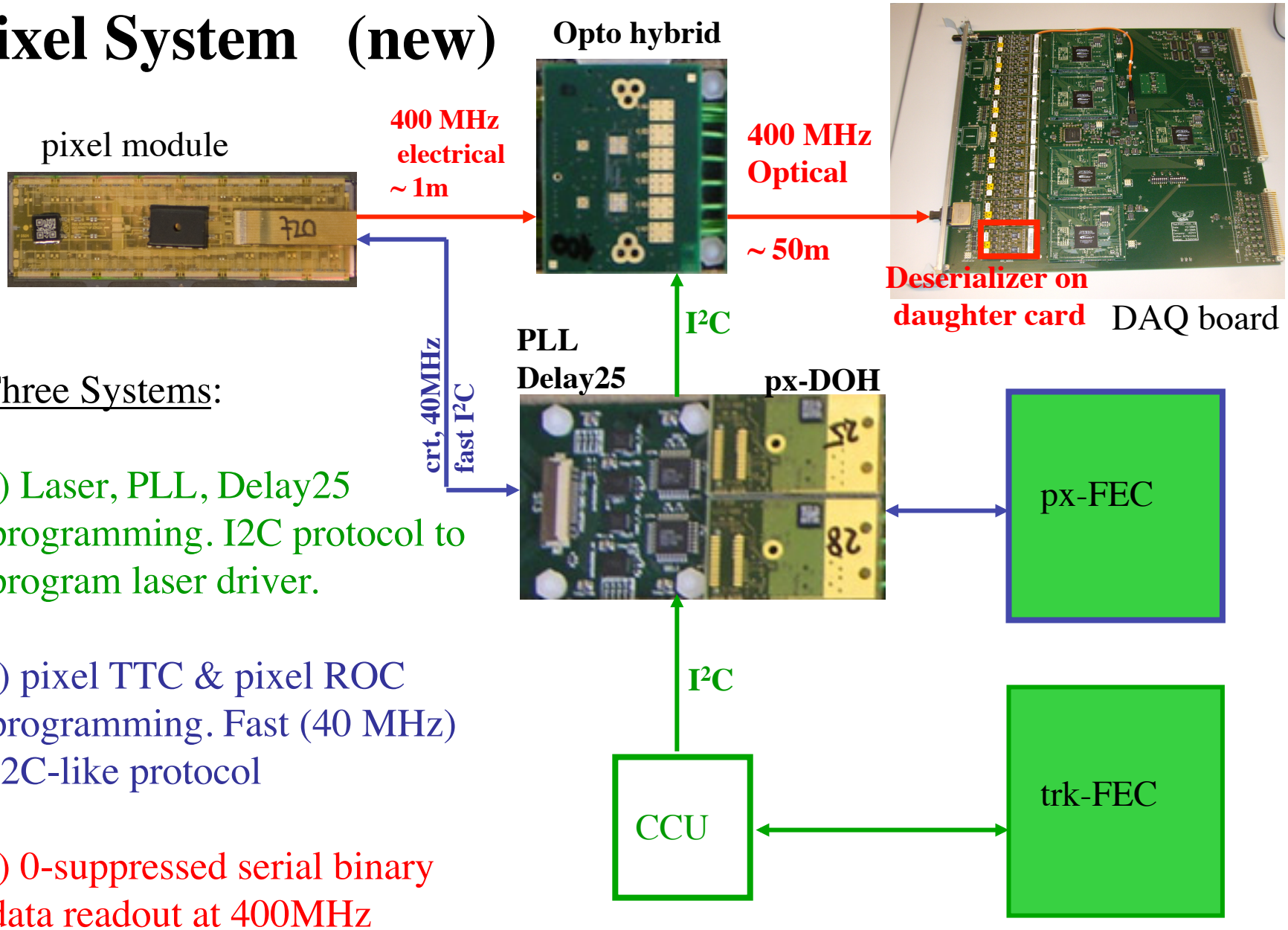
Not shown: 10'000 tons of steel!

Data Rate Estimations

- Full 4 layer phase I geometry
- Simulation with Pythia and GEANT4
- Assuming 24 bits per hit, 100 kHz level 1 trigger rate
- Peak luminosity = $2x10^{34}cm^{-2}s^{-1}$, σ_{tot}=80mb, σ_{signal}=1.5mb
- Data rate includes headers/trailers
- Bandwidth of present analog links ≈ 100 Mbit/sec peak

Layer	1	2	3	4
Pixel fluence [MHz/cm^2]	331	107	49	28
Hits / trigger / module	92	35	16	8.4
MBit/link/sec	265	107	61	40.0
# links	128	224	352	512

Pixel System (new)



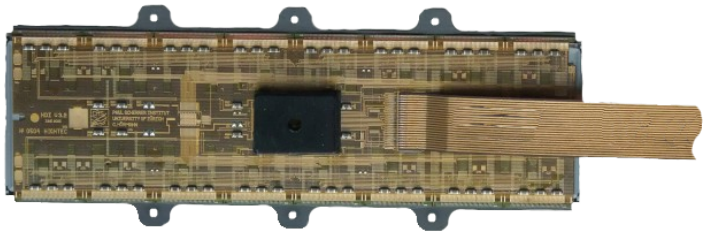
Three Systems:

1) Laser, PLL, Delay25 programming. I2C protocol to program laser driver.

2) pixel TTC & pixel ROC programming. Fast (40 MHz) I2C-like protocol

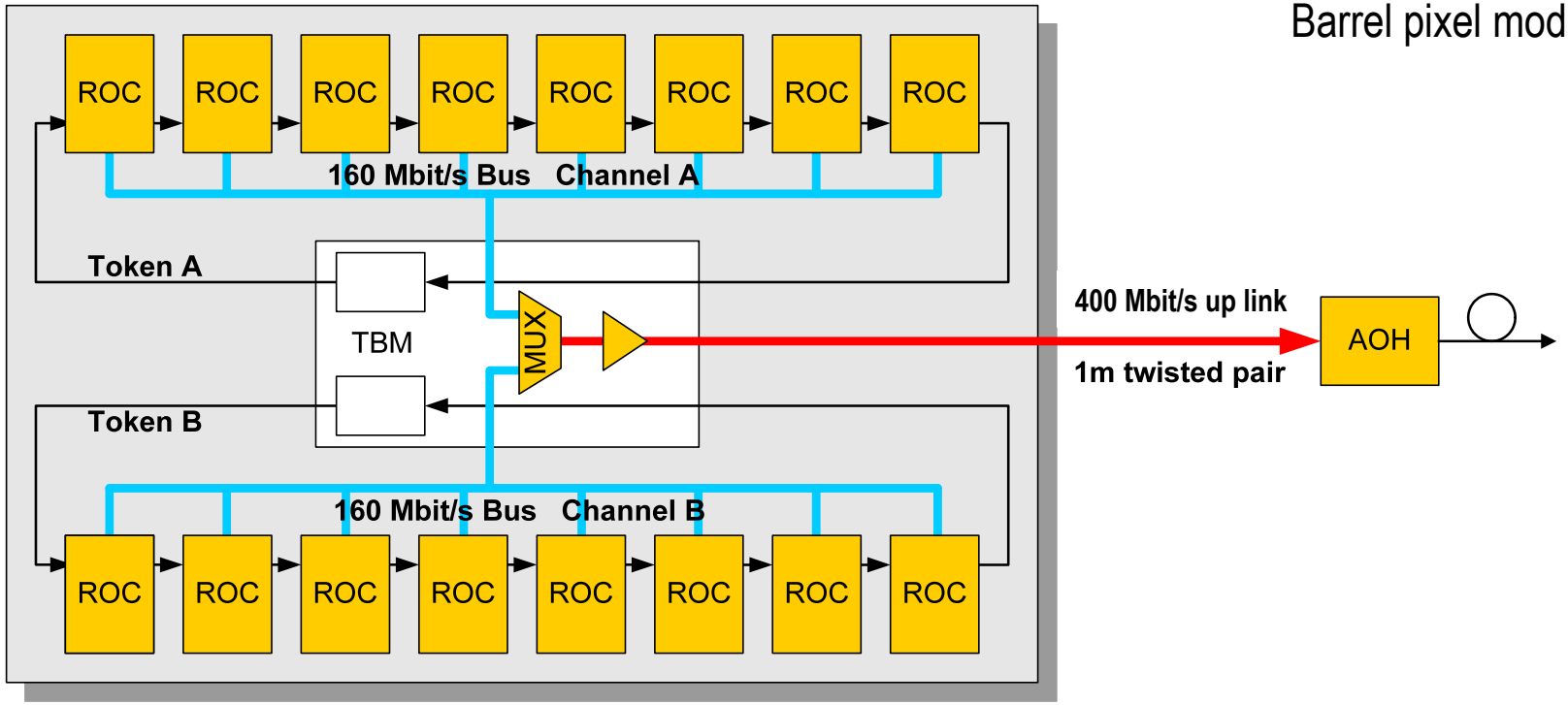
3) 0-suppressed serial binary data readout at 400MHz

Module readout

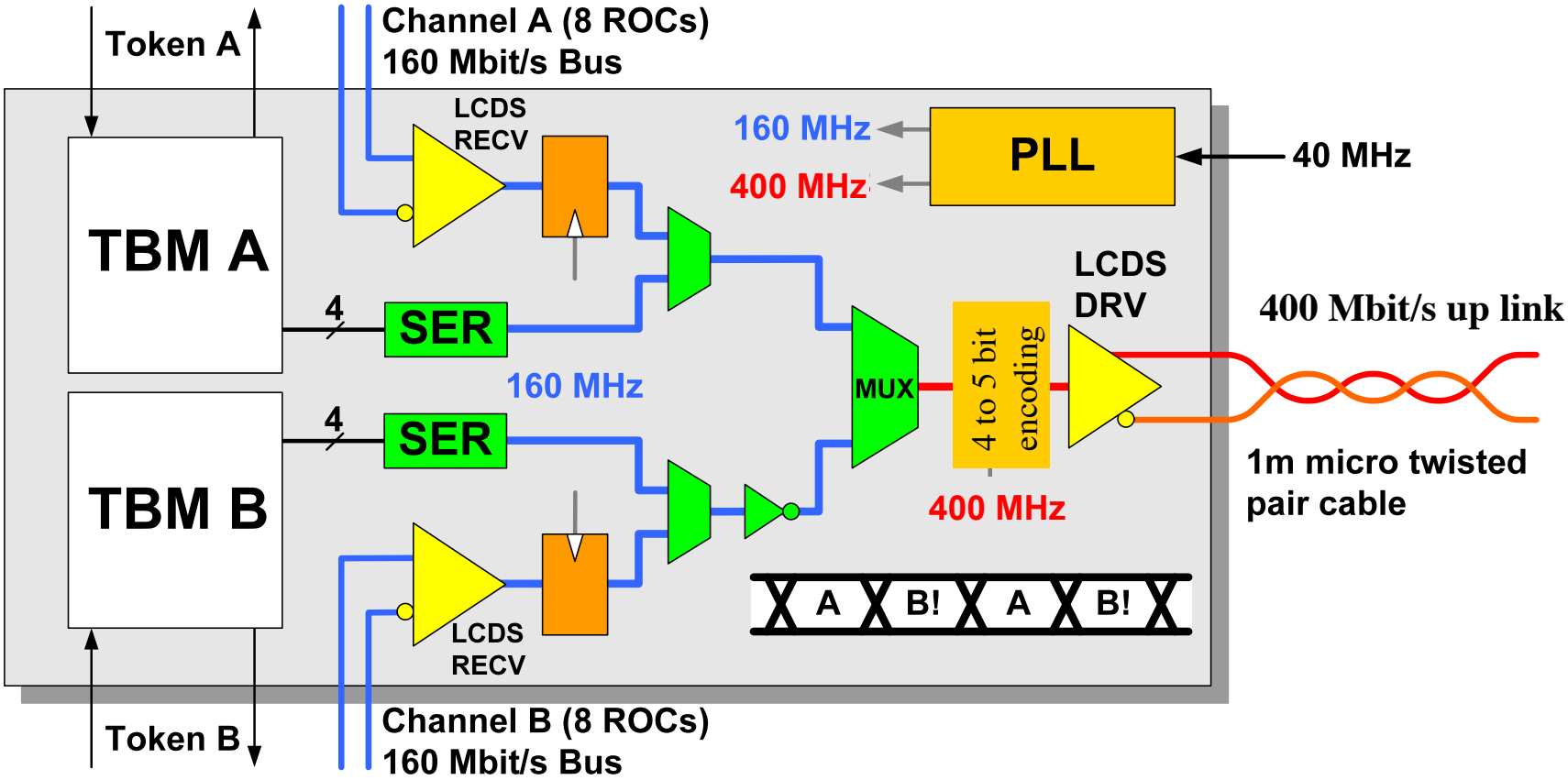


Barrel pixel module

New Readout Scheme



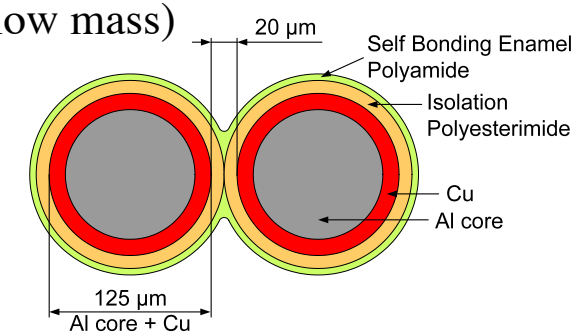
Module Controller: TBM



Dual core: each core controls 8 ROCs

Electrical Low Power Data Link

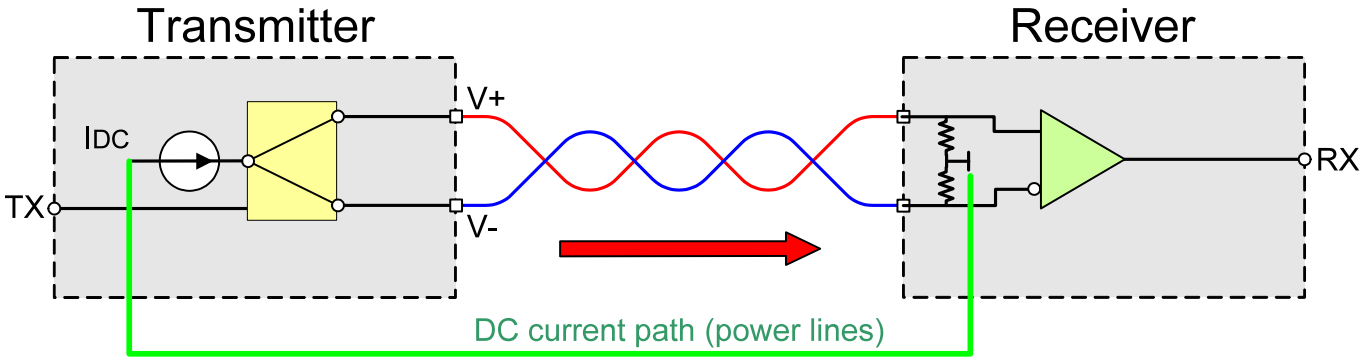
- 400 MBit/s over 1 m
- Unshielded micro twisted pair cable (125 μm wire diameter, low mass)



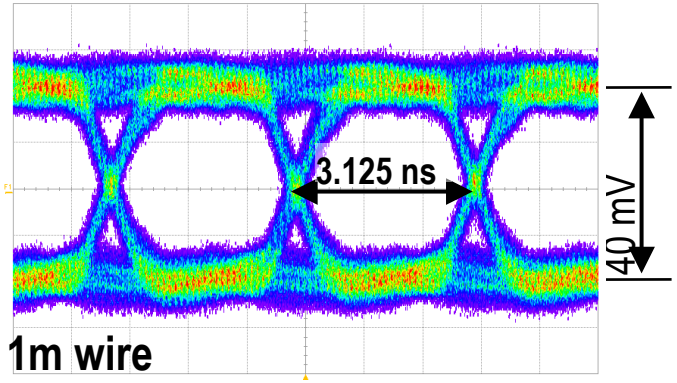
Electrical characteristics:

- Impedance: 50 Ohms (very low for differential line)
- Impedance change: 1.3 Ohms per 1 μm distance variation
- $v = 2/3\ c_0$ (5 ns/m)
- C = 100 pF/m, L=250 nH/m

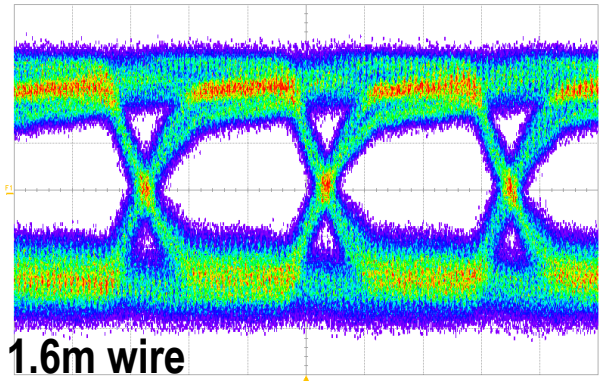
- Low power differential driver and receiver (LCDS)
- Bundled with power and control wires to one module cable



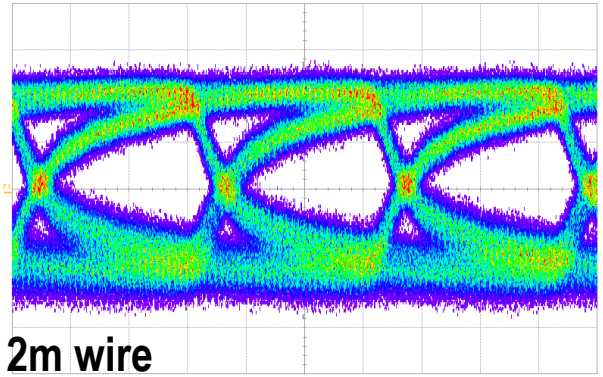
Results, Eye Pattern



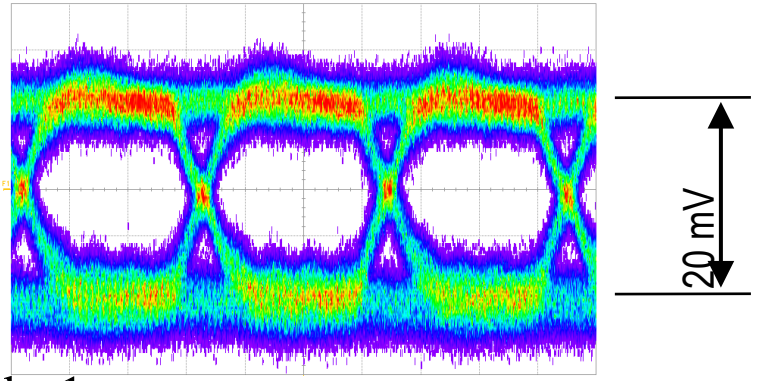
1m wire



1.6m wire



2m wire

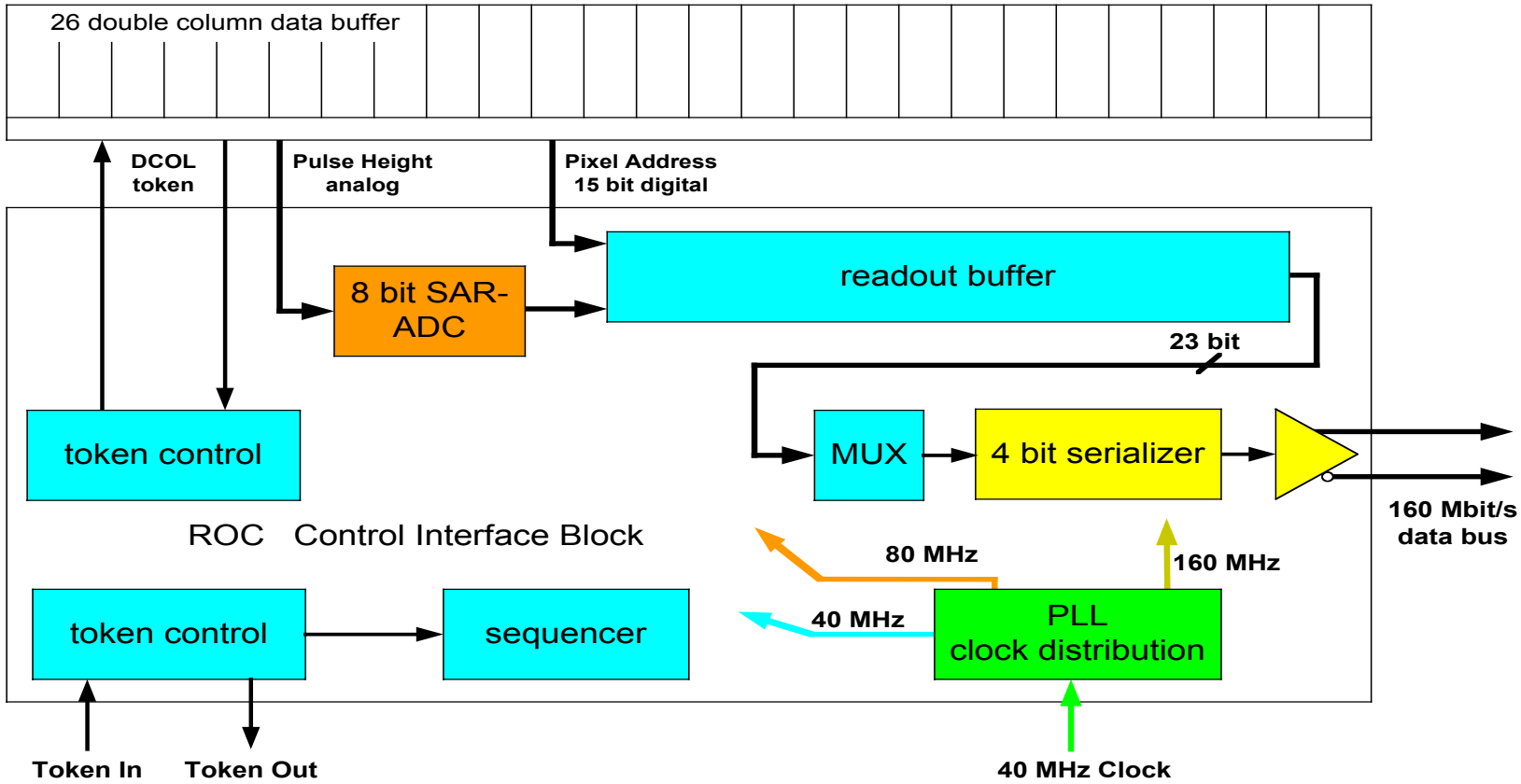


- Wire length: 1 m
- 320 Mbit/s
- Minimal amplitude: 20 mV (+/- 10mV)
- +/- 500 mV DC offset between driver and receiver
- Bit error rate < 10e-12 (different condition)
- Crosstalk: -27 dB
- Power consumption / link: 4mW (12 pJ/bit)

ROC modifications

- Higher rate capability
  - Larger L1 latency buffers with denser layout to reduce trigger latency related data losses
  - **Additional readout buffer stage to lower readout related data losses equalize data fluctuations (→allows operation at higher link occupancy)**
- **Change readout to digital scheme**
  - **Substantially increase readout bandwidth**
- Lowering operational signal threshold
  - Lower threshold translates directly into longer lifetime of detector (less charge from sensor)
- Miscellanea
  - Operational improvements
  - Further optimization of current consumption

Upgrade to Digital Readout



Readout chip periphery

Critical building blocks

- PLL for 160 MHz
  - Components designed and tested. Work very well.
  - Irradiation tests with ^{60}Co source made with ring oscillator at PSI up to 40 Mrad.
  - Max frequency reduced by <10%. Still above 440 MHz
  - Will continue to irradiate
- Serializer running an 160 MHz. To be tested
- Output signal driver. Slight improvements will be made
- ADC running at 80 MHz (see next slide)

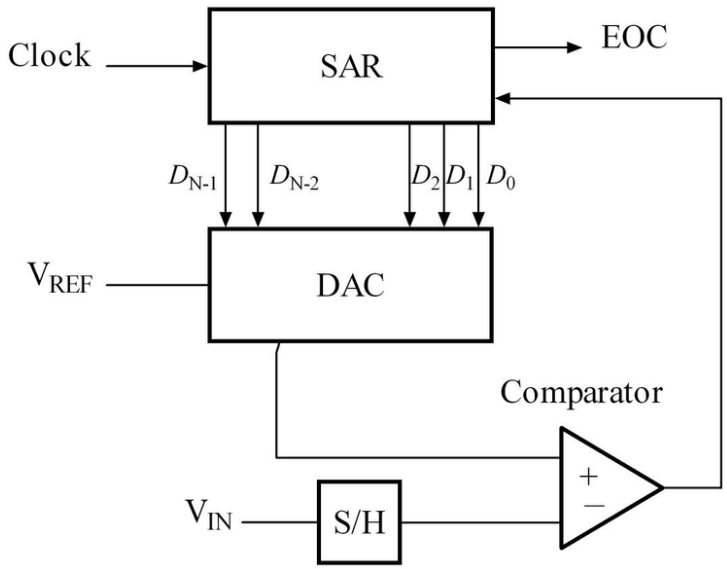
8-bit ADC: design

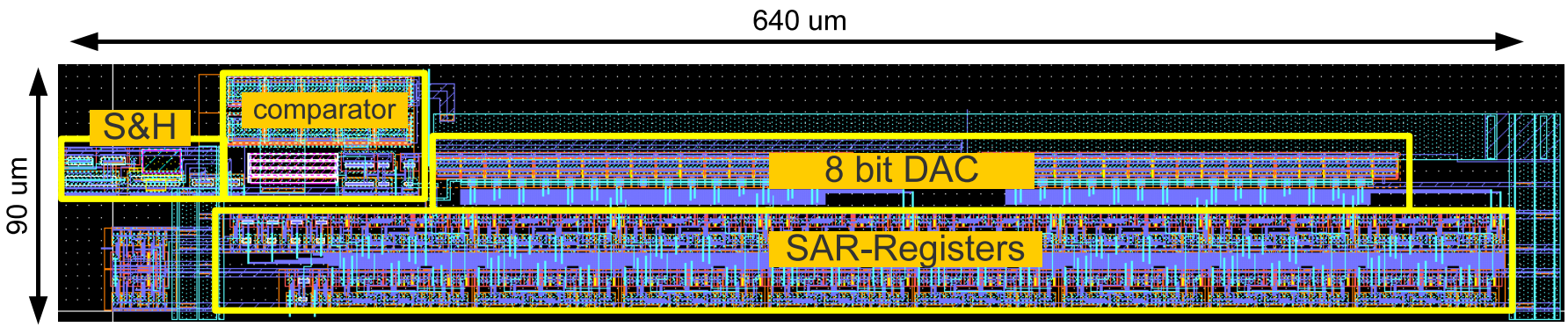
Design

- Successive approximation 8 bit ADC with S&H
- Clock frequency: 80 MHz
- Conversions time: 8 clock cycles

Test Results

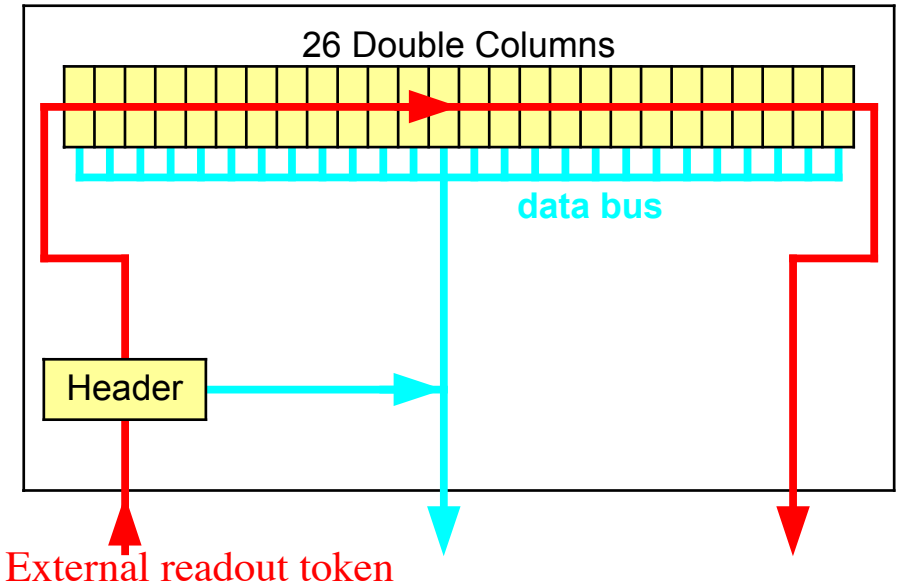
- Non linearity within 1 digit
- Supply current 1 mA (2% of ROC power)
- Speed problem and oscillation, both concerning the comparator → comparator optimization done



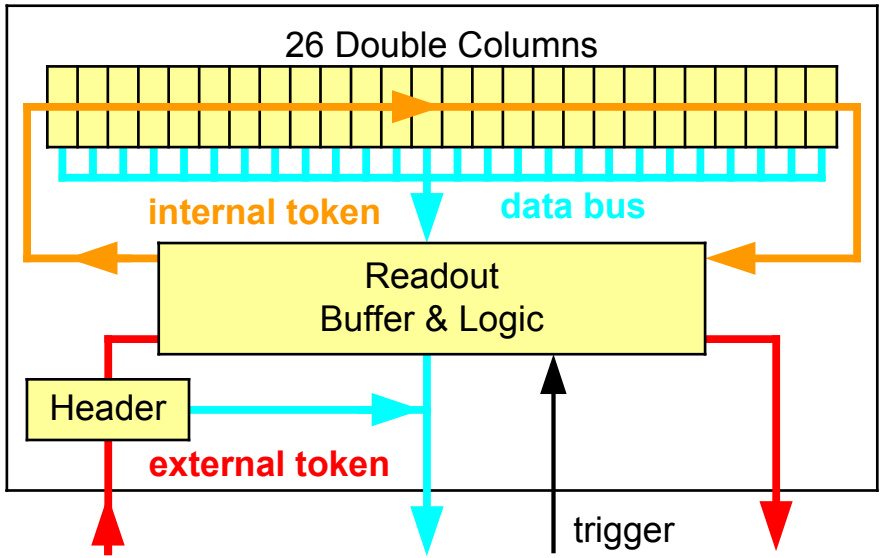


Buffered Readout

present ROC



new ROC

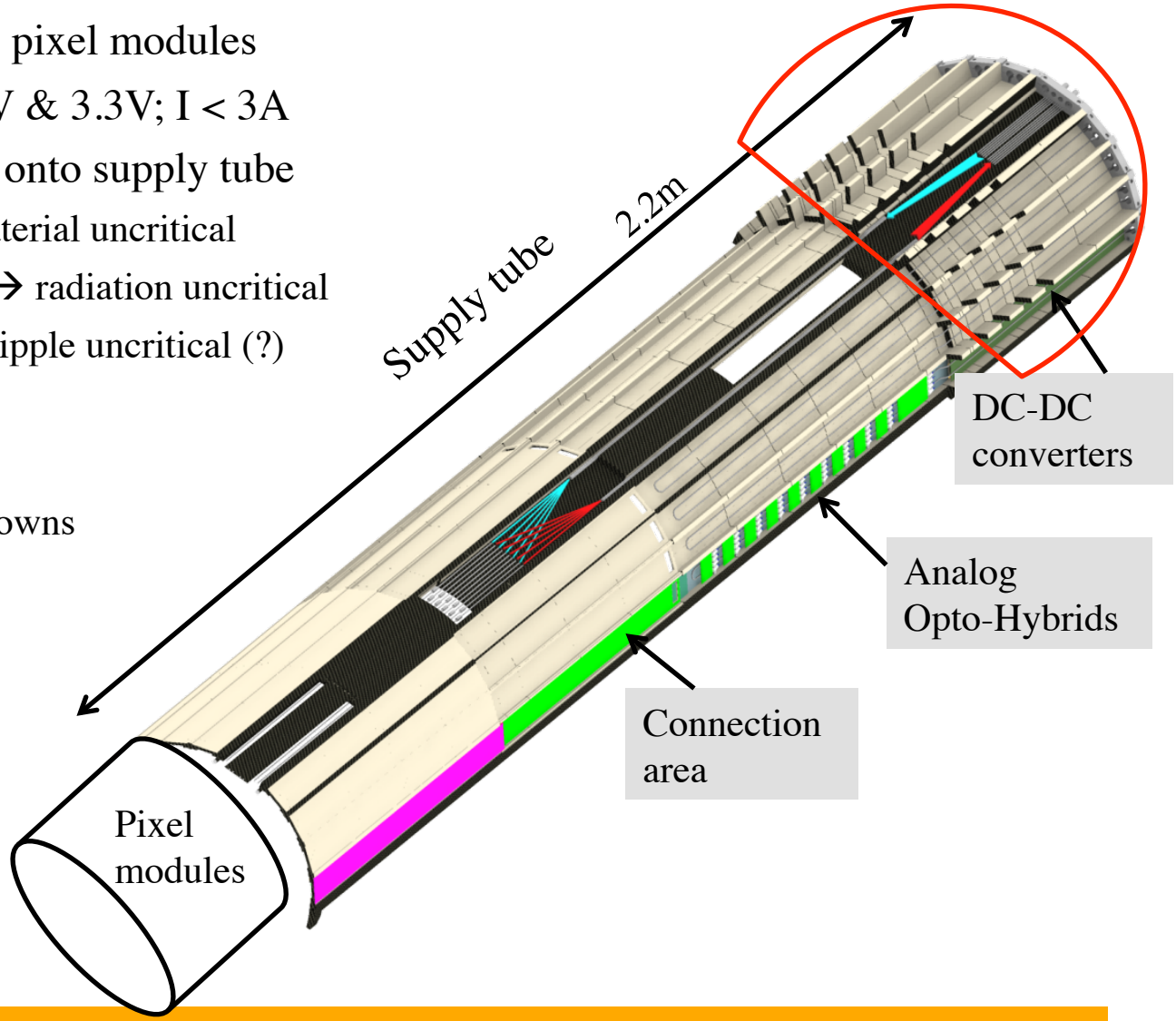


- Double columns with verified data stops → no more events accepted until r/o finished
- Double columns have to wait for external readout token → long dead time
- Sequential readout of 16 ROCs → high token delay

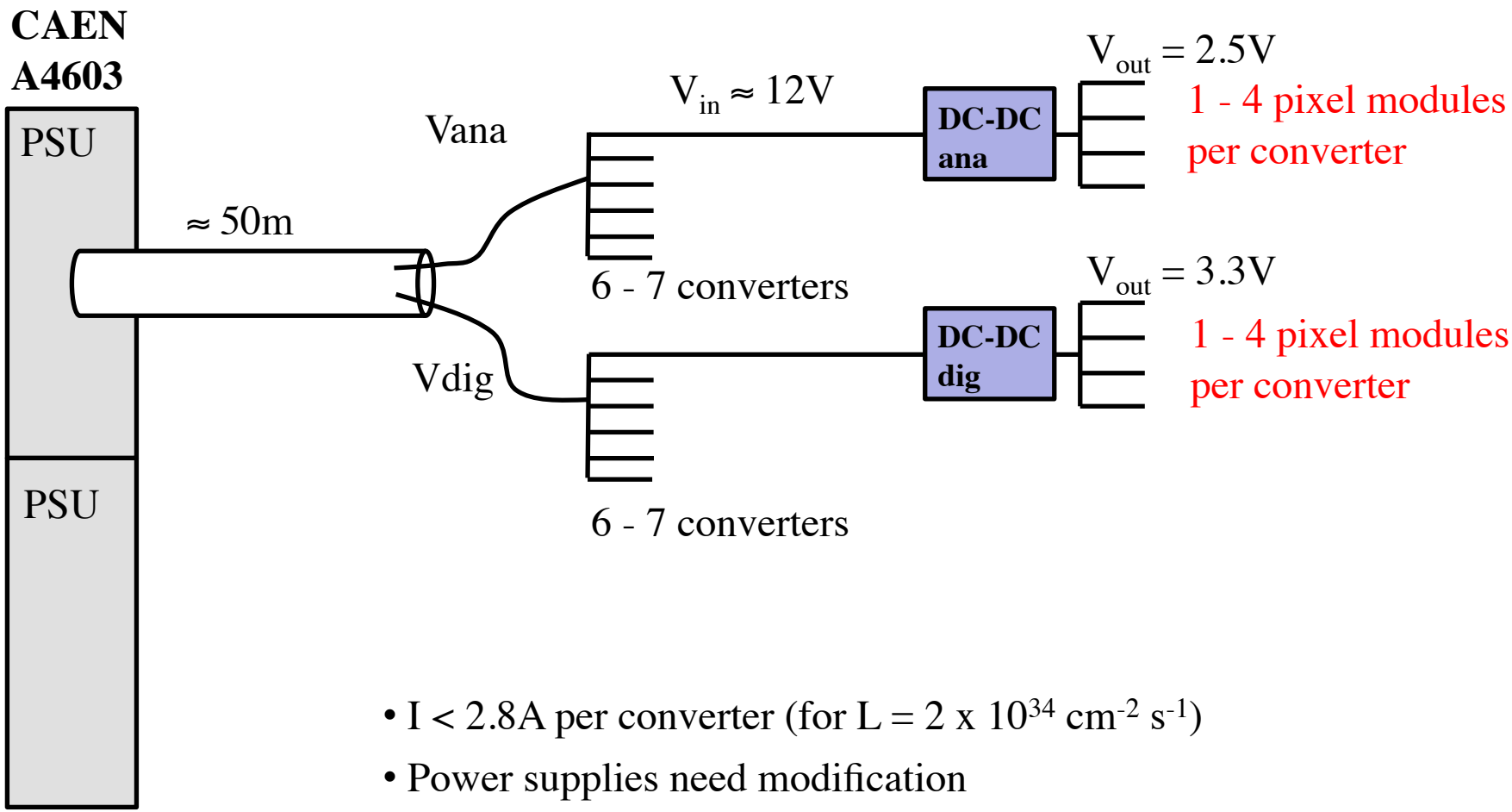
- DCol readout parallel in all ROCs after trigger → reduced waiting time
- ROC readout buffer: read/write simultaneous; data with different time stamps
- Easy implementation in separate buffer on ROC → keep present DCol logic unchanged

Powering: DC-DC converter

- One converters powers 2-4 pixel modules
- Conv. ratio 2-3; V_{out} = 2.5V & 3.3V; I < 3A
- Integration for pixel barrel onto supply tube
  - ✓ Pseudorapidity $\eta \sim 4$ → material uncritical
  - ✓ Large distance to modules → radiation uncritical
  - ✓ Fast on-chip regulators → ripple uncritical (?)
  - ✓ Space tight, but managable
  - ✓ CO_2 cooling
  - ✓ "Easy" access during shutdowns



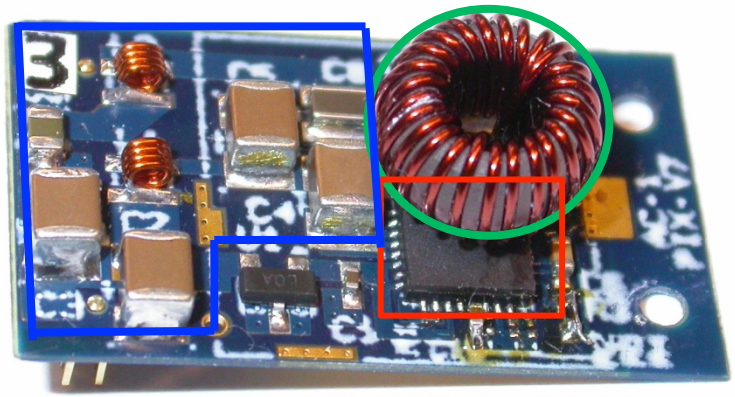
Integration into Phase-1 Pixel Detector

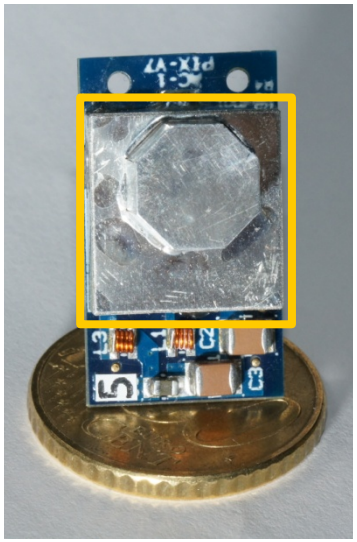


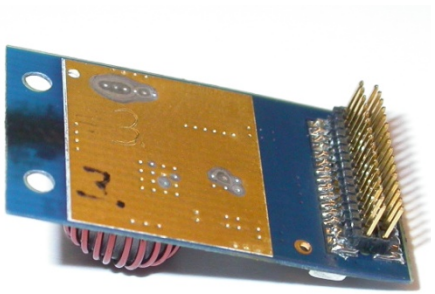
- $I < 2.8A$ per converter (for $L = 2 \times 10^{34}$ cm^{-2} s^{-1})
- Power supplies need modification
- No remote sensing

DC-DC Converter

“PIX_V7“:





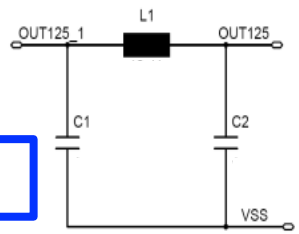


A = 28 x 16 mm^2
M ≈ 2.5g
3.8% of a radiation length

ASIC: AMIS2 by CERN
I_{out} < 3A
V_{in} < 12V
f_s configurable, e.g. 1.3MHz

PCB:
2 copper layers a 35μm
0.3mm thick
Large ground area on bottom for cooling

Toroidal inductor:
L = 450nH
R_{DC} = 40mΩ
Plastic core

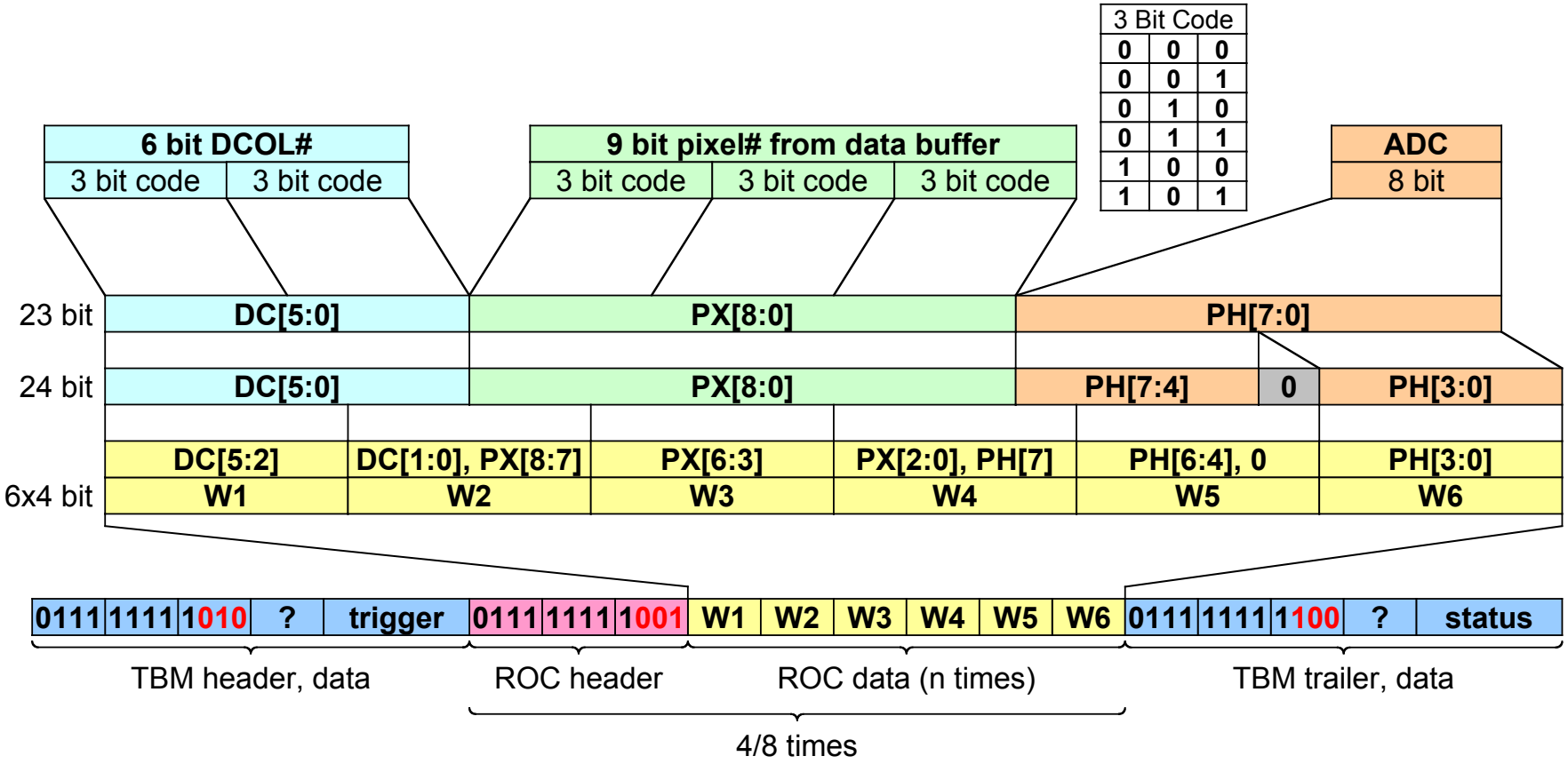


Pi-filters at in- and output

Shield

Backup slides

Digital Data Format



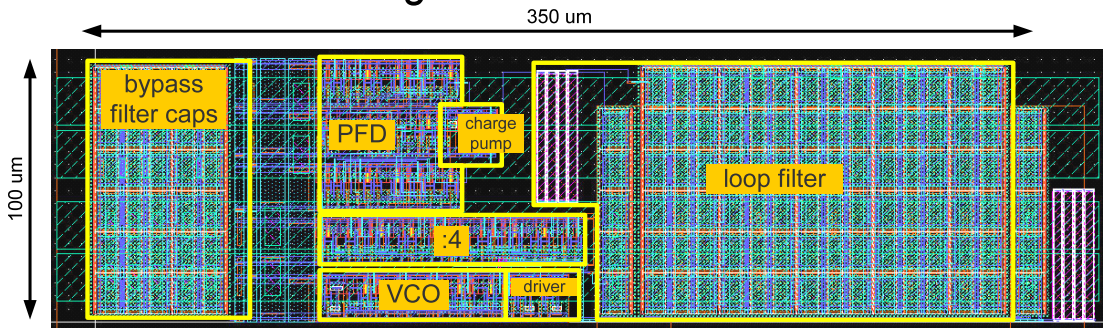
- Running at 160 MHz from ROC to TBM, 400 MHz from TBM to FED
- Needs fast on chip ADC running at 80 MHz

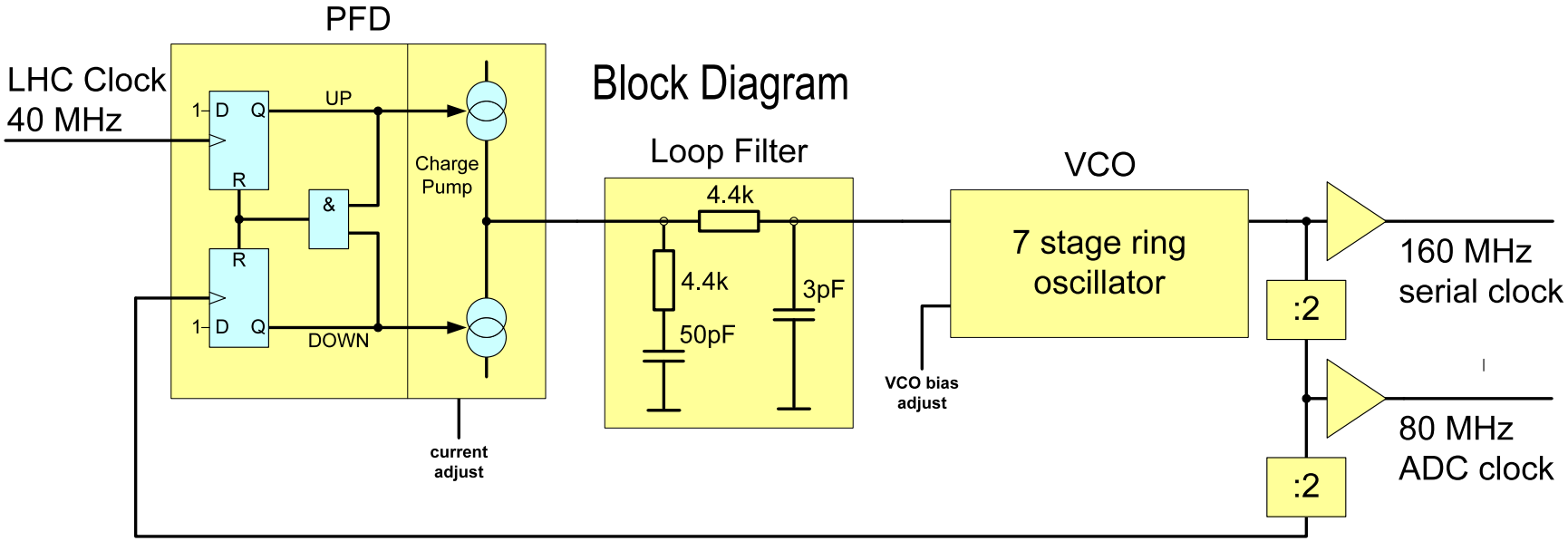
Frequency Multiplier PLL Design

Technical Data:

- Reference input: 40 MHz
- Outputs: 80 MHz (ADC), 160 MHz (serializer)
- No external components needed (includes loop filter, capacitors)

250 nm ASIC Design



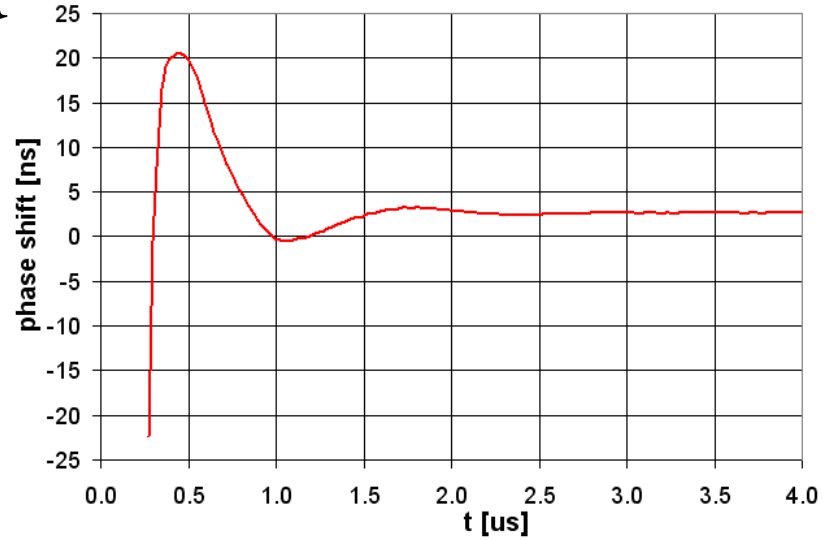


Frequency Multiplier PLL Results

Test results:

- PLL locks for 10 … 75 MHz reference frequency
- Supply current: 720 μA
- Lock time: 3 us
- Jitter < 30 ps

start up phase vs time



reference and output signal at start up