

Mu3e pixel chip “MuPix” status report for PSI user meeting

Frank Meier
Universität Heidelberg
on behalf of the Mu3e collaboration

February 8, 2016



Overview

Introduction

MuPix7

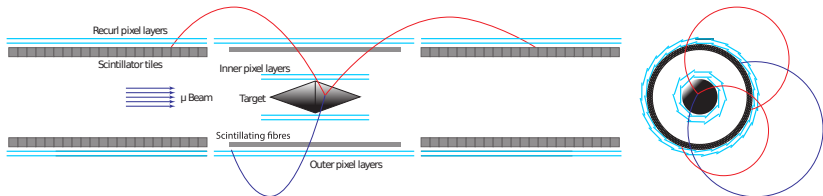
Towards MuPix8

Conclusions



Introduction

The Mu3e experiment, Phase-Ib configuration:



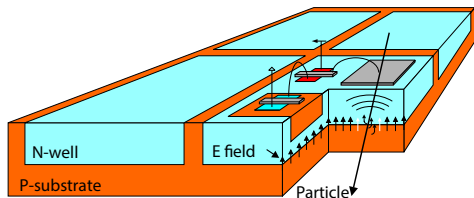
Key requirements:

- ▶ High rate: 10^8 muon stops on target per second
- ▶ Time resolution: 20 ns
- ▶ Vertex resolution: about $200 \mu\text{m}$
- ▶ Momentum resolution: about $0.5 \text{ MeV}/c^2$
- ▶ Low material budget: 1‰ X_0 per pixel layer



Introduction

We use a High-Voltage Monolithic Pixel Sensor (HV-MAPS):



- ▶ HV CMOS technology used automotive and audio industry
- ▶ Reverse biasing up to -90 V (reliable)
- ▶ Thinning to $50\ \mu\text{m}$ possible and done



Introduction

Several generations of MuPix chips realised:

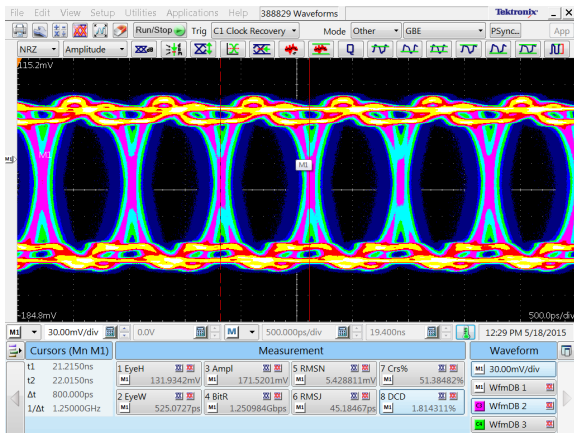
Version	Year	Main features
MuPix1/2	2011/12	Analog prototype chips
MuPix3	2013	First digital readout
MuPix4	2013	Working digital readout and time-stamping
MuPix6	2014	Readout bugs fixed, double-staged preamplifier
MuPix7	2014	Fast serial readout (1.25 Gbit/s), internal state machine, internal clock generation

MuPix3–7 have an active area of $3 \times 3 \text{ mm}^2$, chip size is $3 \times 4 \text{ mm}^2$.
MuPix7 pixel size: $103 \times 80 \mu\text{m}^2$.



MuPix7: Fast serial readout signal

Signal quality of fast readout signal at 1.25 Gbit/s is very good:

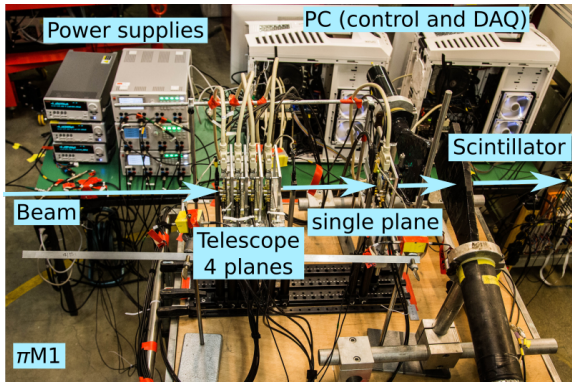


Clock is at 125 MHz, high speed clock internally generated.
Measured on test bench using chip on standard test board.



MuPix7: Telescope

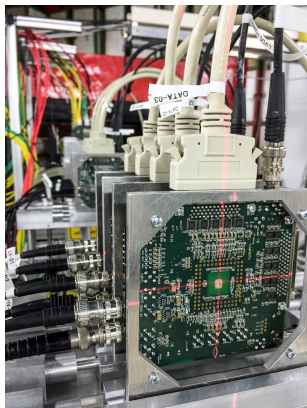
Telescope setup, e.g. at PSI π M1:



Telescope with 4 MuPix7 planes, 1 plane elected as DUT



MuPix7: Test beams



Several MuPix7 testbeam campaigns during 2015:

- ▶ Mainz MAMI, 1 GeV e^- (spring)
- ▶ CERN SPS, 180 GeV π (July)
- ▶ PSI π M1, 250 MeV π^+ , μ^+ , e^+ mix (October)
- ▶ DESY, 4 GeV e^+ (March, October)

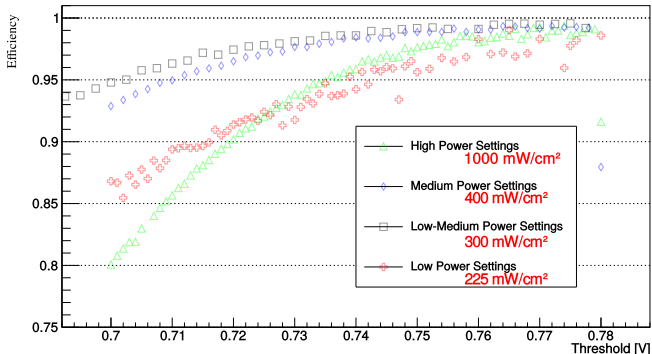
Over this course, the setup became more reliable. Boards were debugged with MuPix6 already, which helped a lot.

What follows is a selection of results from those campaigns.



MuPix7: Efficiency

Efficiencies of DUT in a telescope:



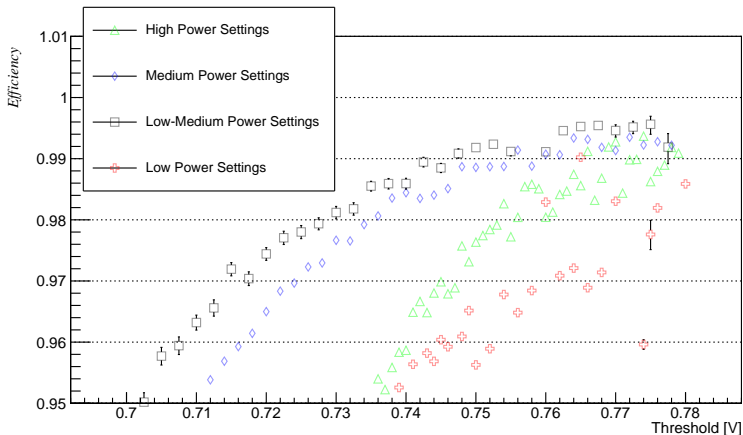
Technique: Extrapolate tracks to DUT. Comparing different power settings. Further optimisation planned.

Data taken at PSI



MuPix7: Efficiency

Efficiencies of DUT in a telescope:

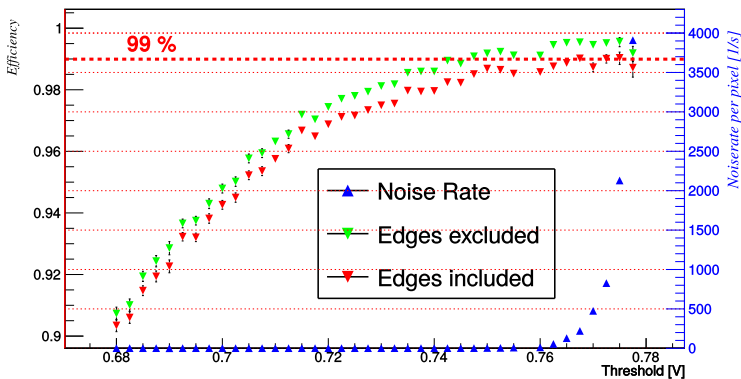


Same data, but zoomed in. Note: Hit rate is 300 kHz per chip.
Data taken at PSI



MuPix7: Efficiency

Efficiencies of DUT in a telescope:

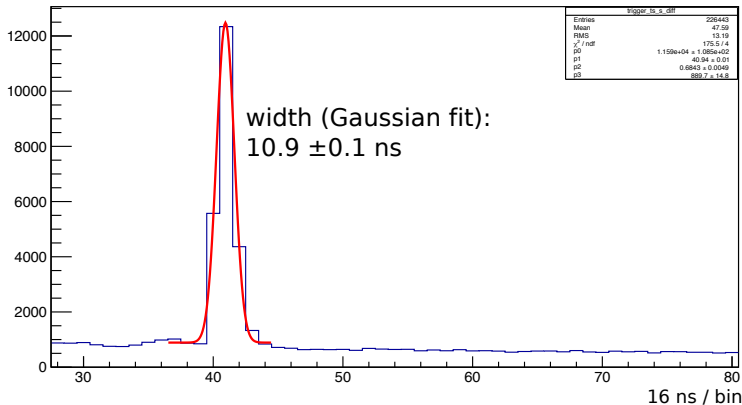


One setting (intermediate power) as example with noise rate
Data taken at PSI



MuPix7: Time resolution

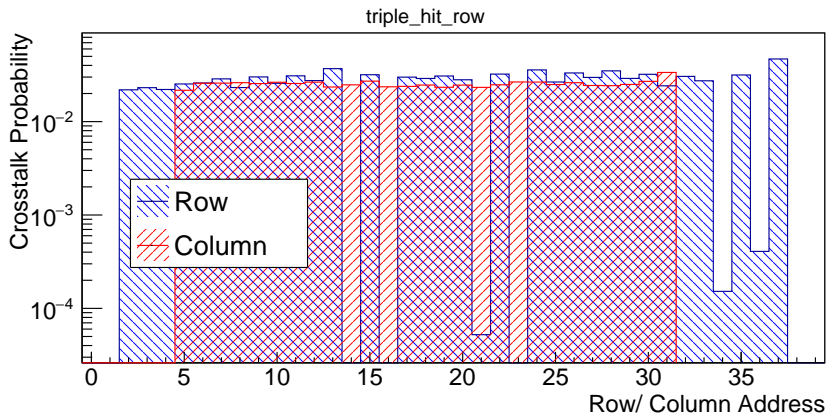
Trigger TimeStamp Difference Distribution for Single Events



Technique: Scintillator coincidence signal as reference. Plotted timestamp seen in MuPix7.



MuPix7: Crosstalk

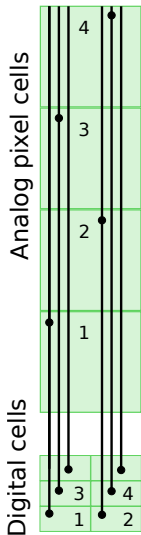


Method: Extrapolated track to DUT. Select events with 3 hits, center one matched to track. No entry: no such events found.

Do we understand the pattern?



MuPix7: Crosstalk



MuPix uses separate areas for analog and digital processing.

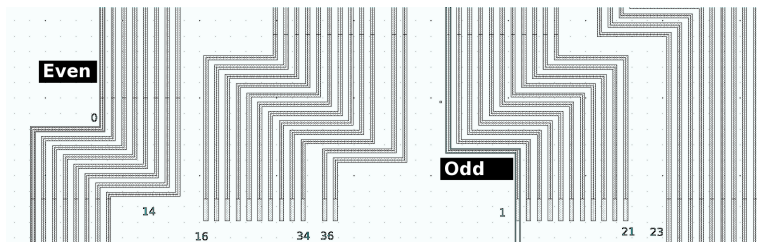
Pixel cells (sensor and preamp) are connected **point-to-point** to a corresponding digital cell (comparator, logic).

Long transmission lines can couple signals.

But still: Why the holes in the row-wise distribution?



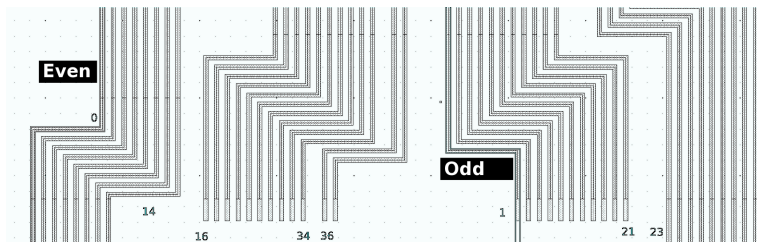
MuPix7: Crosstalk



The space distribution between lines is not uniform. Does the pattern match?



MuPix7: Crosstalk



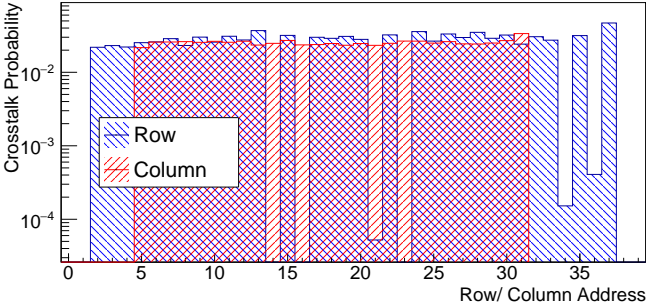
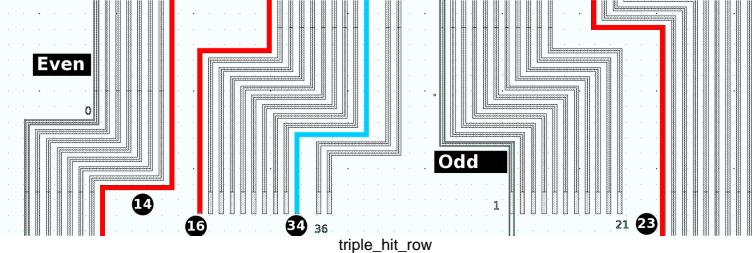
Yes. Lines of pixels 14, 16, and 23 have bigger spacing to neighboring lines, no crosstalk seen.

Column 34 has intermediate spacing, lower crosstalk.

See next slide...

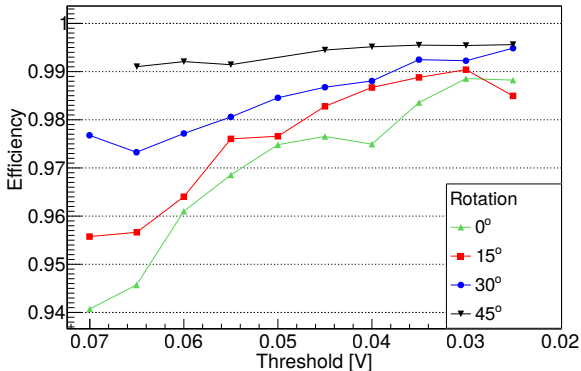


MuPix7: Crosstalk



MuPix7: efficiency of tilted sensor

Efficiencies with DUT under different angles:



Data taken at DESY



MuPix7: DAQ performance

- ▶ **CERN SPS:** MuPix7 run successfully at rates of about **500 kHz** (on chip)¹.
 - ▶ Speed limit of MuPix7 telescope: about **1 million tracks per second**. Can be increased by optimizing DMA transfer.
 - ▶ Fast data transfer and reconstruction demonstrated (simulation and at DESY).
 - ▶ Hits sorted on FPGA
 - ▶ Transferred to memory using DMA
 - ▶ Processed in GPU for track reconstruction.
- 300 MB/s** with simulated data achieved².
- ▶ **Three MuPix7 telescopes** (4 layers each) exist and proven reliable. Using own sensor and readout became a key advantage for efficient use of beamtime.

¹Exact rate determination difficult due to fluctuating bunch filling rate.

²This is processing speed, not write to disk.



Fact check:

	Specification	MuPix7	Conclusion
Pixel size (μm^2)	80×80	103×80	→ MuPix8
Sensor size (mm^2)	20×20	3×3	→ MuPix8
Thickness (μm)	50	50	ok
Bandwidth per chip (Gbit/s)	3×1.25	1×1.25	→ MuPix8
Hit rate (MHz/cm^2)	2.5	5.5	ok
Spatial resolution (μ)	< 100	$103/\sqrt{12}$	ok
Time resolution (ns)	< 20	11	ok
Efficiency (%)	> 99	99.5	ok
Signal to noise	> 20	10 ... 15	→ MuPix8 (substrate)
Power (mW/cm^2)	≤ 300	≤ 300	ok



MuPix7

In summary, with MuPix7 we could show:

- ▶ We have a **fully functional HV-MAPS chip**, $3 \times 3 \text{ mm}^2$
- ▶ **Specifications** met for key parameters that can be tested with MuPix7. MuPix8 is expected to cover the rest.
- ▶ Operation at high rates: 300 kHz at PSI π M1. We survived even higher rates of about 1 MHz at SPS.
- ▶ **Crosstalk** on setup under control, on chip seen. Mitigation plan exists (see MuPix8, later slides).
- ▶ We routinely operate systems of up to 8 chips in testbeams reliably.
- ▶ Data processing of one telescope (4 chips) at full rate on GPU demonstrated.



Towards MuPix8

Goals:

- ▶ **Scaling-up** from $3 \times 3 \text{ mm}^2$ to $13 \times 20, \text{ mm}^2$ (active area)
- ▶ All **pads on one edge** (required for integration studies)
- ▶ **Submission** deadline: June 2016 (not earlier due to foundry capabilities)
- ▶ First chip suitable for **integration studies**
- ▶ Options for mitigating **crosstalk**:
 - ▶ Adjust amplifier to optimize amplitude for strong signals
 - ▶ Place ground lines between signal lines
 - ▶ Switch from voltage to current signalling

Chip designers are **confident** that space is sufficient to solve these issues. Next months will show.

- ▶ Foundry (AMS) provides **higher-resistivity substrate** ($20 \Omega\text{cm} \rightarrow 80 \Omega\text{cm}$). Will be explored with MuPix8 for the first time.



Towards MuPix8

Integration studies:

- ▶ Build a **prototype of an inner layer module**: 2×3 chips.
- ▶ Studies with different **flex print options** (1 signal layer, 2 power layers):
 - ▶ **Traditional**: 3 layer copper: conservative but reliable, too much material for final design ($2\% X_0$)
⇒ Electrical integration studies



Towards MuPix8

Integration studies:

- ▶ Build a **prototype of an inner layer module**: 2×3 chips.
- ▶ Studies with different **flex print options** (1 signal layer, 2 power layers):
 - ▶ **Traditional**: 3 layer copper: conservative but reliable, too much material for final design ($2\% X_0$)
⇒ Electrical integration studies
 - ▶ **Baseline**: 1 copper layer (signal), 2 aluminium layers (power/GND), sandwiched ($1.2\% X_0$ possible)
⇒ Copper technology has nice spacing ($10 \mu\text{m}$ feature sizes available)



Towards MuPix8

Integration studies:

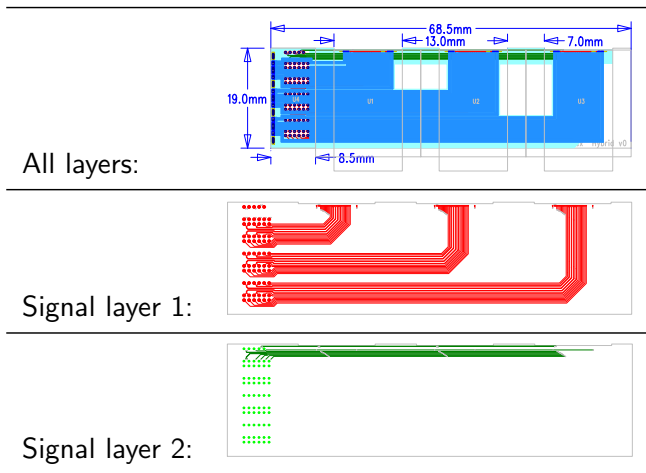
- ▶ Build a **prototype of an inner layer module**: 2×3 chips.
- ▶ Studies with different **flex print options** (1 signal layer, 2 power layers):
 - ▶ **Traditional**: 3 layer copper: conservative but reliable, too much material for final design ($2\% X_0$)
⇒ Electrical integration studies
 - ▶ **Baseline**: 1 copper layer (signal), 2 aluminium layers (power/GND), sandwiched ($1.2\% X_0$ possible)
⇒ Copper technology has nice spacing ($10 \mu\text{m}$ feature sizes available)
 - ▶ **Optimal**: 2 layer Aluminium, if necessary with one additional layer. Uses pad-bonding ($1\% X_0$)
⇒ Technology implemented by ALICE. Riskier approach, new territory but promising.

See next page for an example layout.



Towards MuPix8

This is an example design for the two options using Cu layers:



Layer 1: point-to-point signals, layer 2: bus-type signals



Conclusions

- ▶ MuPix shows a clear path of incremental improvements over time
- ▶ MuPix7 is a fully functional HV-MAPS chip showing performance to spec
- ▶ MuPix8 will tackle up-scaling in size and data-rate per chip
- ▶ First integration tests will be possible with MuPix8, effort started

(Almost) no results would have been possible without the great support at all testbeam facilities (CERN, DESY³, MAMI, PSI).

We gratefully acknowledge the beamtime we received.



³a member of the Helmholtz Association (HGF)

BACKUP



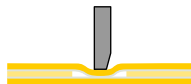
Al flexprint

Layer-to-layer or Layer-to-chip bonding:

Via:



Stack of Al coated polyimide with spacer



Ultrasonic wedge bonding



PI: Polyimide

Bond finished

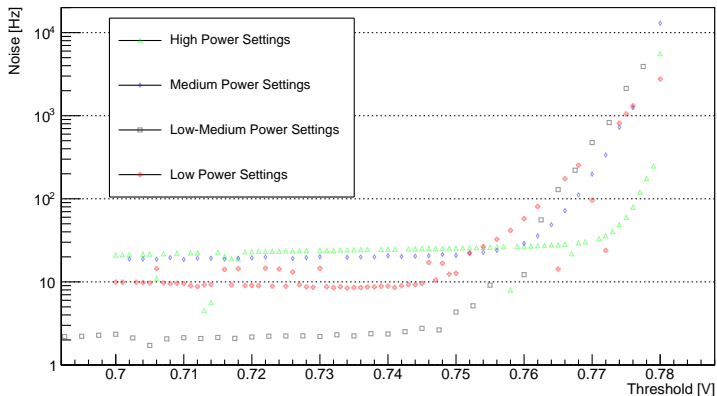
Bond to chip:



(Note: there is a small dip)



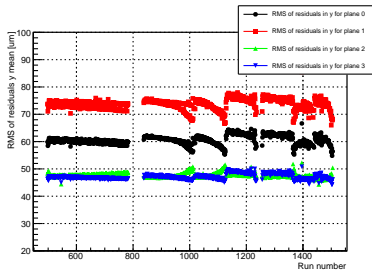
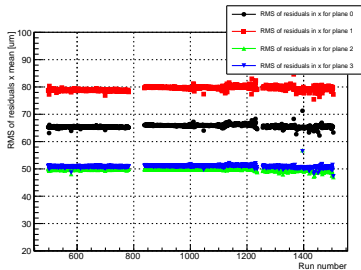
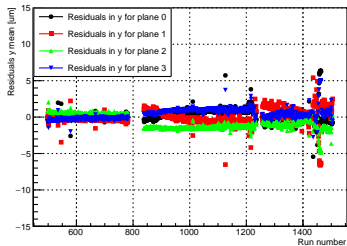
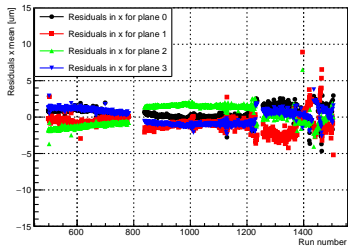
Noise per power setting



Same measurement as shown for efficiencies, noise shown here.



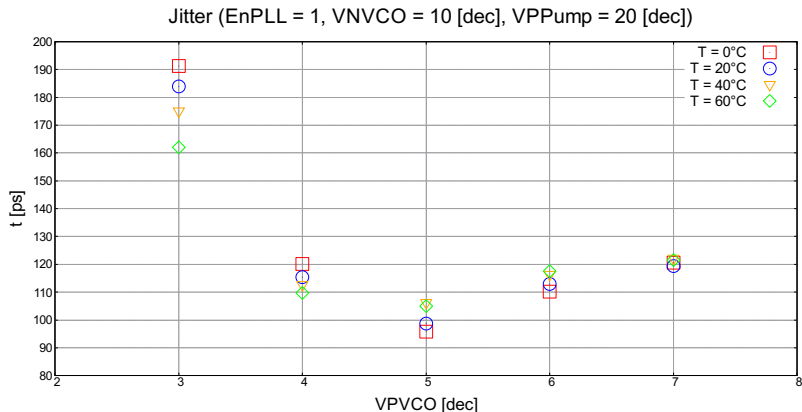
Telescope alignment



Data taken at DESY.



Jitter temperature dependence



Measured in a temperature chamber. Work in progress.

