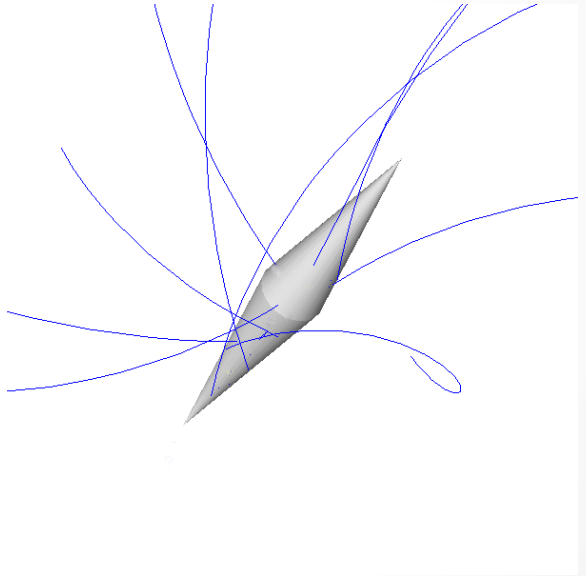
The trigger-less readout for the Mu3e experiment

Dirk Wiedner

On behalf of the Mu3e collaboration

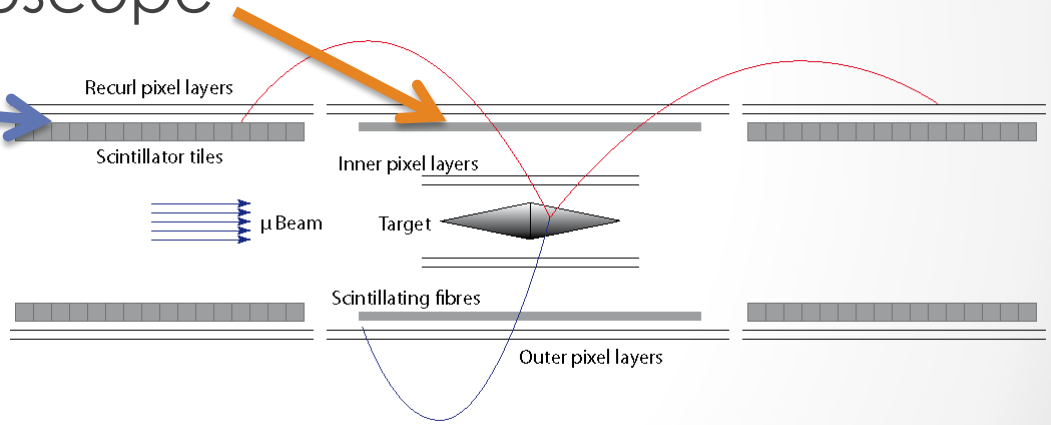
Readout Requirements

- 100 MHz muon decays
- 50 ns readout frames (pixel)
- O(5000) pixel chips
- O(7000) scintillating fibers
- O(7000) timing tiles
- **Online filtering**



Timing Detectors

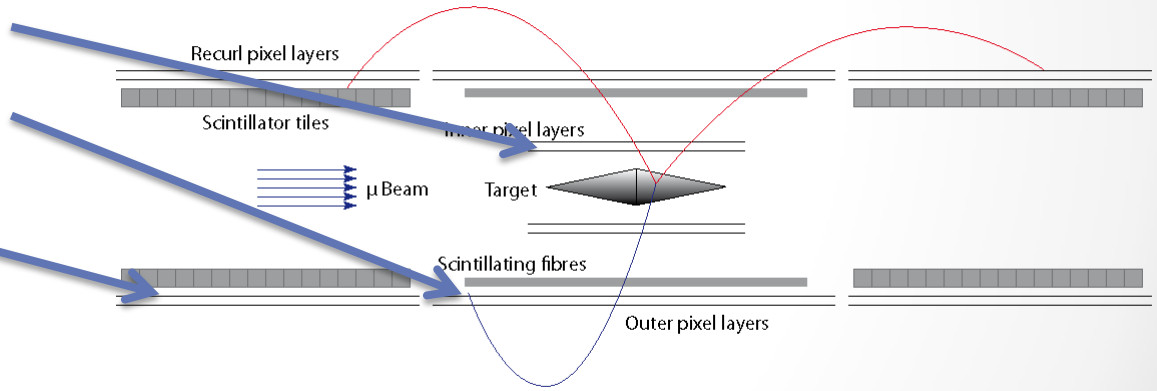
- Scintillating fiber hodoscope
- Timing tiles
- On detector zero-suppression



O(7000) fibers
O(7000) tiles

Silicon Pixel Detector

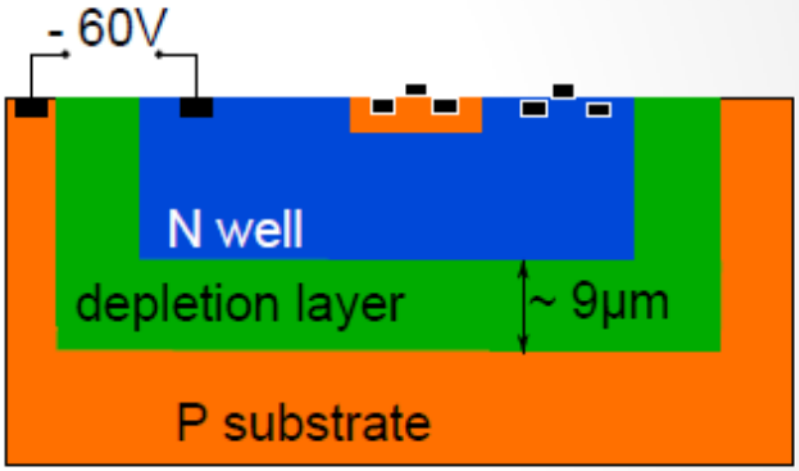
- Inner double layer
- Outer double layer
- Re-curl layers
  - Both sides (x2)
- Sensor size
  - 2x2 cm^2



108 inner sensors
4680 outer sensors

HV-MAPS

- **H**igh **V**oltage **M**onolithic **A**ctive **P**ixel **S**ensors
- HV-CMOS technology
- Reversely biased -85V
  - Charge collection via drift
    - ➢ Fast O(1 ns)
  - Thinning to 50 µm



by Ivan Peric

I. Peric, A novel monolithic pixelated particle detector implemented in high-voltage CMOS technology Nucl.Instrum.Meth., 2007, A582, 876

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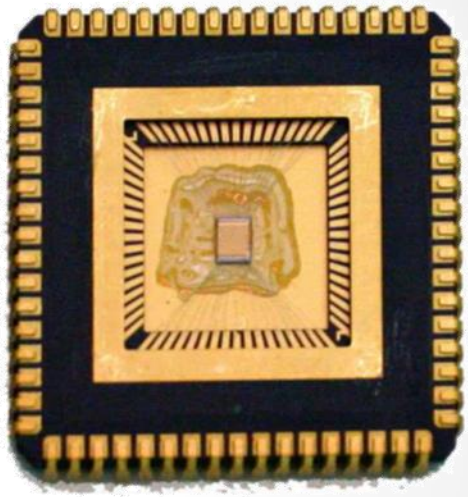

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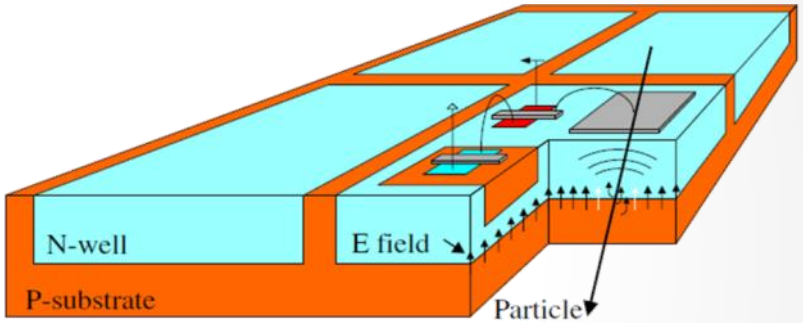
- **Integrated readout electronics**
  - **Zero suppression**
  - **1.25Gbit/s serial LVDS outputs**



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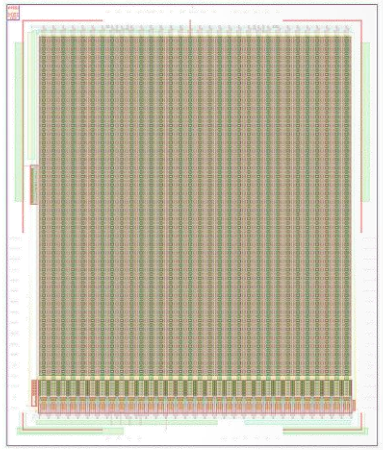

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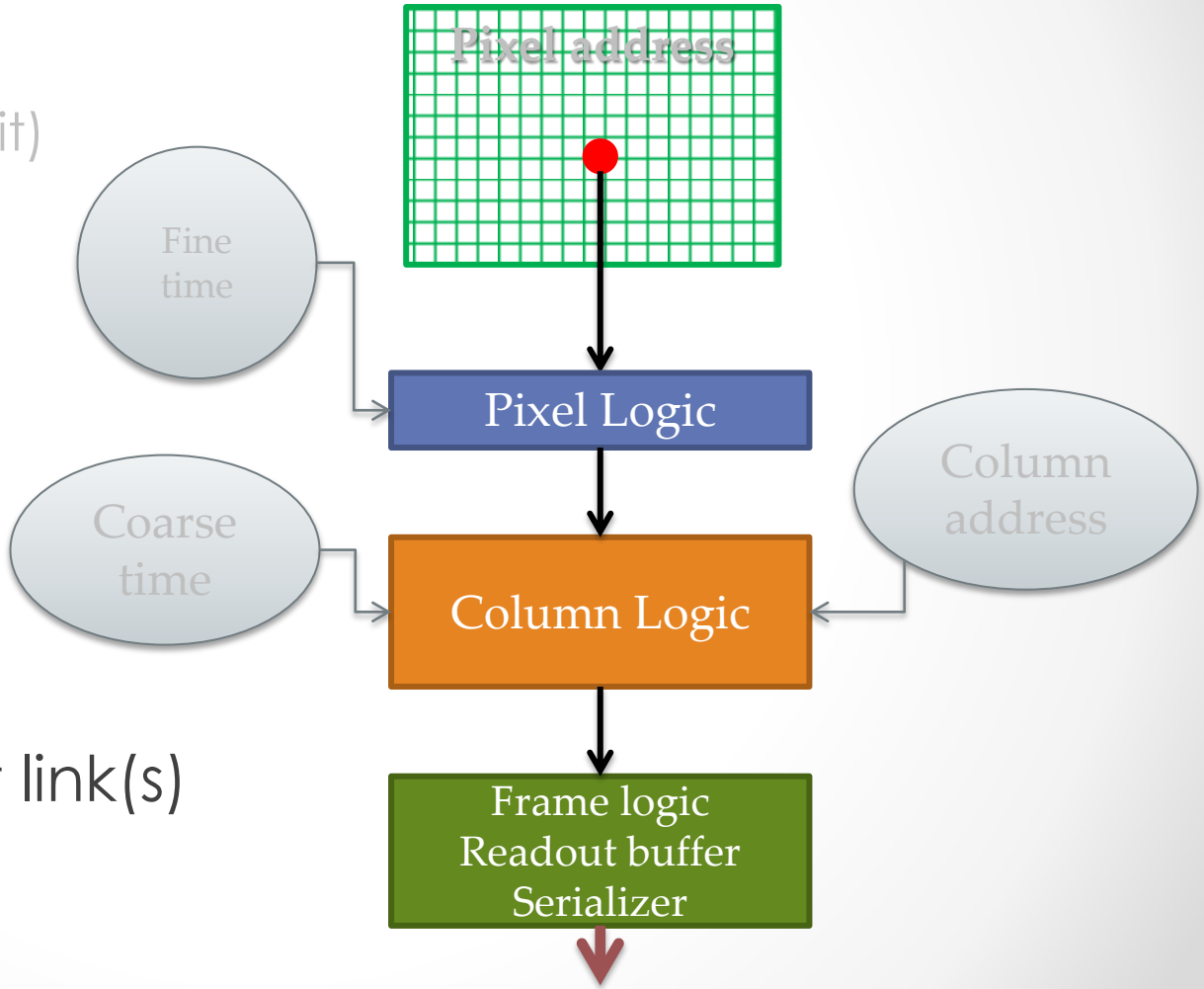
Pixel Readout Scheme

Pixel Readout Scheme

- Pixel logic
  - Pixel address (8 bit)
  - Fine time (8 bit)
  - 50 ns frames
- Column logic
  - Pixel data
  - Column address
  - Coarse time
- Readout buffer
- Serializer and fast link(s)



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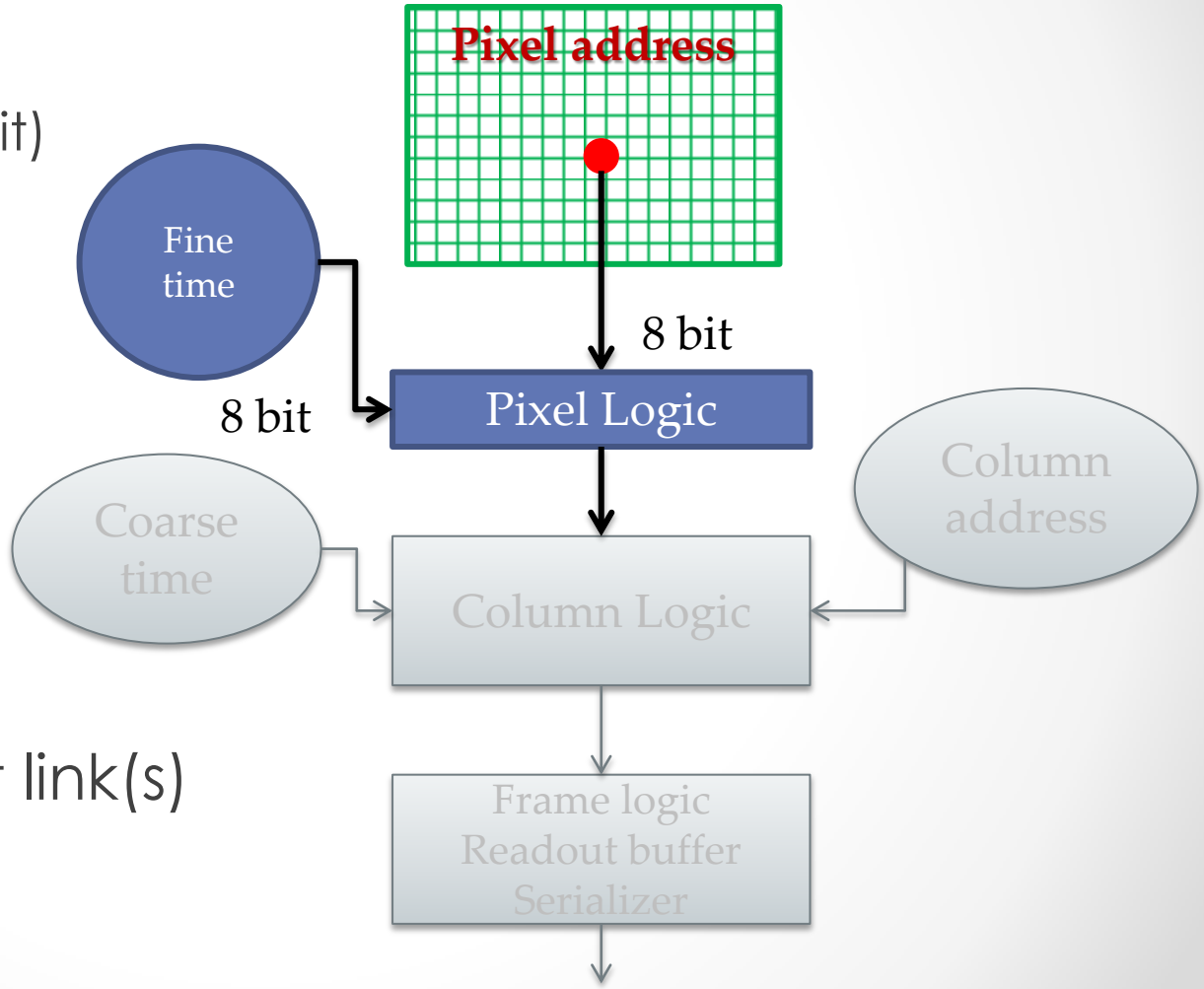

Pixel Readout Scheme

- Pixel logic
  - Pixel address (8 bit)
  - Frame number (4 bit)
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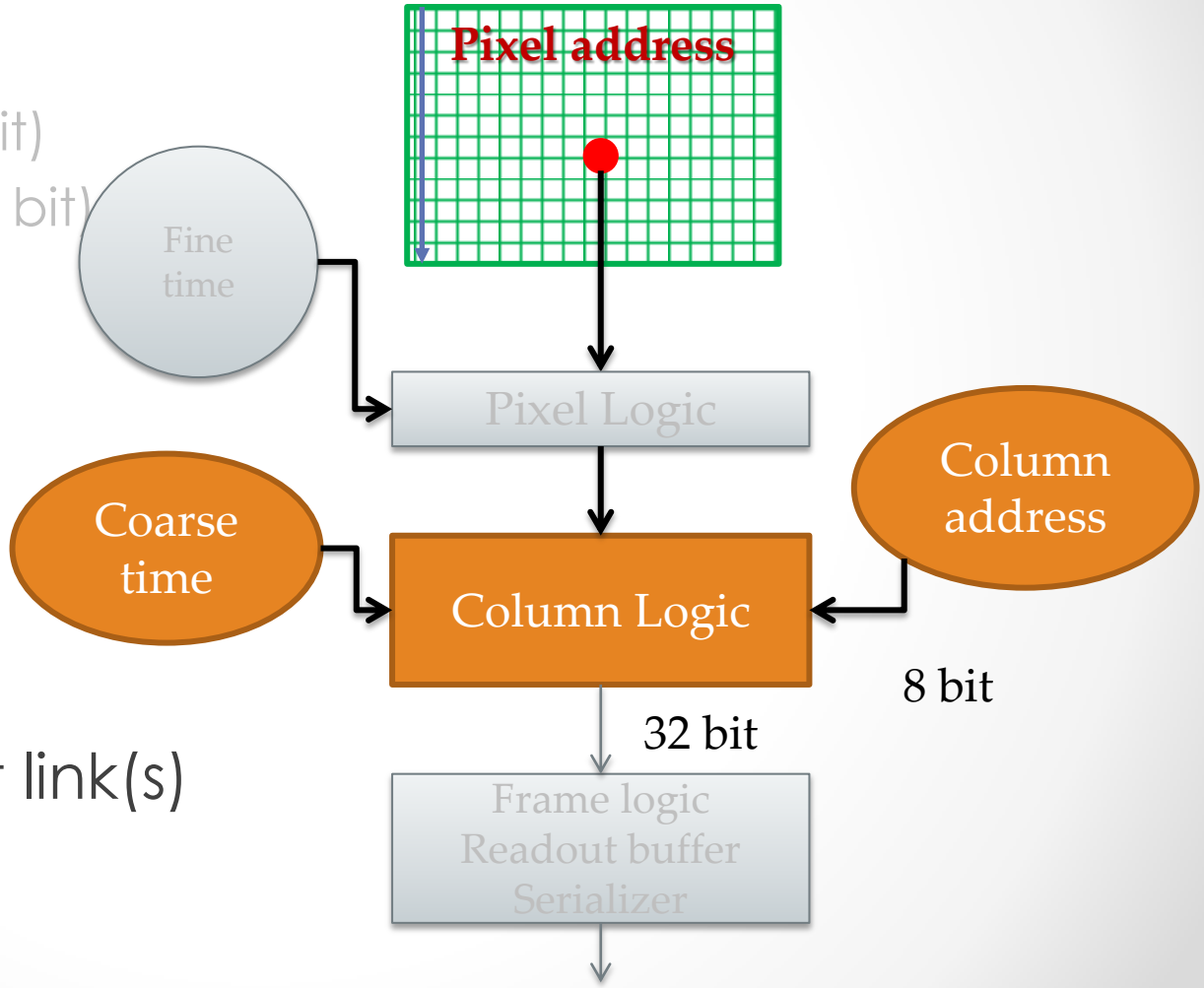

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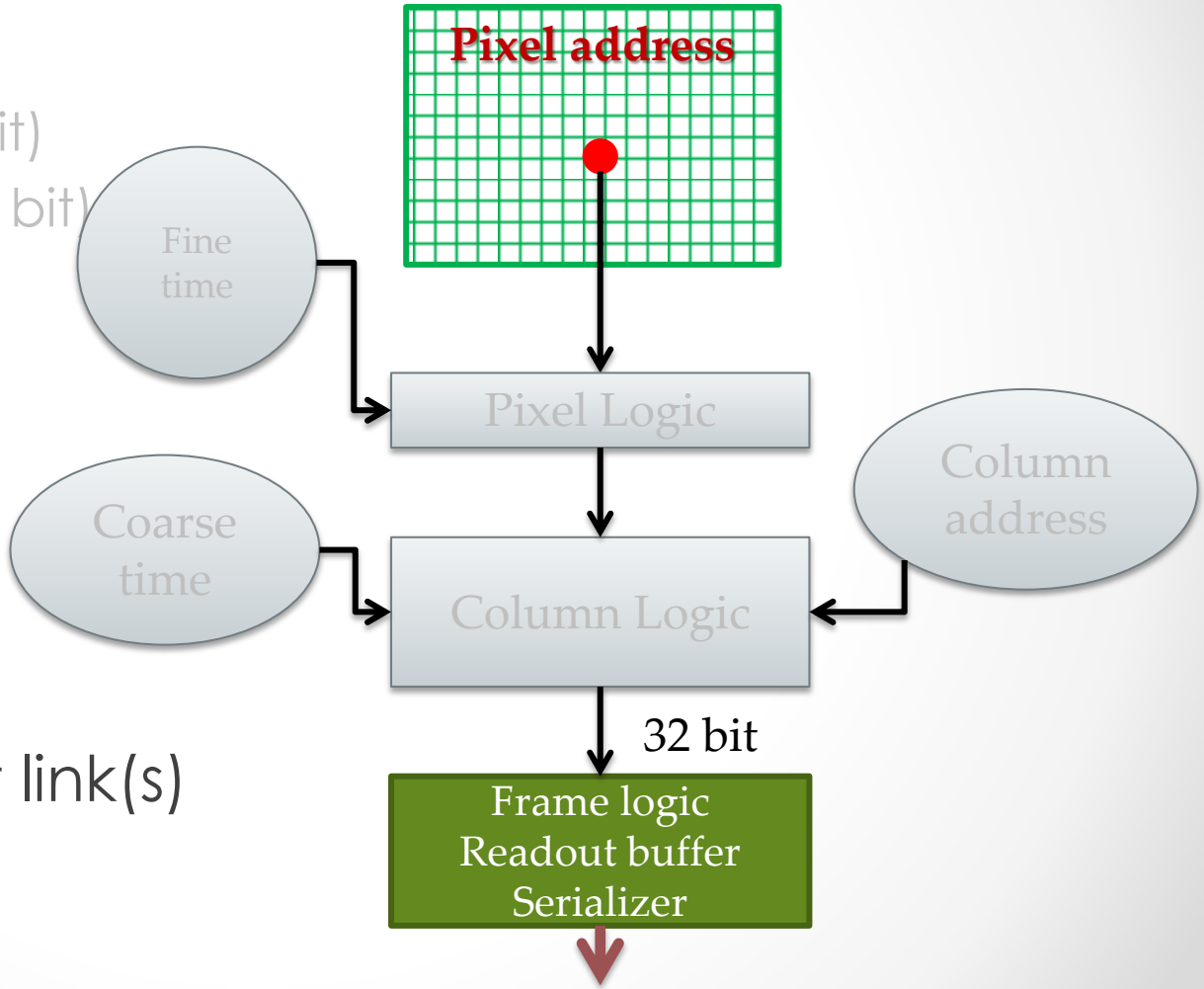
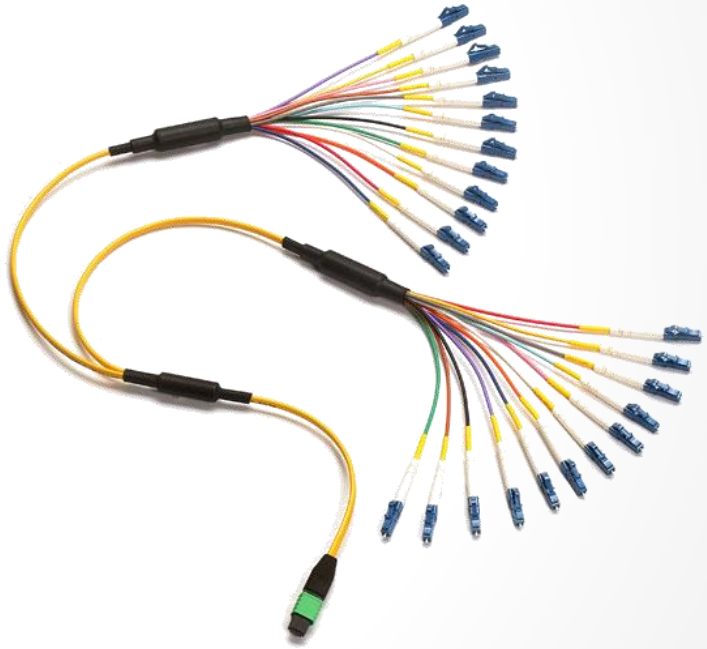


Data Link Scheme

From detector slices
to time slices

Link Overview

- Front end links
  - Pixel sensor to on-detector FPGA
    - 1.25bit/s
    - LVDS
  - Timing detector readout
- Optical links from detector
  - Front end FPGAs
  - … to readout boards
  - 5 Gbit/s
- Optical links in counting room
  - Off-detector read out boards
  - …to PC Farm



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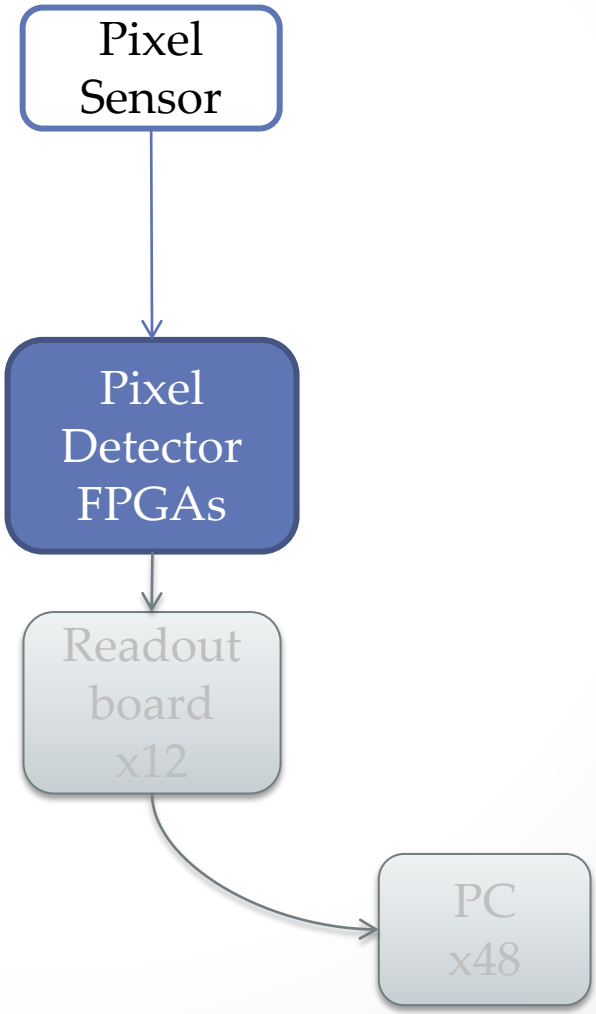

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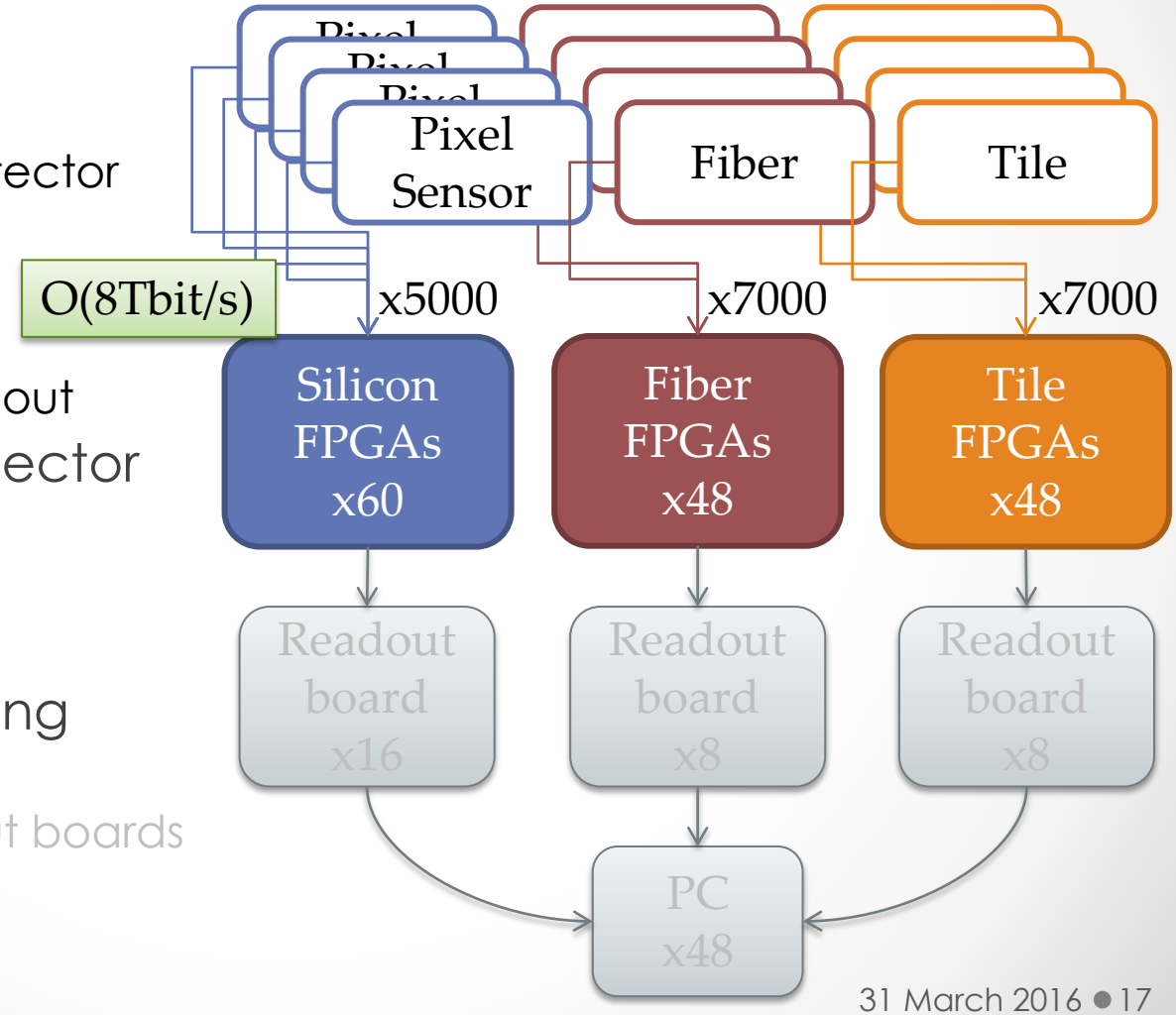

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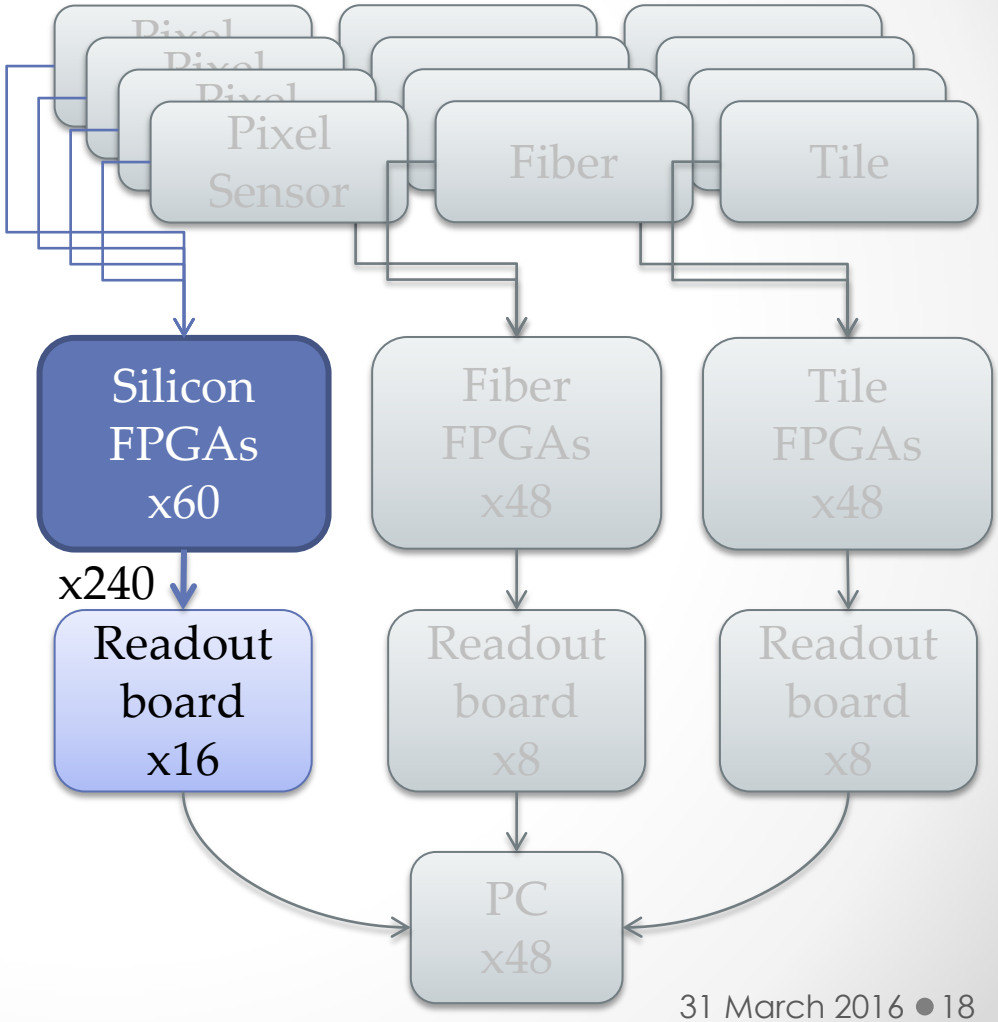

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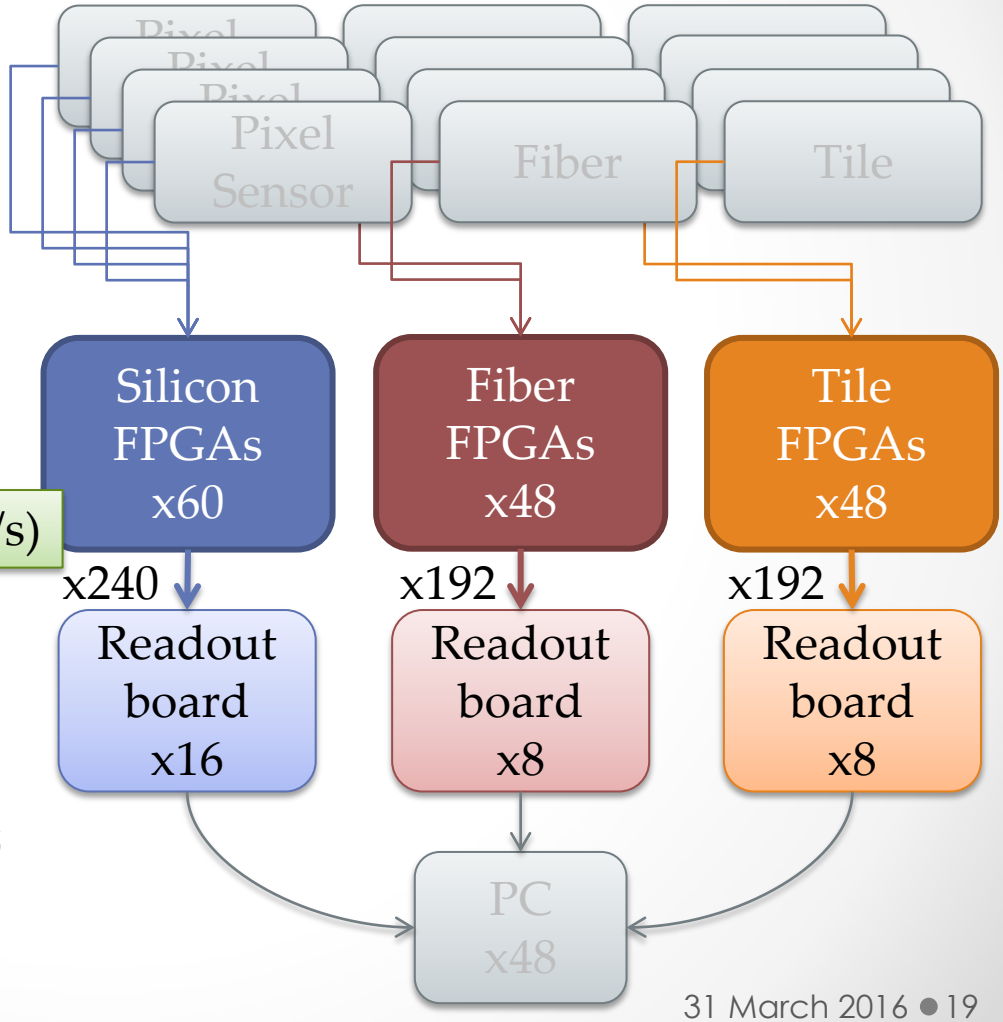

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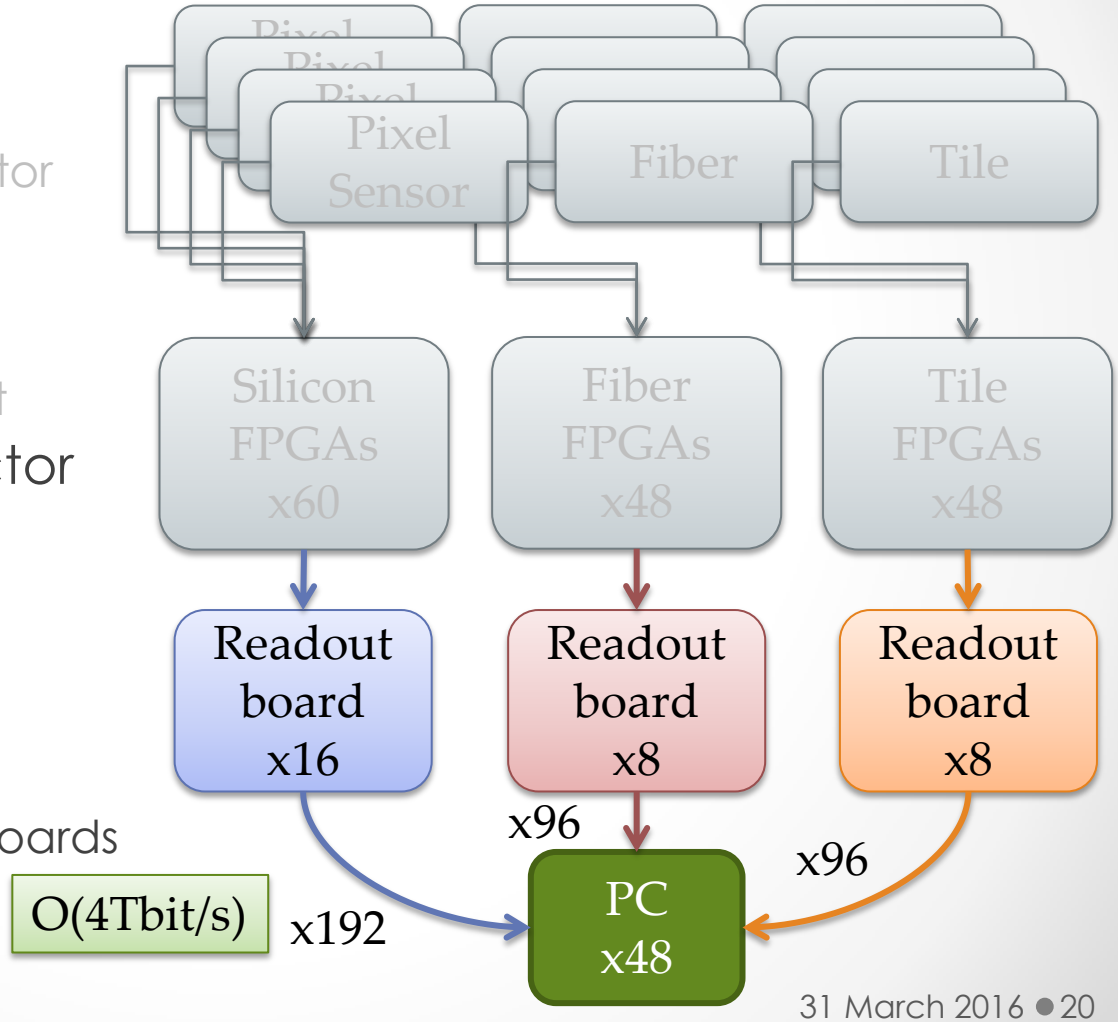
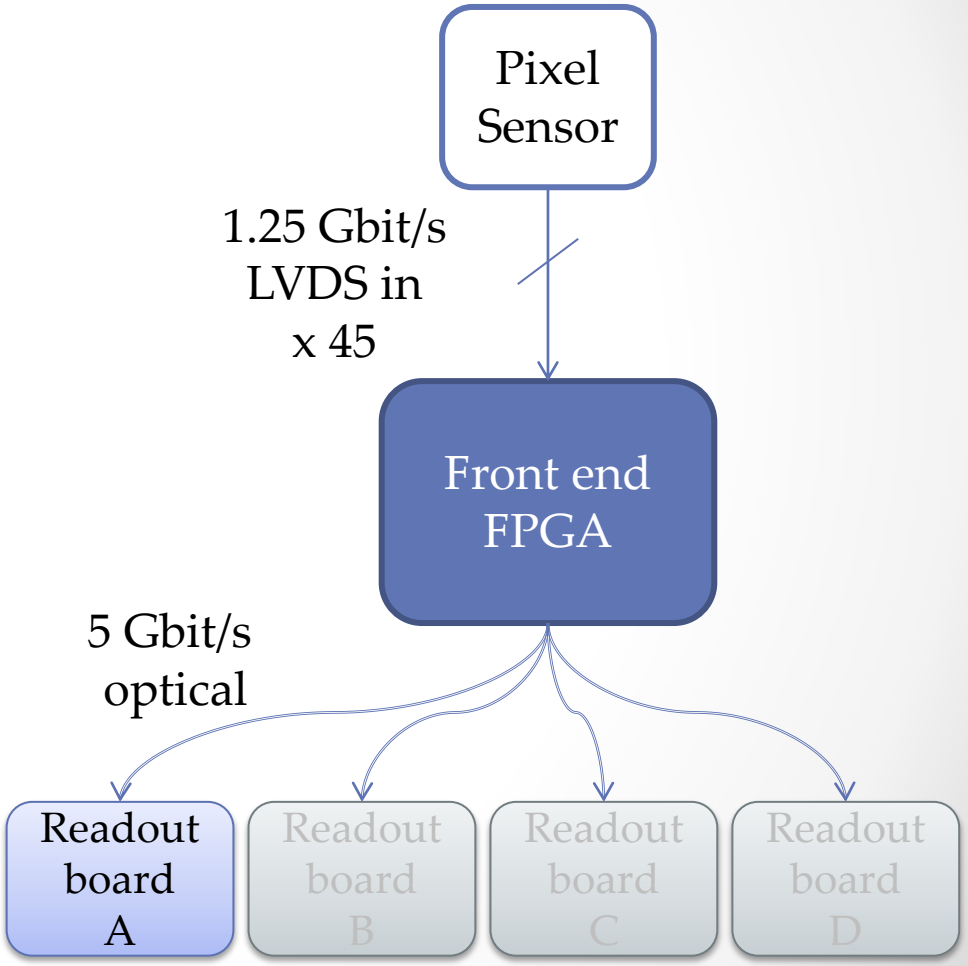


Front End FPGAs

- FPGAs on detector
  - 60 (+96) pieces
- Receive sensor data
  - 45 LVDS inputs
- 5 Gbit/s outputs
  - 8 optical links
  - … to counting house
- Switching data between readout boards farms A-D



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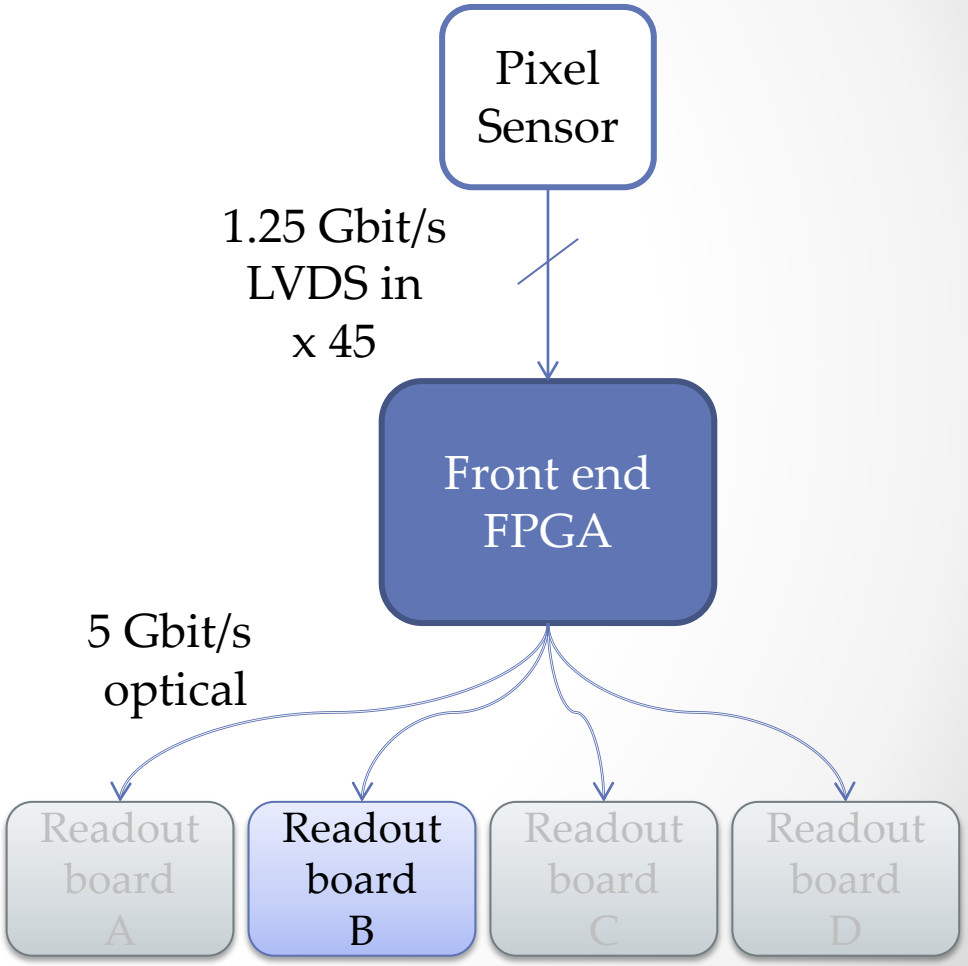

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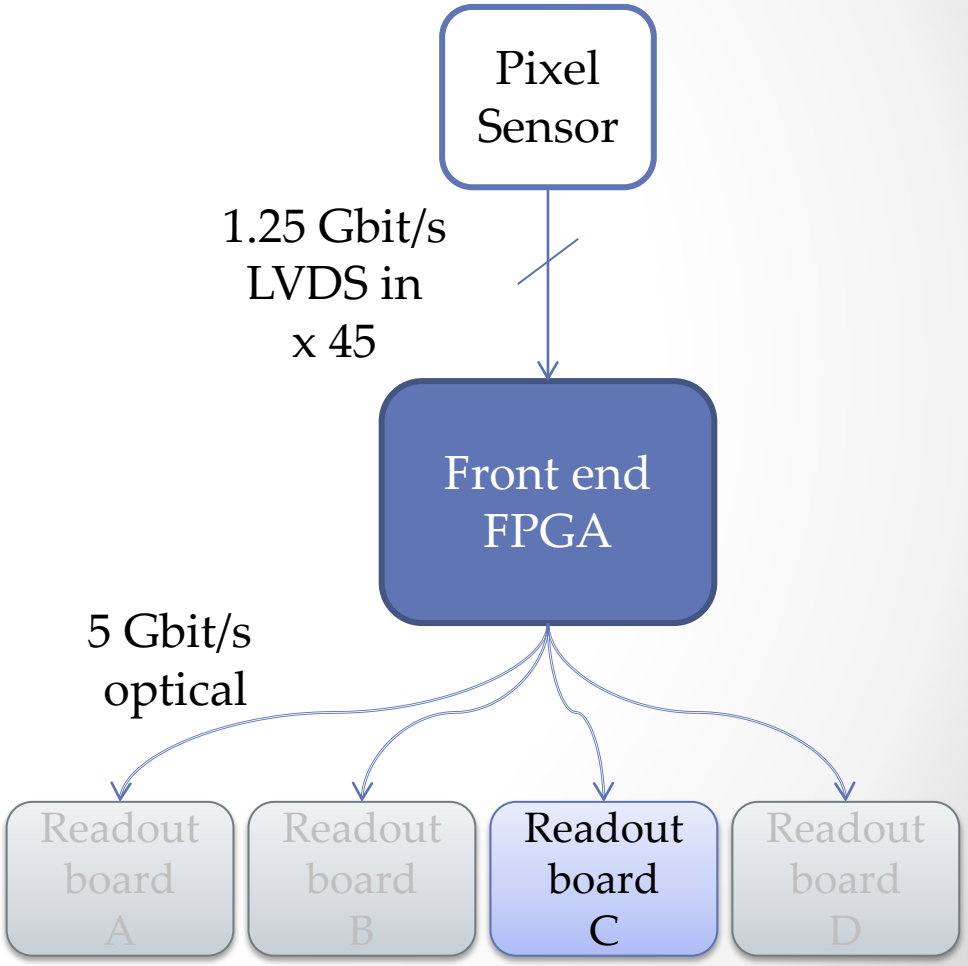

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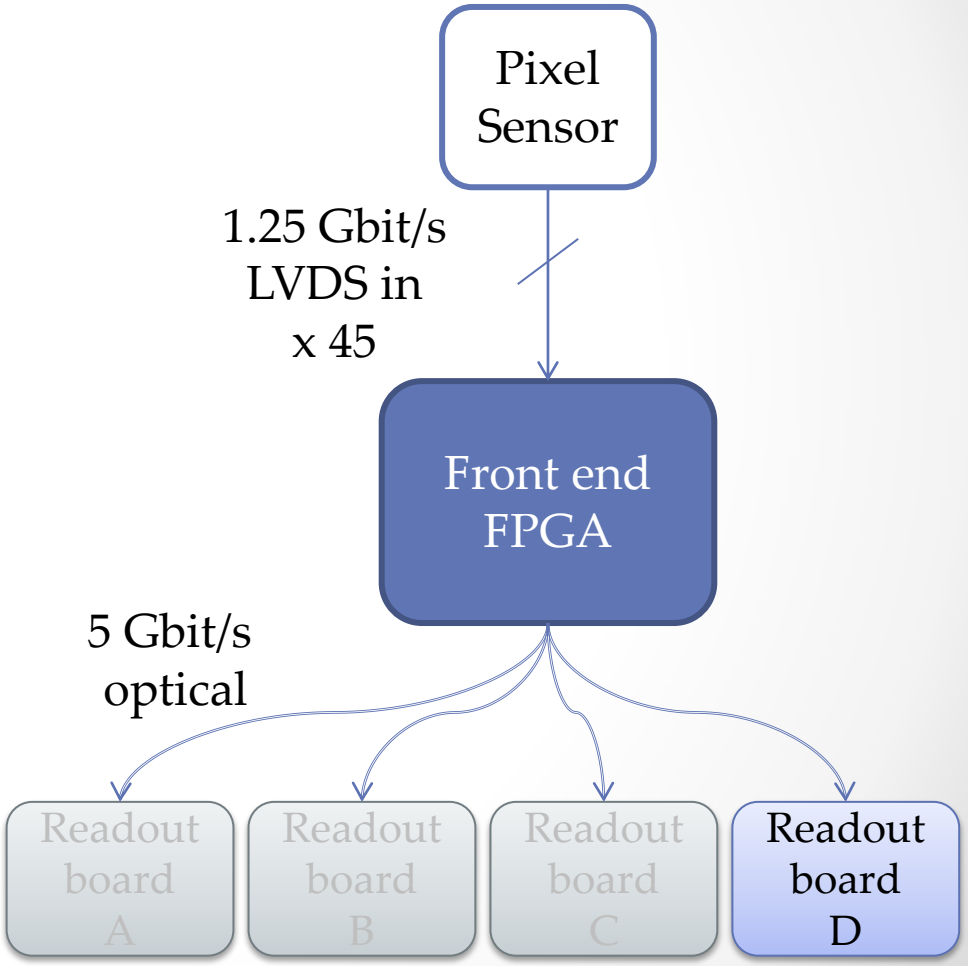
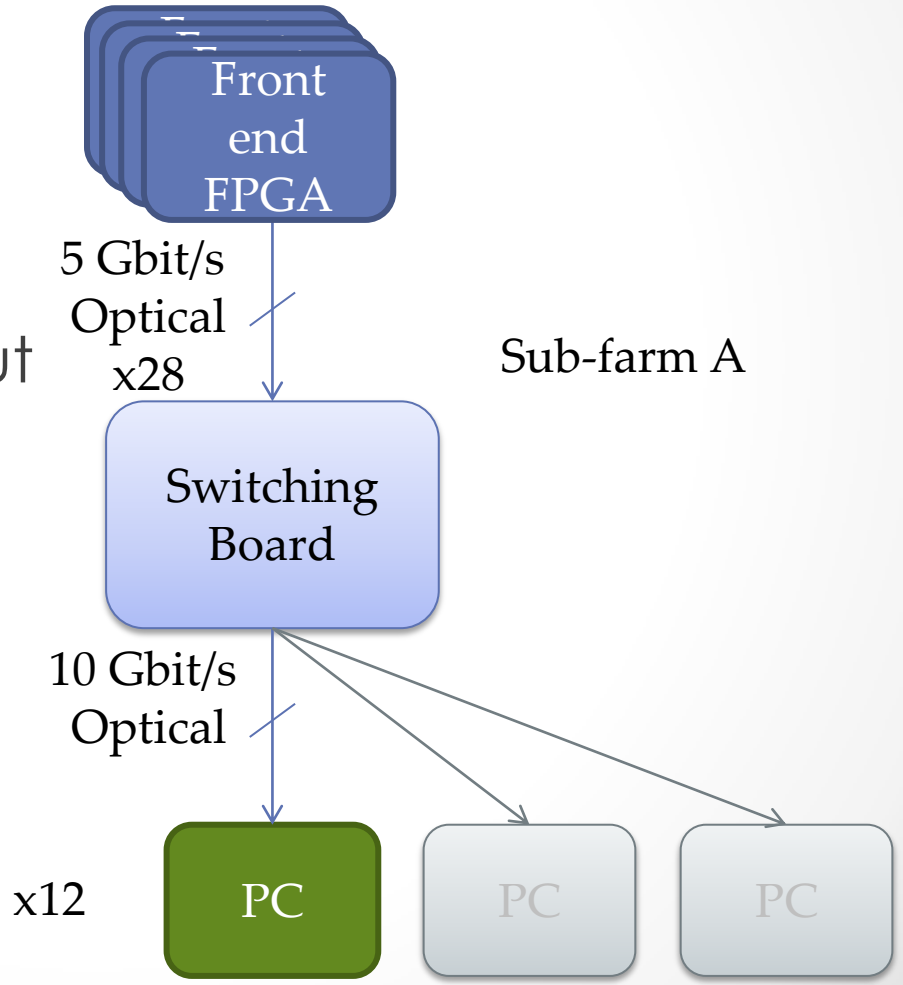


Switching Board

- FPGA readout boards
  - 4 per sub-detector
- 5 Gbit/s optical inputs
  - 48 inputs
- 10 Gbit/s optical output
  - 12 outputs to PCs
- Switching network
  - A-D sub-farms
  - One output per PC



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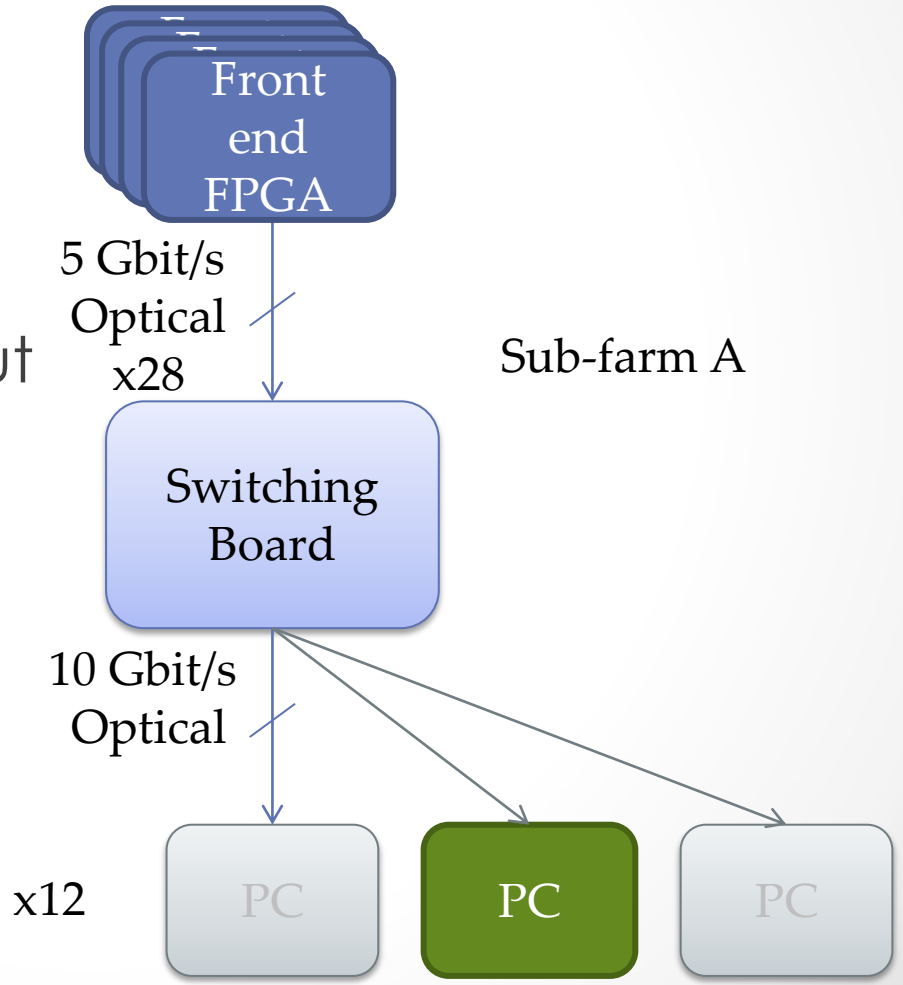
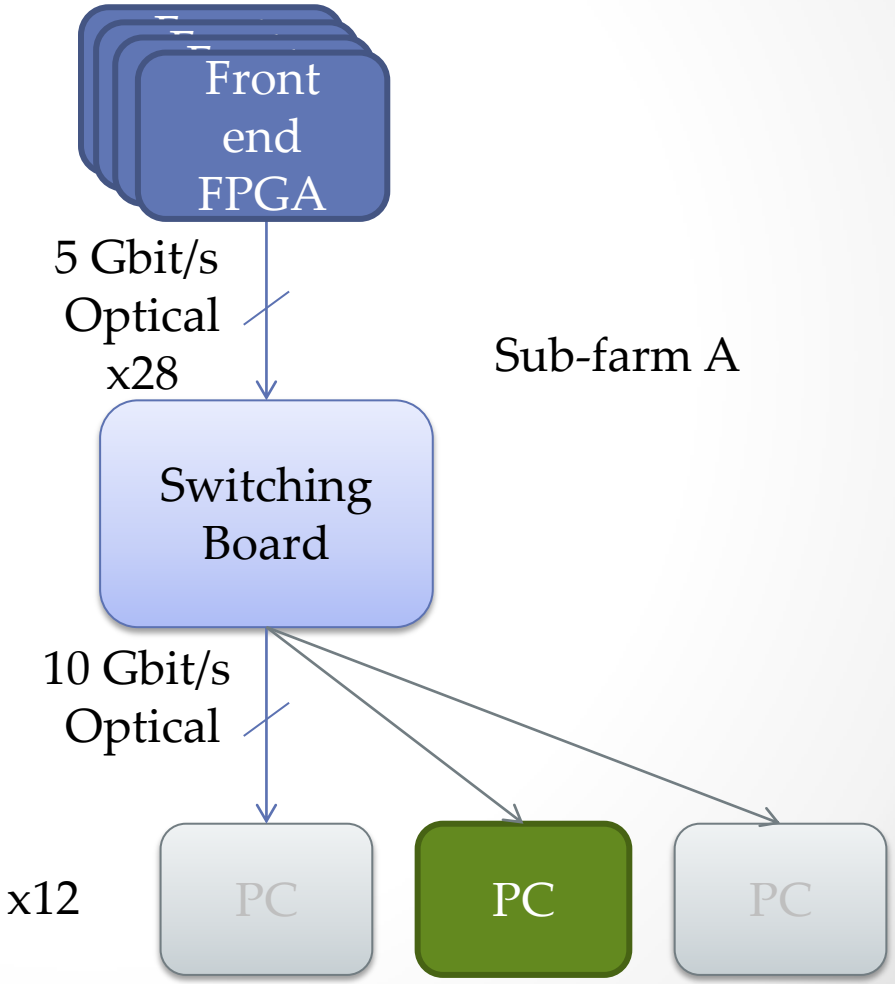


Switching Board

LHCb PCIe40 PCB

- Marseille
- First prototypes available



GPU-PC

- PC with GPU
- 10 Gbit/s Fiber input
  - 8 inputs from sub-detectors
- Data filtering
  - Timing Filter on FPGA
  - Track filter on GPU
  - Data to tape < 100 MB/s

Optical mezzanine connectors

FPGA PCIe board

GPU computer

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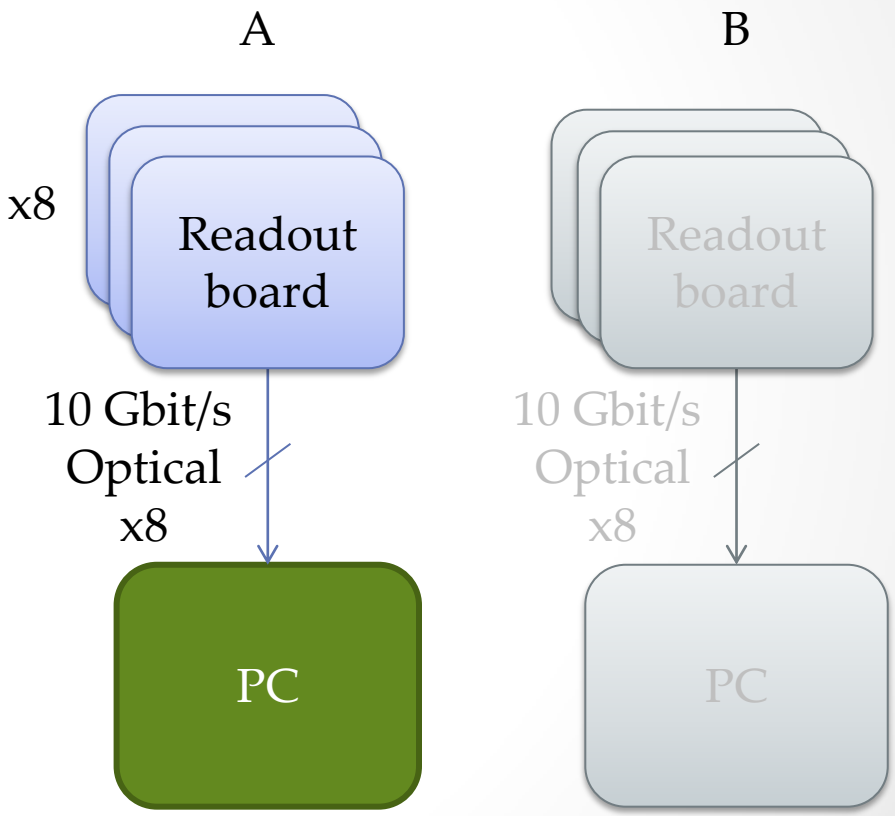
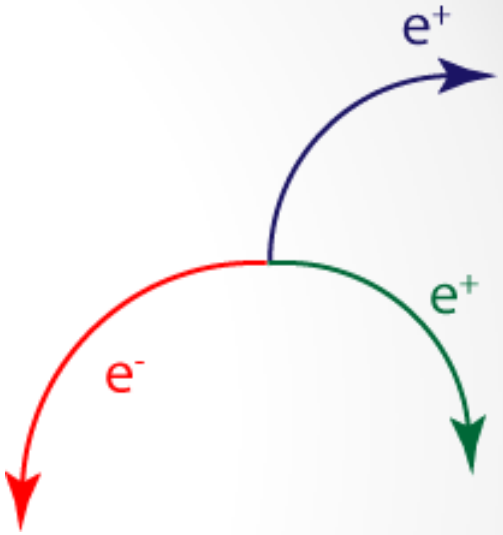
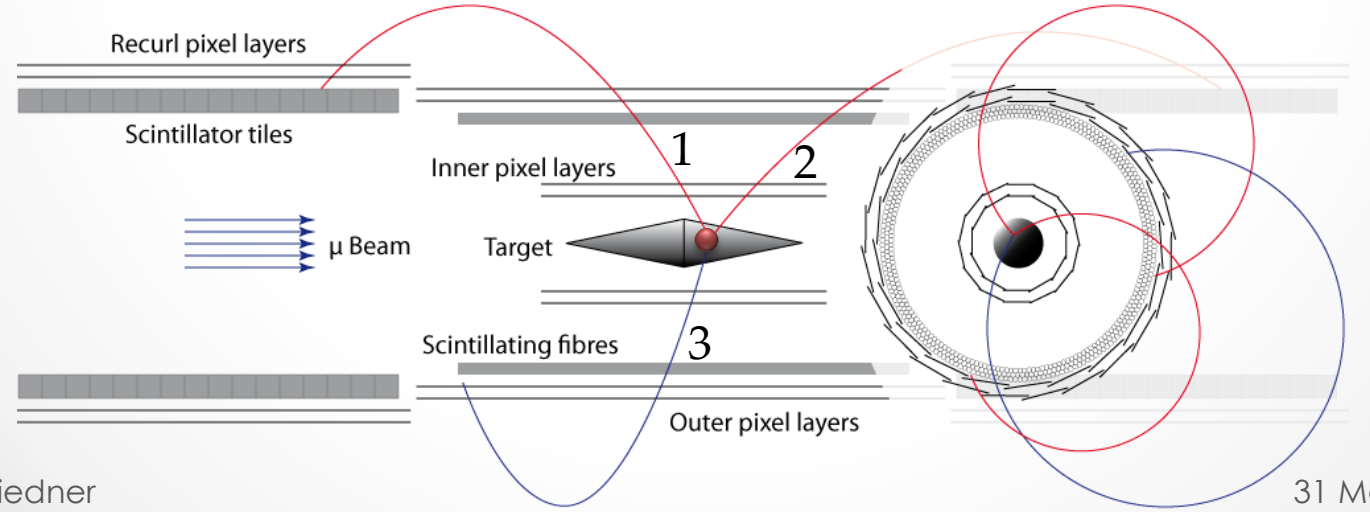


Vertex Filter

- Entire event on GPU
- Large target
  - Large spread of muons
  - Easy vertex separation
- Reject data without three tracks
  - … inside area interval on target





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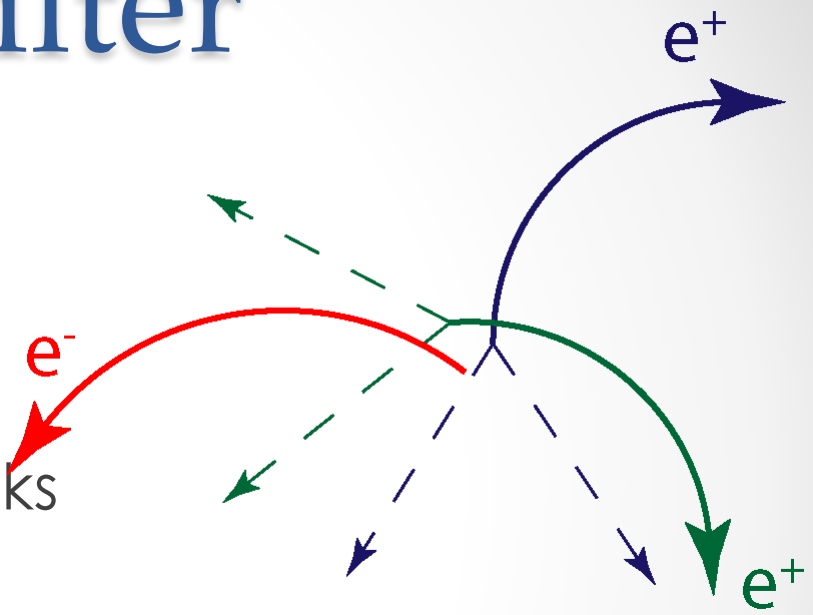
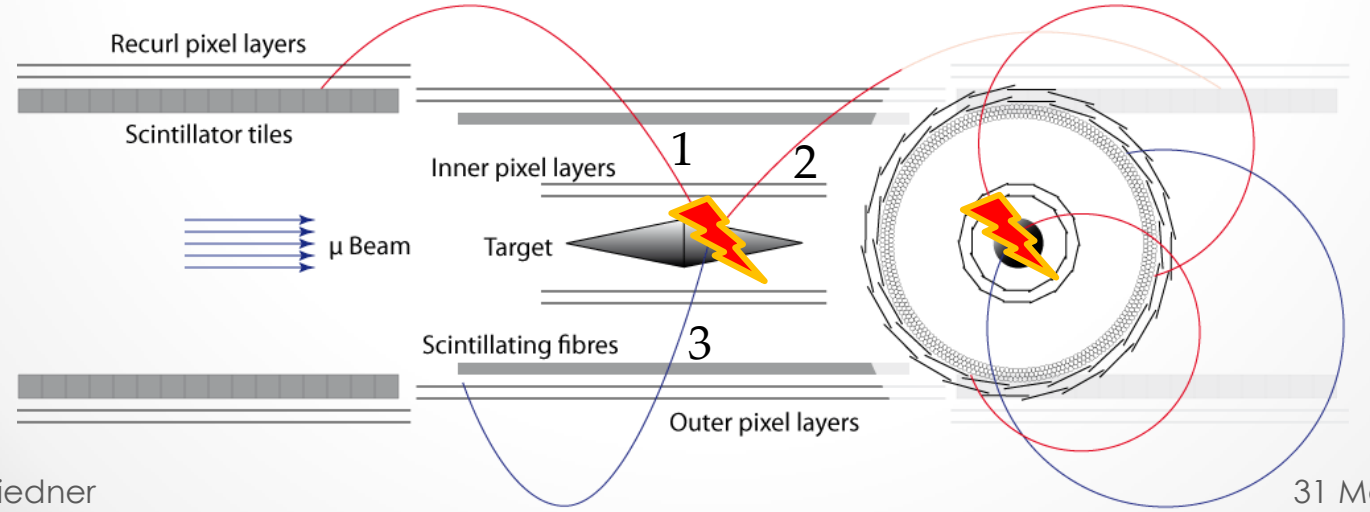
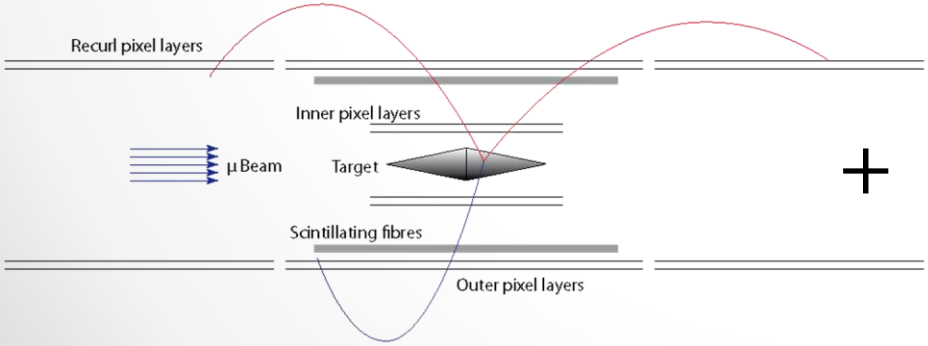




Summary

- Mu3e has 300M pixels @ 10^8 muons/s
- 1 Tbit/s data
- 0-suppressed serial data from active pixel sensors
- Switched optical network
- GPU filter farm with optical inputs



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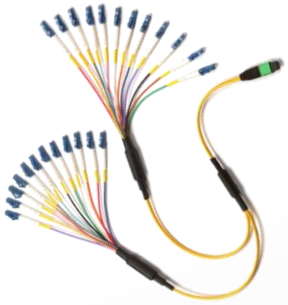

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