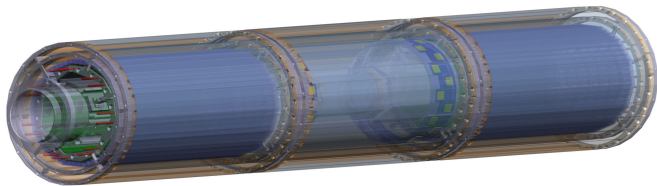


The Mu3e Pixel Tracker

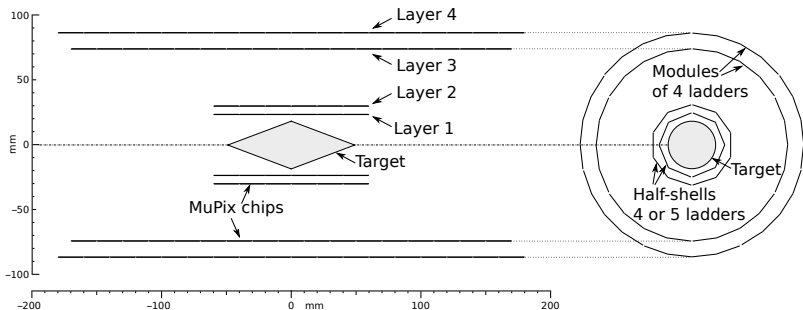
Frank Meier
Universität Heidelberg
on behalf of the pixel team

Februar 6, 2017



Pixel tracker design essentials

Geometry of central tracker:

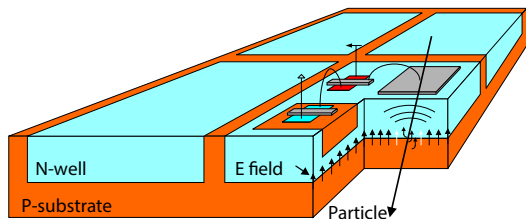


Recoil stations are copies of layer 3/4, extending in z.



Pixel tracker design essentials

The basic building block: MUPIX chip.



HV-CMOS

Thinned to $50\ \mu\text{m}$

Active chip
area $20 \times 20\ \text{mm}^2$

Ivan Perić, Nucl.Instrum.Meth. A582 (2007)
876-885

NB: Sensor performance follows later in this talk.



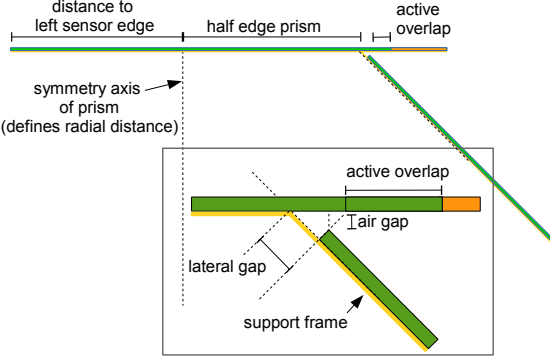
Pixel tracker design essentials

While using the same sensor chip, inner layers and outer layers differ:

- ▶ Inner layer:
 - ▶ 12 cm long (6 chips)
 - ▶ Two layers, two half shells
 - ▶ Half shells form one rigid unit
 - ▶ We call one half layer a module
- ▶ Outer layer:
 - ▶ 34/36 cm long (17/18 chips)
 - ▶ Two layers, made with modules of 4 ladders
 - ▶ Layer 3 has 6 modules, layer 4 has 7 modules
 - ▶ Modules installed individually, removable by design



Pixel inner layer

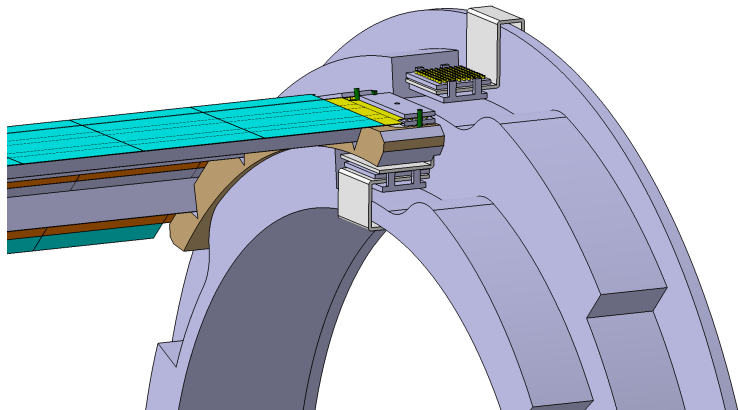


Chips/HDI assembly (green) on polyimide support frame (yellow).

Observe overlap for enhanced hermeticity.



Pixel outer layer

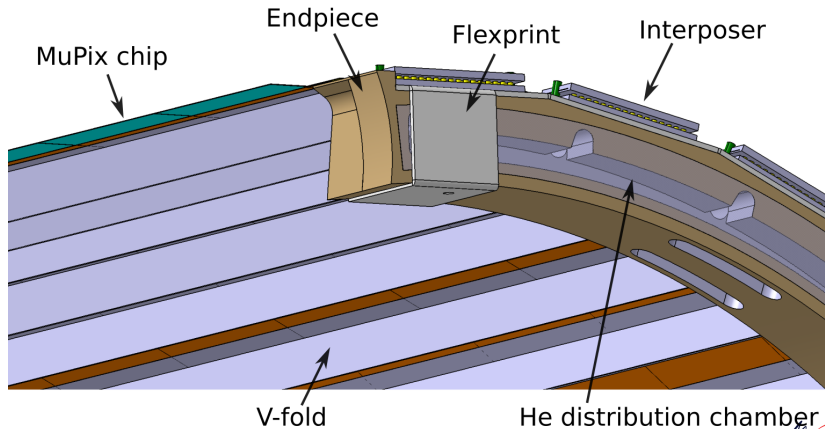


Shown: One layer 3 module inserted.

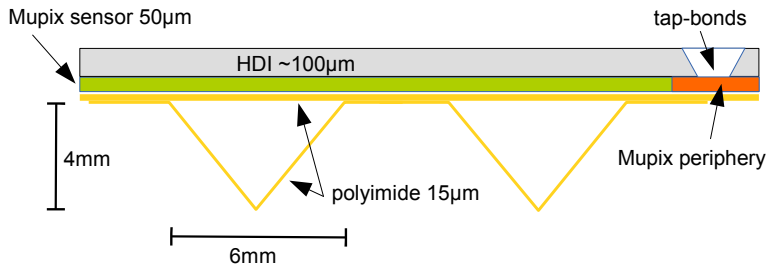
Observe the interposer (contact matrix) for electrical connections (power and signals). Industry standard component.



Pixel outer layer



Pixel outer layer



Pixel outer layer

How does the insertion mechanism work?

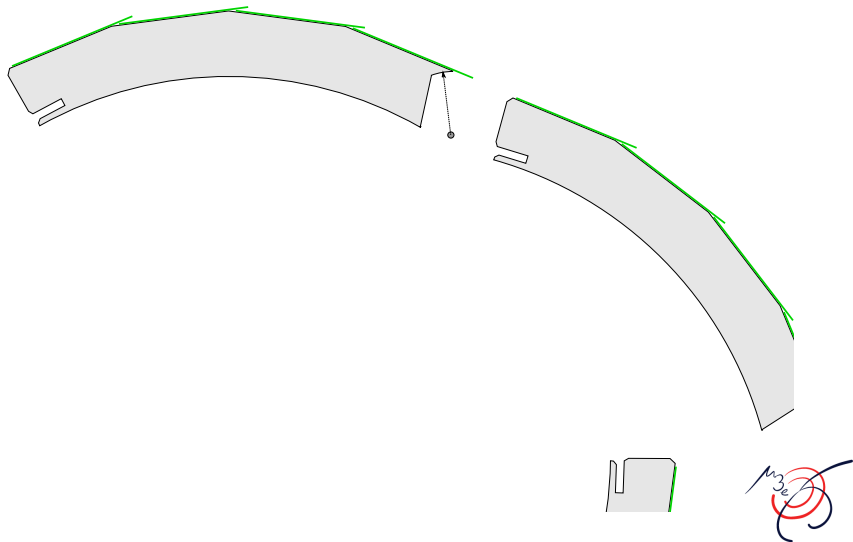
Next few slides show an animation.

Mechanically tested using 3d printed model.

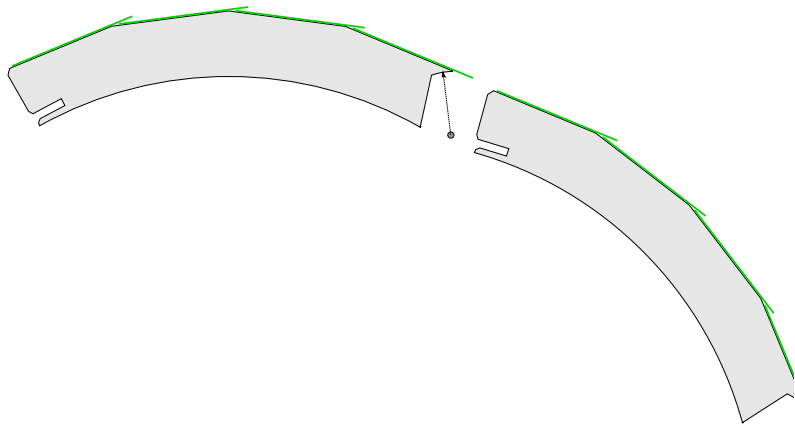
Note: Endpiece shape more matured meanwhile.



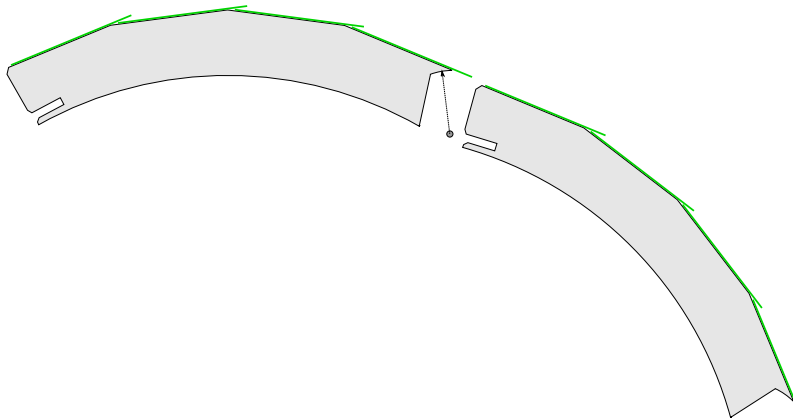
Pixel outer layer



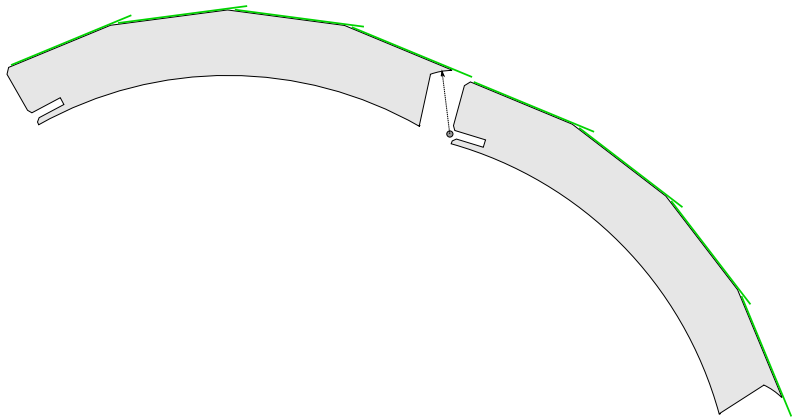
Pixel outer layer



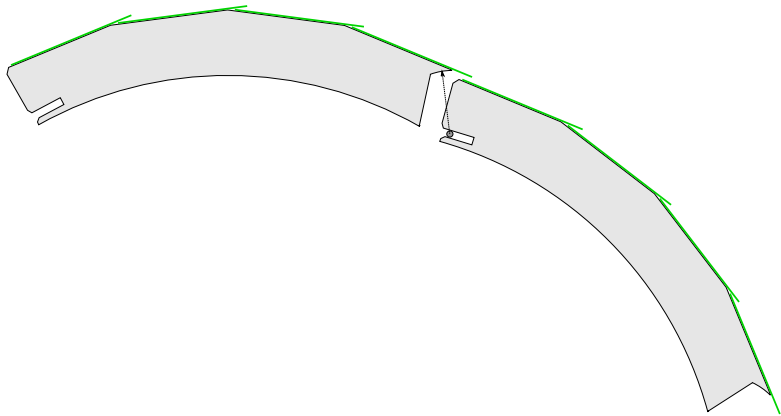
Pixel outer layer



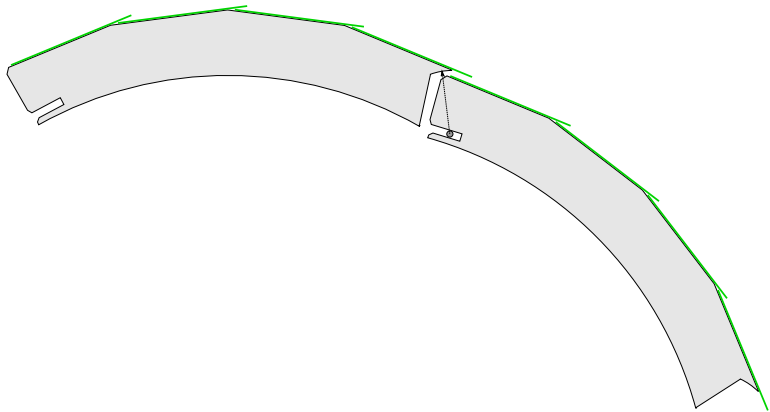
Pixel outer layer



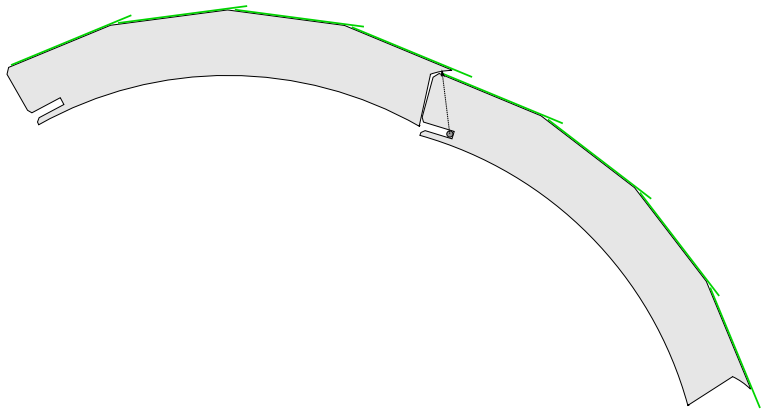
Pixel outer layer



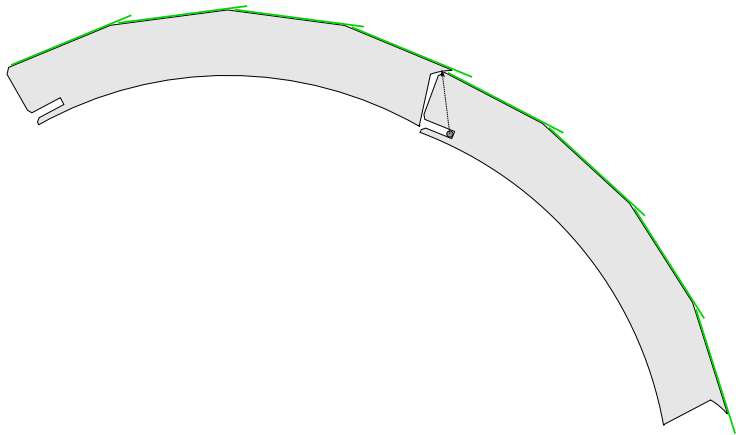
Pixel outer layer



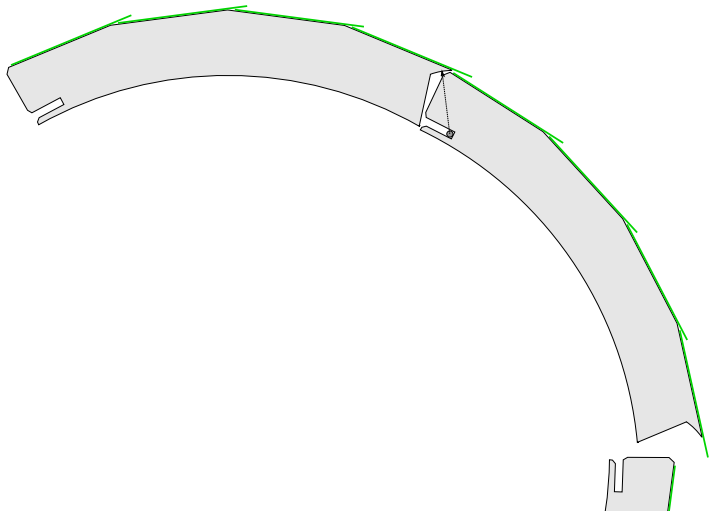
Pixel outer layer



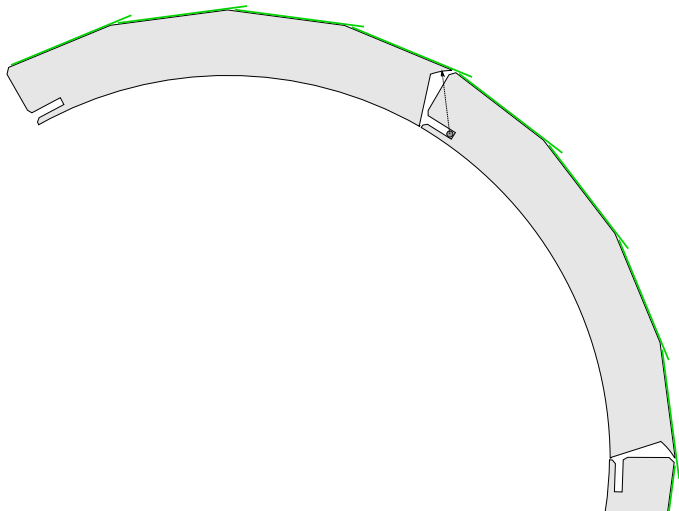
Pixel outer layer



Pixel outer layer



Pixel outer layer

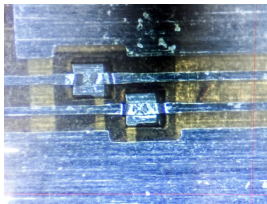


Ladder properties

Al 14 μm
PI 10 μm
Glue 5 μm
PI 25 μm
Glue 5 μm
Al 14 μm
PI 10 μm

HDI technology chosen to minimise material

Left: Stack of two conductor layers
Bottom: Example of SpTAB bond of a via.
Looks similar when to a chip.



Ladder properties

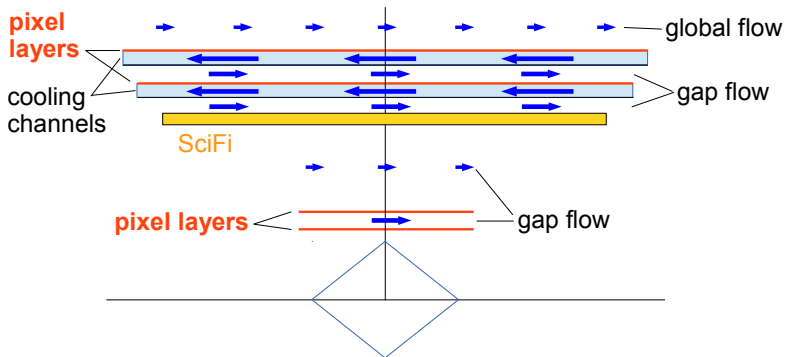
Tear-down of material contributions:

	Layer 1-2		Layer 3-4	
	t [μm]	X/X_0	t [μm]	X/X_0
MuPIX Si	45	0.48×10^{-3}	45	0.48×10^{-3}
MuPIX Al	5	0.06×10^{-3}	5	0.06×10^{-3}
HDI polyimide & glue	45	0.18×10^{-3}	45	0.18×10^{-3}
HDI Al	28	0.31×10^{-3}	28	0.31×10^{-3}
polyimide support	25	0.09×10^{-3}	≈ 30	0.10×10^{-3}
adhesives	10	0.03×10^{-3}	10	0.03×10^{-3}
total	158	1.15×10^{-3}	163	1.16×10^{-3}



Detector cooling

Cooling done using He flow:



Detector cooling

Following pages will show simulation results for outer layer modules.

Assumptions:

- ▶ Power dissipation 400 mW/cm^2

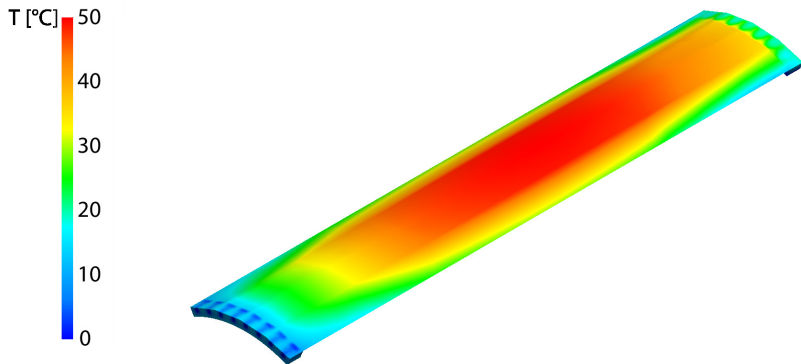
Pessimistic scenario. Chip is expected to dissipate less power (high resistivity substrate, one amplifier stage less).

- ▶ Helium flows
 - ▶ in folds: 20 m/s
 - ▶ between layers 3 and 4: 5 m/s
 - ▶ between layers 1 and 2: 10 m/s
 - ▶ global flow: 0.5 m/s



Detector cooling

First: outer layer module only:

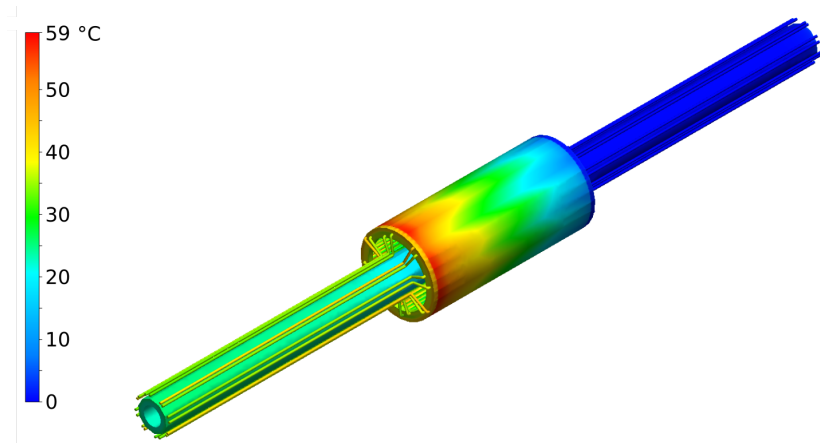


Note: Last year we showed results with higher ΔT . Had only one V-fold. Validation of simulation with measurement pending.



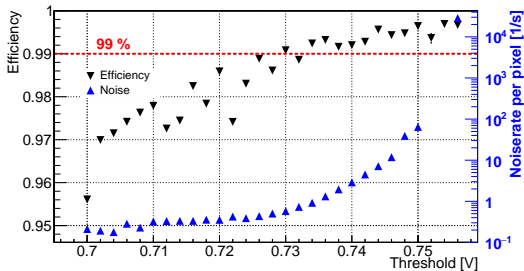
Detector cooling

Barrel thermal simulation (all 4 layers):



T_{\max} on inner layers is 40 °C (invisible in this plot)

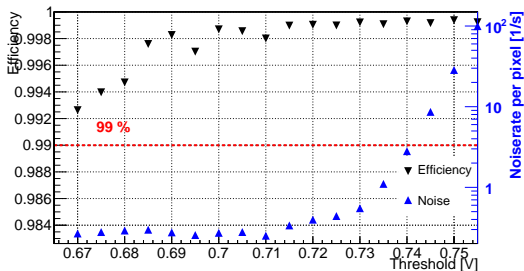


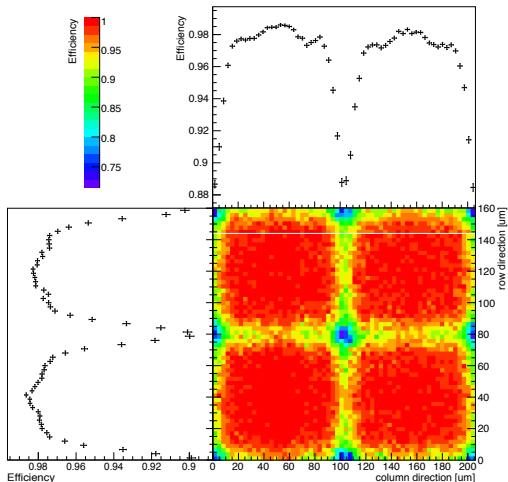


Efficiencies are very good at settings where power dissipation is 400 mW/cm^2

Top: perpendicular impact,
bottom: 60°

Beam: 4 GeV electrons



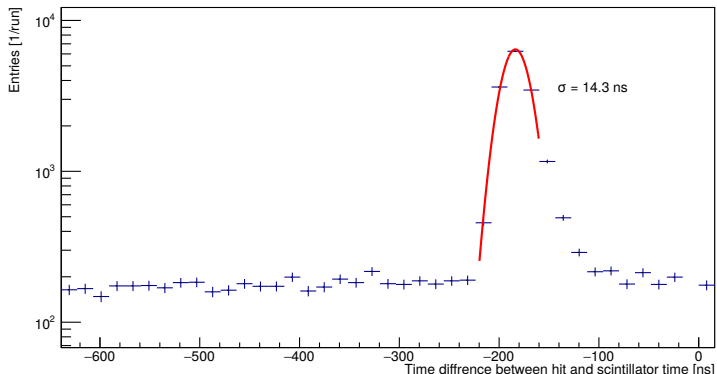


Sub-pixel efficiency study using EUDET telescope at DESY.

Bias voltage -40 V for lower overall efficiency to enhance effects.

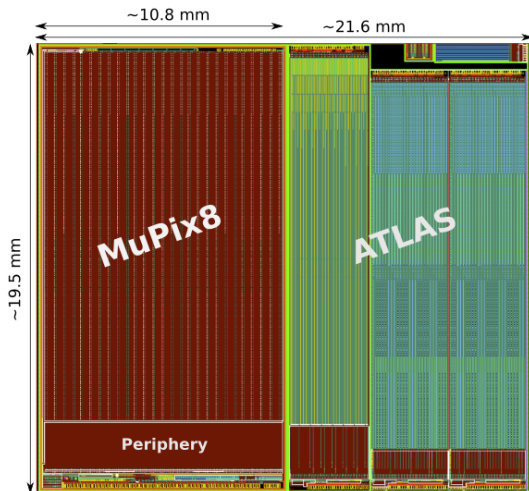


Time resolution at same power settings are very good:



- ▶ Results shown were from v7.
- ▶ v8 chip currently in production, expected in a few weeks
- ▶ Pixel size $80 \times 80 \mu\text{m}^2$ achieved
- ▶ Higher resistivity substrate: $80 \Omega \text{ cm}$ instead of $20 \Omega \text{ cm}$
- ▶ Power reduction expected
- ▶ Pixel cell to periphery cross-talk reduced
- ▶ Timewalk correction using time-over-threshold
- ▶ More features in TDR





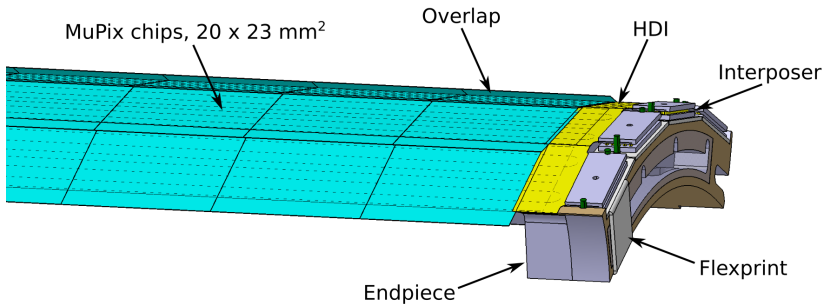
MuPIX8 currently in production

The chip will almost match full target size for the experiment but active area is smaller.



Manufacturing concept

Reminder: outer layer module:



Manufacturing concept

Central station consists of:

Part	Consists of
Layer 1	2 half-shells
Layer 2	2 half-shells
Layer 3	6 modules
Layer 4	7 modules

Approach:

- ▶ **Inner layers:** Four half-shells (module equivalent), unique parts.

⇒ **Prototype manufacturing**

- ▶ **Outer layers:** One station totals to 13 modules.

For three stations we need 39 modules of two types (L3/4)

⇒ **Small scale manufacturing**



Manufacturing concept

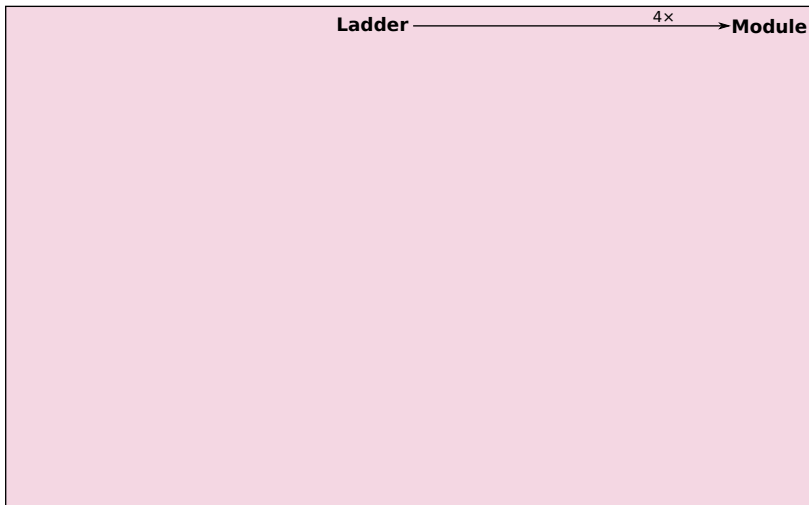
We want to make modules. . .

Module



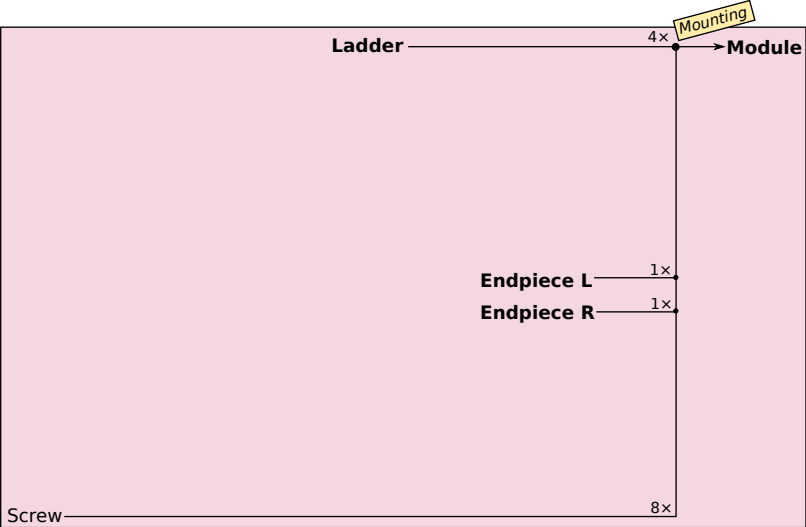
Manufacturing concept

For this we need ladders, of course



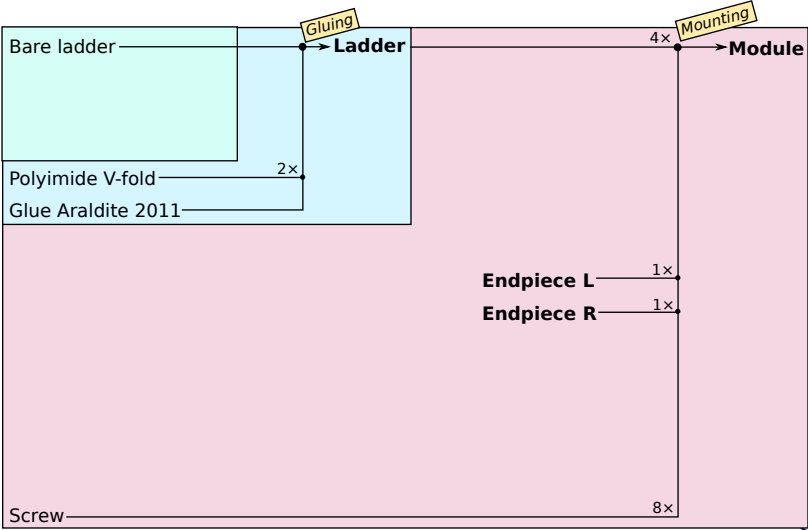
Manufacturing concept

Plus some other stuff



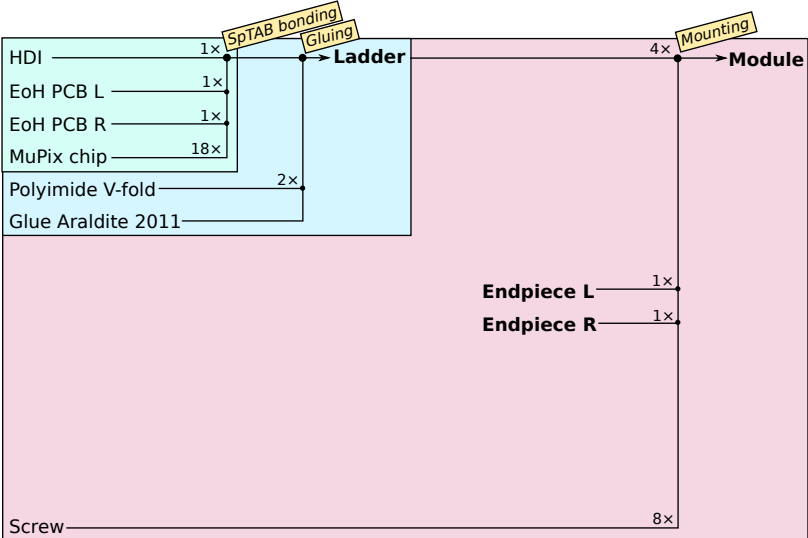
Manufacturing concept

But ladders are made of parts as well



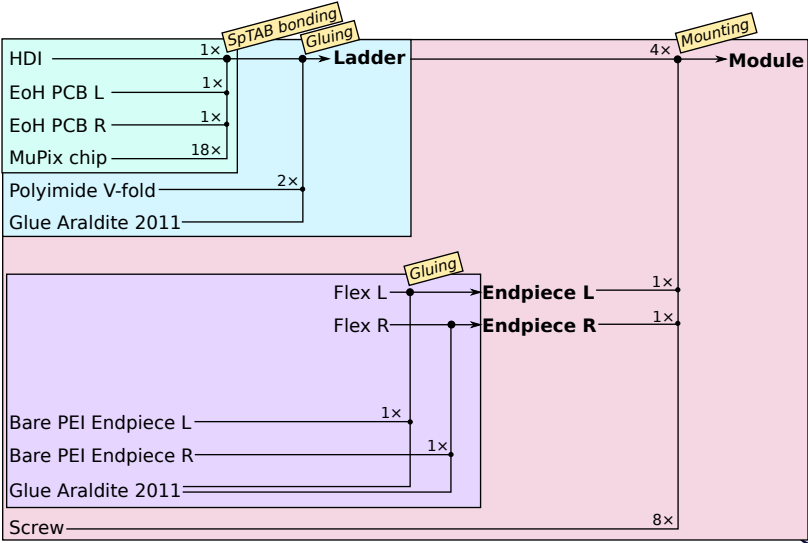
Manufacturing concept

The HDI is another sub-part



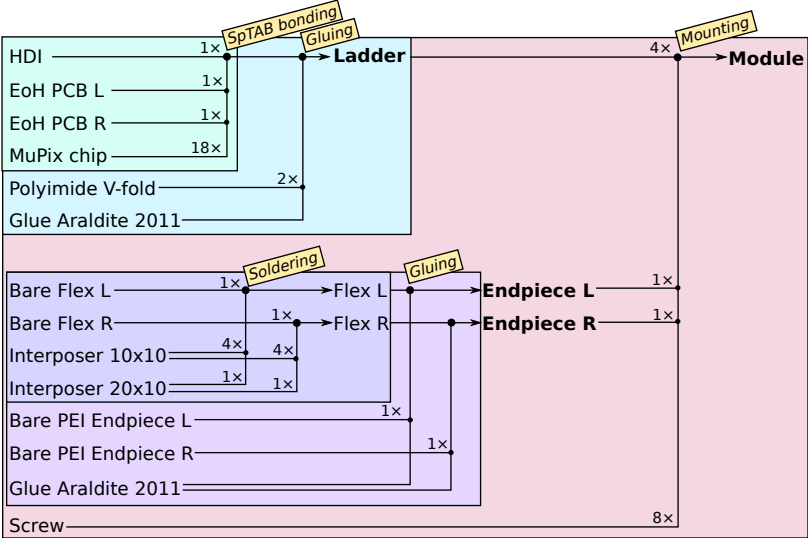
Manufacturing concept

More parts: Endpieces...



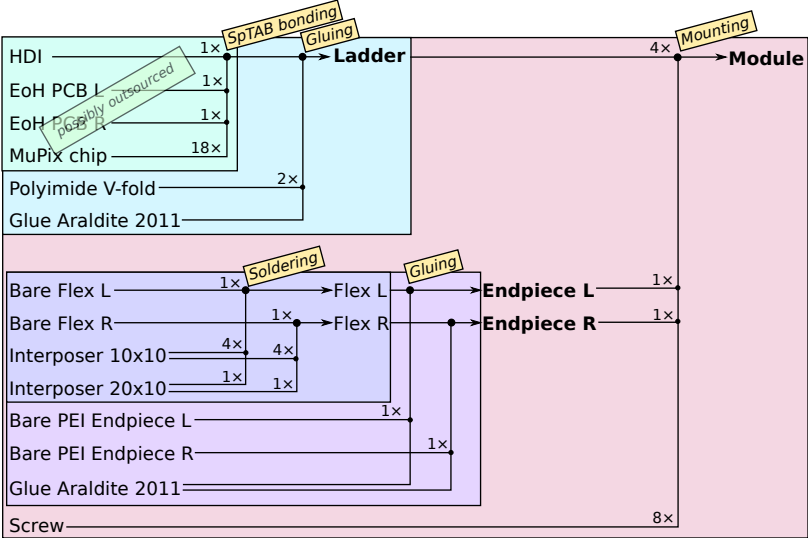
Manufacturing concept

... require some steps as well



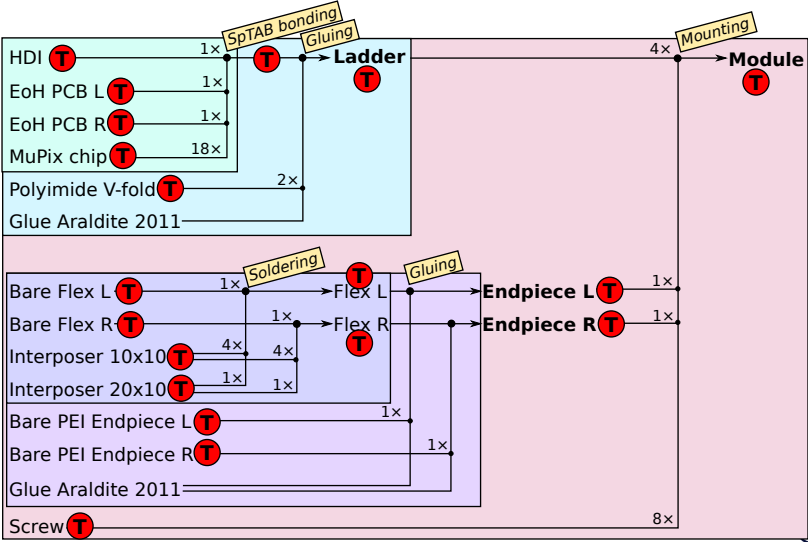
Manufacturing concept

Depending on supplier, outsourcing is an option



Manufacturing concept

Quality control takes place at every stage:



Manufacturing concept

Bill of material for 1 module

Product	per unit	per module
Ladder		4
HDI	1	4
End-of-HDI PCB (L)	1	4
End-of-HDI PCB (R)	1	4
MuPix chip	18	72
Polyimide V-fold	2	8
Screw	2	8
Endpiece (L/R)		2
Bare Flex	1	2
Interposer 10x10	4	8
Interposer 20x10	1	2
Bare PEI Endpiece	1	2

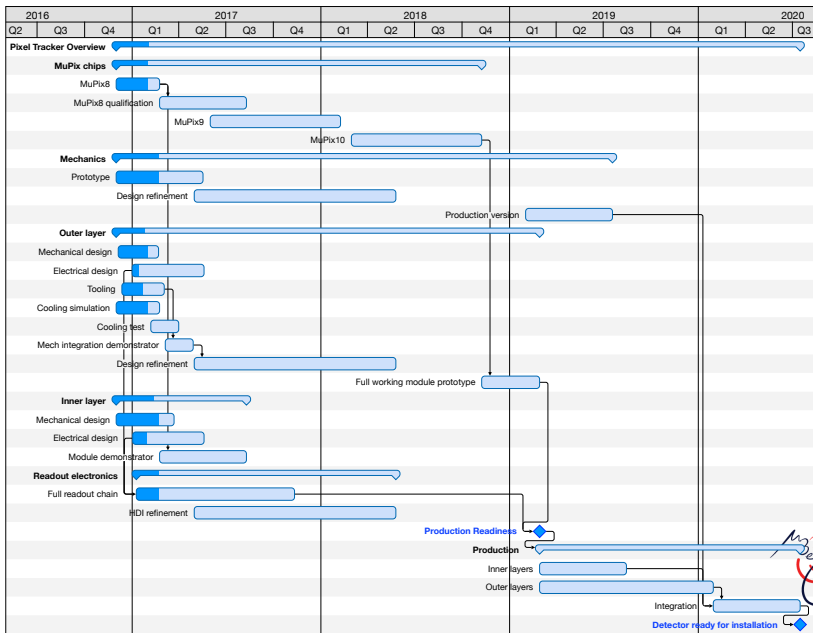


Bits and pieces

- ▶ **Vertical slice** test in progress, expected fully working towards autumn. Will include a **module demonstrator** operating 3 modules (= one electrical unit of an inner layer ladder) and a **full readout chain** (electrical and optical).
- ▶ **Cooling studies** were already good but will be repeated with improved 2 V-channel design.
- ▶ **Testboard** for MUPiX8 in preparation. Chip characterisation will start as soon as chips become available.
- ▶ **Tooling** for production line underway. Tools for making V-folds and gluing designed, waiting for workshop.



Tentative schedule



Conclusions

- ▶ Detector design matured, left concept stage for everything
- ▶ Module design available, manufacturing processes under development
- ▶ Existing MUPIX7 chip characterised and working very well
- ▶ New MUPIX8 chip available soon, first chip at full size – looking forward to
- ▶ Readout chain progressing well, full demonstrator later this year



BACKUP



Backup material

Plans for HDI

- ▶ Issue: Chips require filter capacitors nearby. Capacitors come with high- Z material, hence we have to move them out of the fiducial volume.
- ▶ We have to bridge up to 18 cm of power traces.
- ▶ We look into the option of integrating a plate capacitor into the HDI.
- ▶ Would change layering to 3 layers: 1 signal, 2 power/GND, the latter forming a cap
- ▶ Both vendors were confronted with the idea. Both think it can be done. Design limits will be investigated.
- ▶ In parallel we investigate how robust MUPiX8 is in terms of powering
- ▶ This is a topic for this year



Backup material

Mechanical stability of outer layer modules

- ▶ Has been investigated on previous design and found to be good
- ▶ Method: Detector surface response to acoustic signals using laser interferometry
- ▶ Will be repeated for new module design
- ▶ We expect new design to be more robust (doubled number of V-folds, smaller bending radius of edges) but need to cross-check
- ▶ Will use improved setup extending interferometer to resolve counting ambiguity issues we had in the past



Backup material

Serial powering option

- ▶ MUPIX7 showed very little dependence on chip activity during operation, e.g. no significant change in power consumption between beam on/off
- ▶ This makes MUPIX a candidate for serial powering
- ▶ Current MUPIX designs not suitable because they need more than one supply power
- ▶ Serial powering hasn't been a requirement but our measurements suggest potential
- ▶ We will design a test setup to investigate further
- ▶ A future version of MUPIX would require internal voltage regulators in order to reduce chip to one external supply voltage
- ▶ Has implications, not a priority task but highly interesting



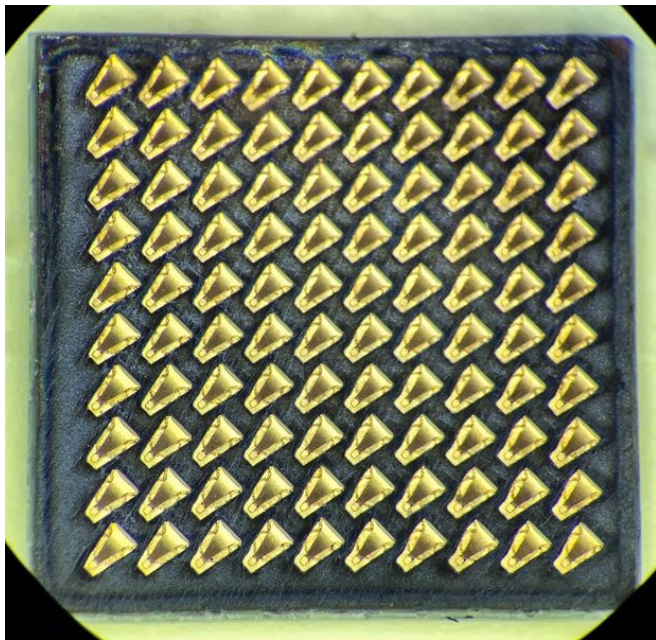
Backup material

MUPIX plans

- ▶ MUPIX8 still requires too many pad connections to be used for a full outer layer prototype module
- ▶ HDI technology in aluminium does not allow for the density needed for a MUPIX8
- ▶ We foresee MUPIX9 for consolidation of open issues
- ▶ Will bring things like simplified slow control (fast, unidirectional I²C à la CMS pixel or anything else feasible), voltage regulators, reduced pad scheme
- ▶ Will be a small footprint MPW study
- ▶ MUPIX10 envisioned to be the first chip to full spec

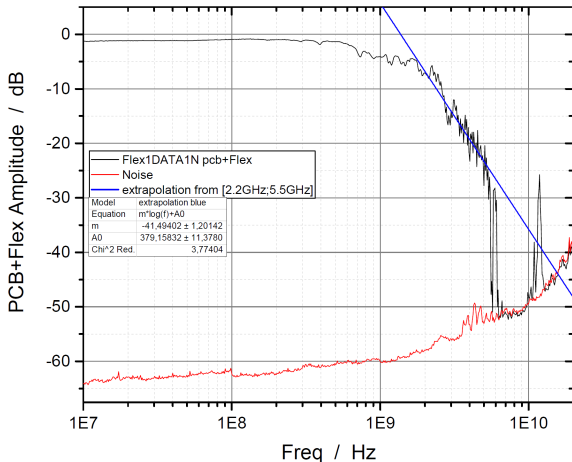


Backup material



Backup material

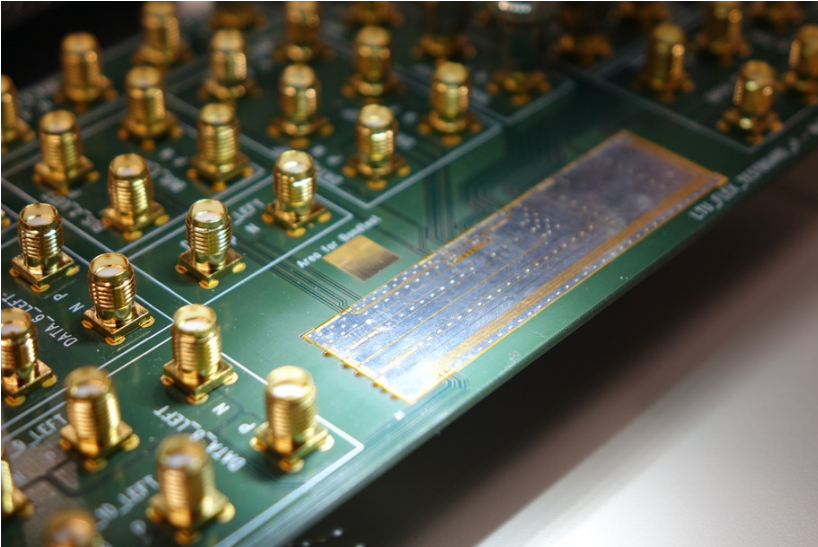
Bode plot of HDI in LTU technology:



Note: BER test showed no errors ($< 5.9 \times 10^{-13}$) at 2.5 GHz (double the speed we use)

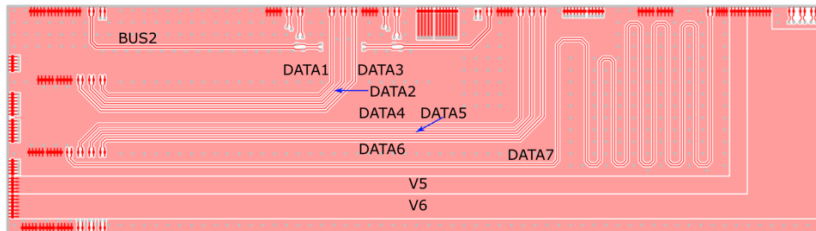


Backup material



Backup material

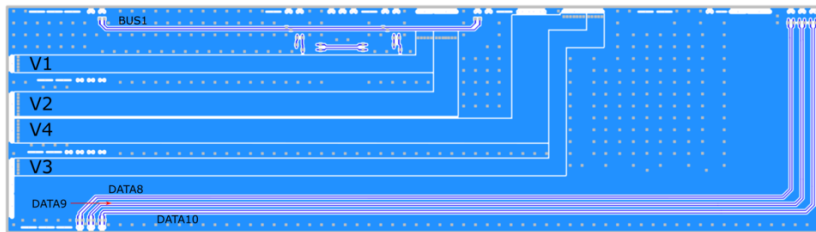
Layout of HDI used for characterisation:



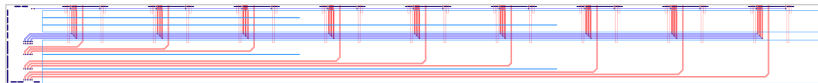
Note: DATA7 has a length of 18 cm, matching the longest trace on an outer layer module.



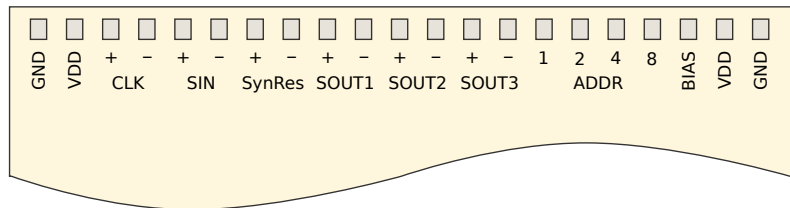
Backup material



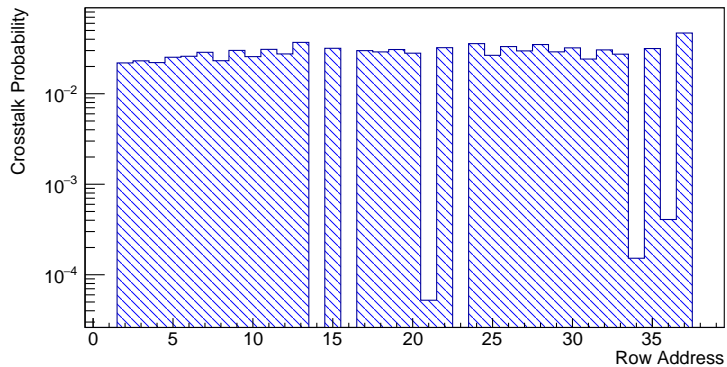
Backup material



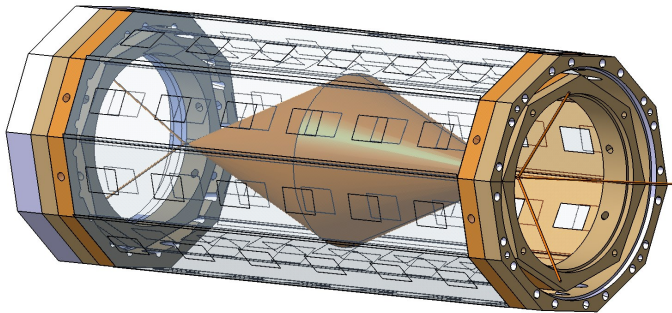
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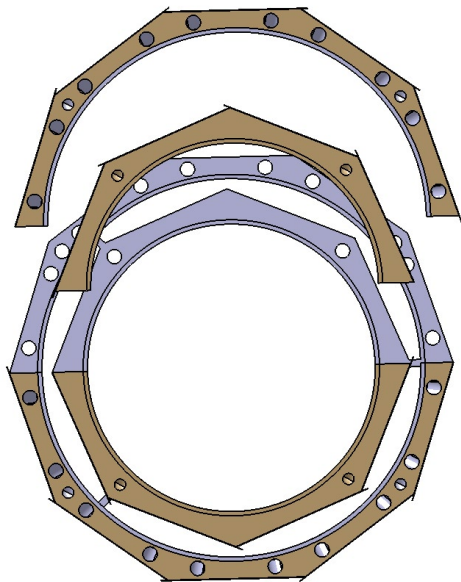
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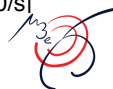
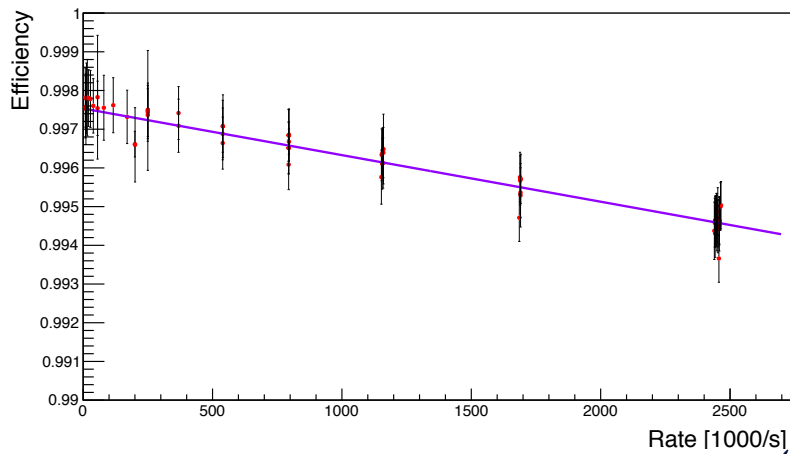
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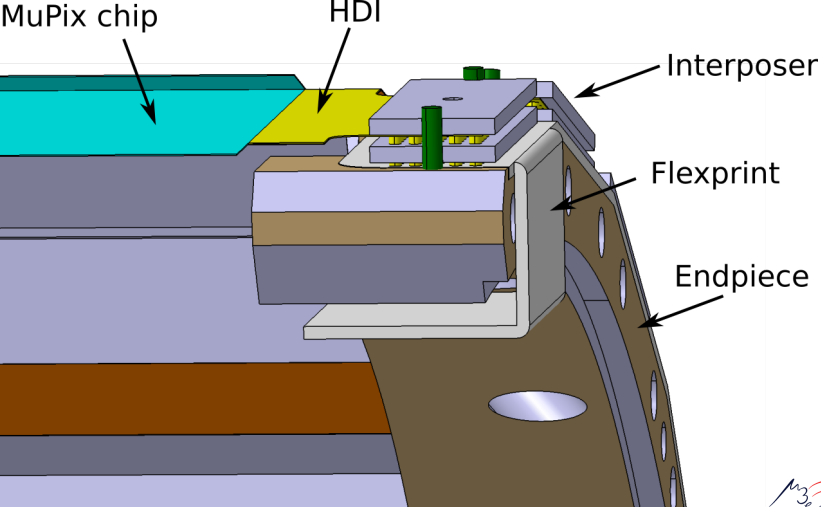
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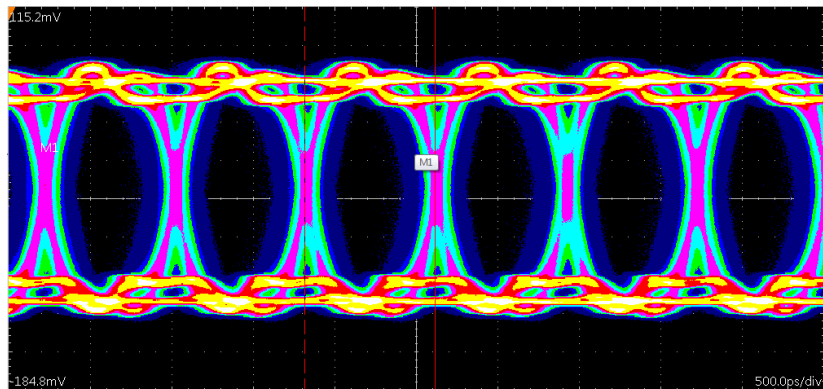
Backup material



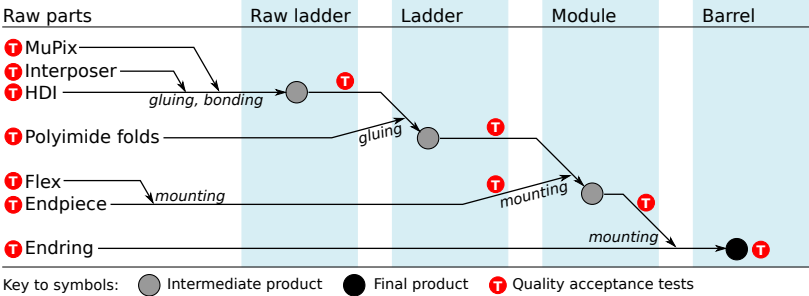
Backup material



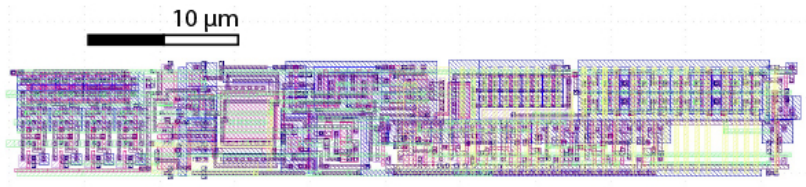
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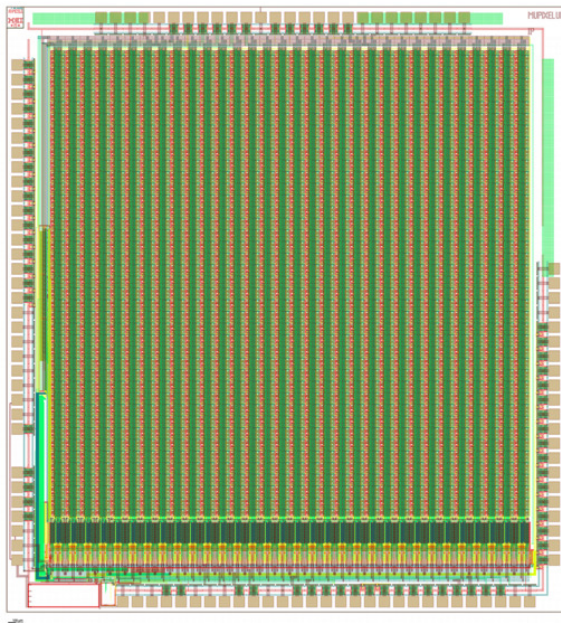
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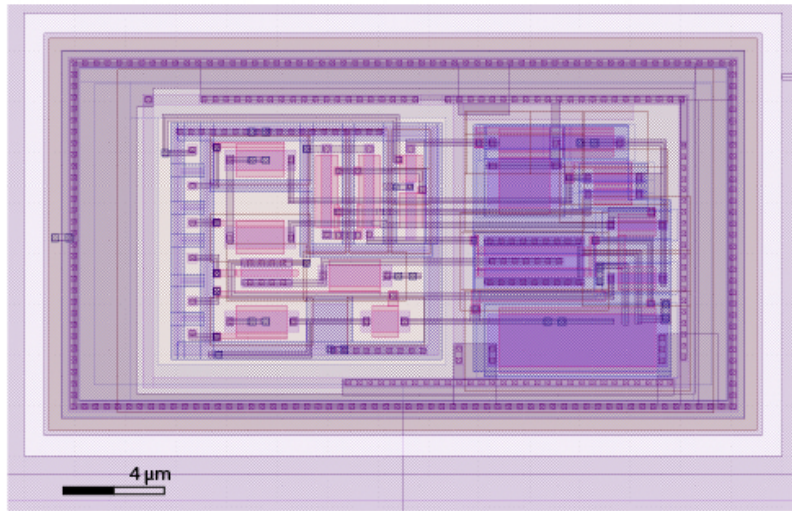
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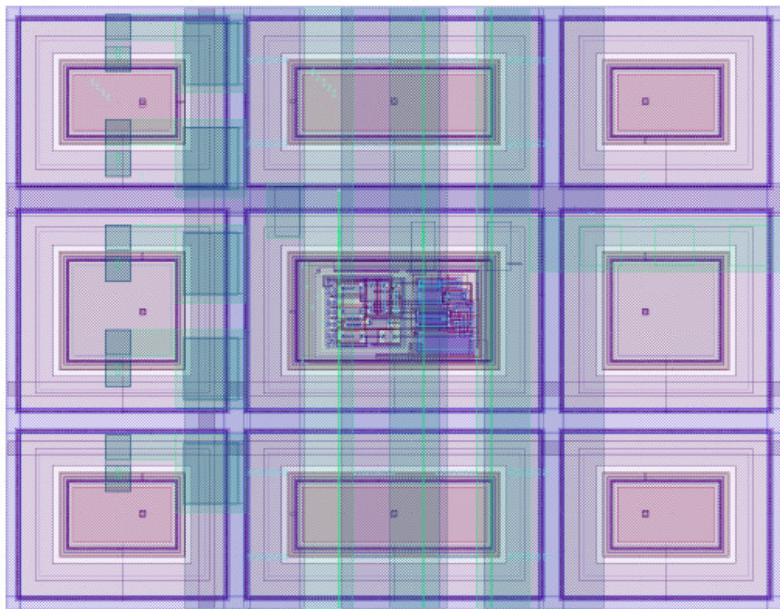
Backup material



Backup material



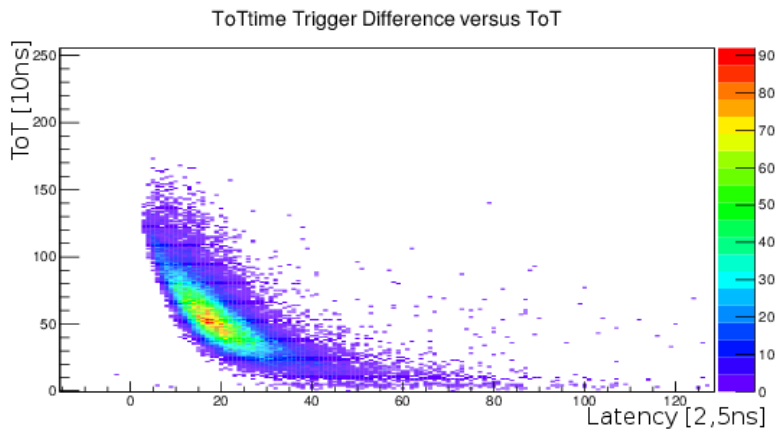
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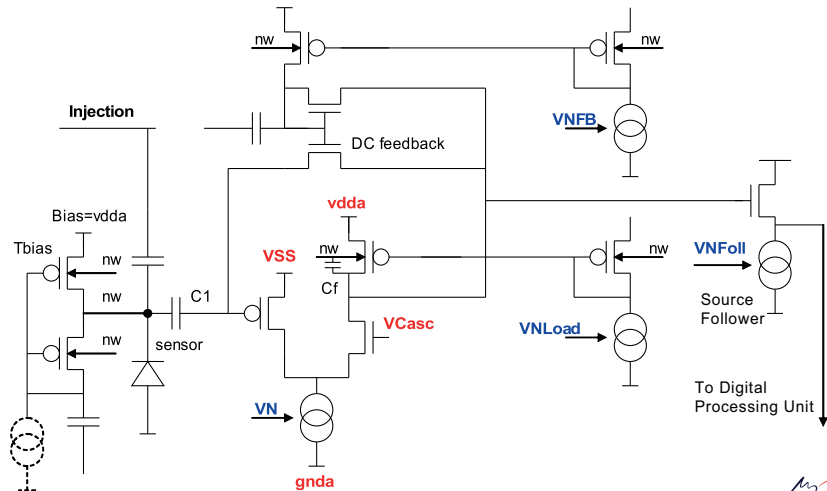
20 μm



Backup material



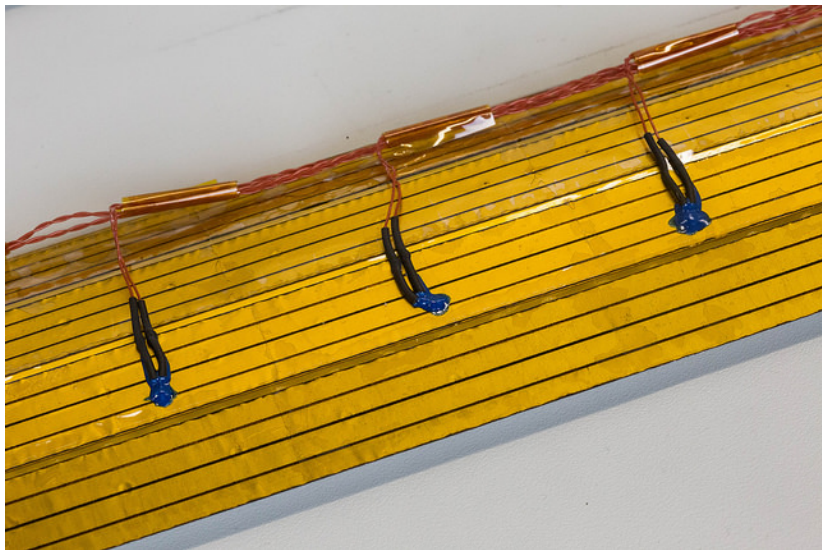
Backup material



Backup material

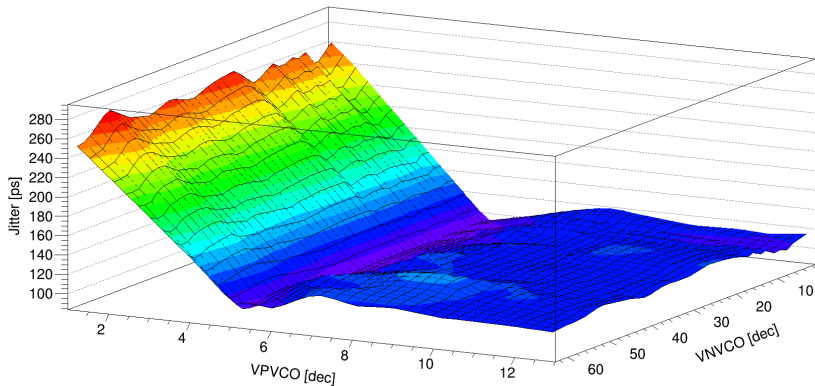


Backup material

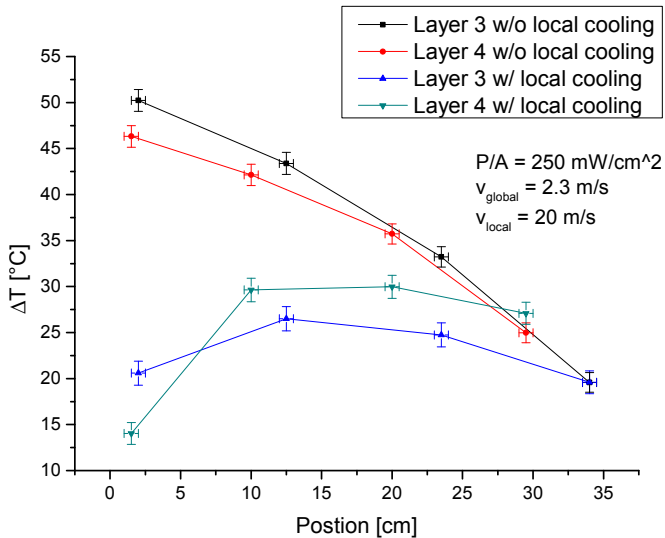


Backup material

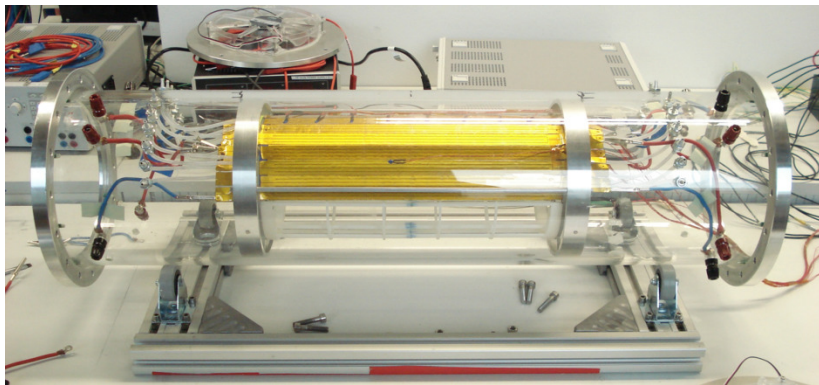
Jitter (EnPLL = 1, VPPump = 20 [dec])



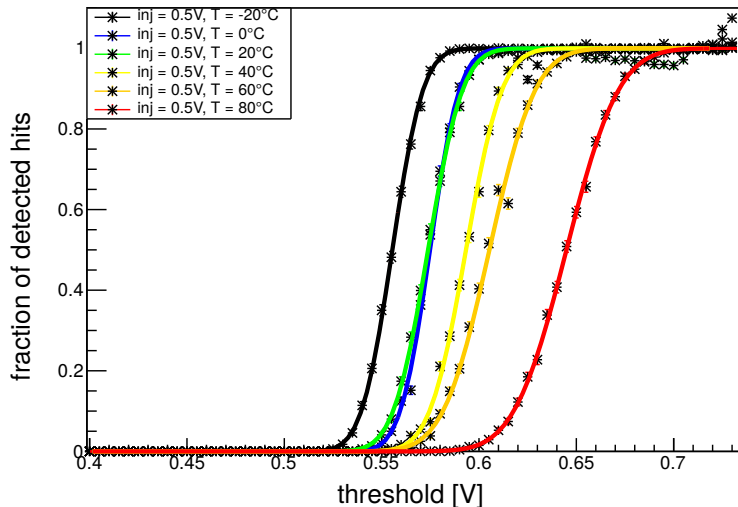
Backup material



Backup material



Backup material



Backup material

