Mu3e Inner Detector Design and Pixel
PSI BVR 2018

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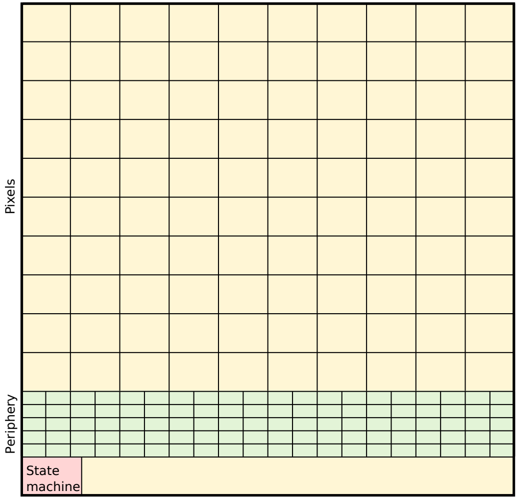
Overview

MuPix

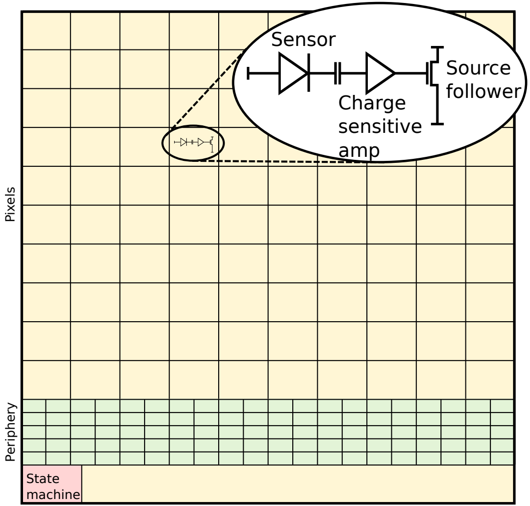
MuPix – Principle



The MuPix chips are depleted MAPS chips consisting of

- Active pixel matrix
- Partner pixel in periphery
- State machine
- Plus support circuitry (VCO, PLL, etc., not shown)

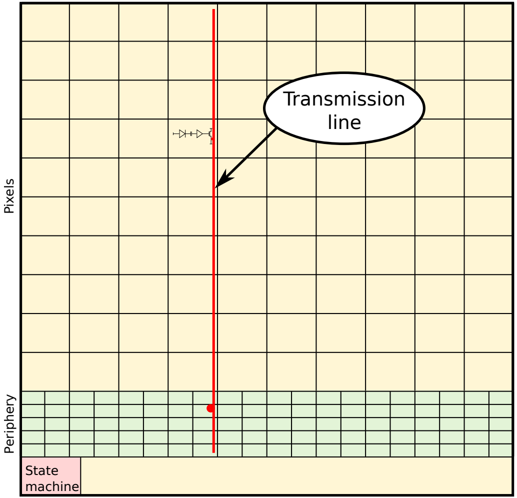
MuPix – Principle



The **analog cell** has

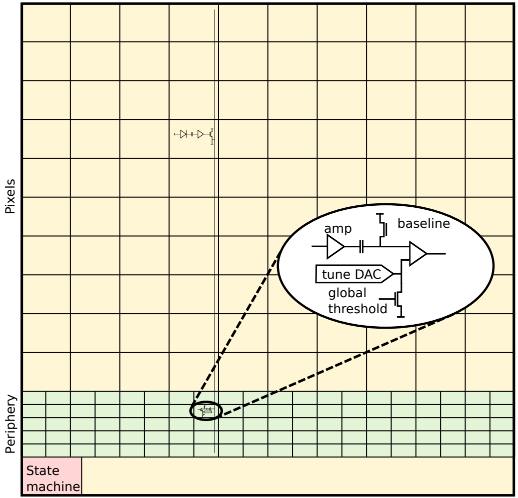
- a reverse biased sensor ($\approx -85\,\text{V}$)
- a charge sensitive amplifier
- a source follower to drive. . .

MuPix – Principle



the **transmission line** to the corresponding partner cell in the periphery.

MuPix – Principle

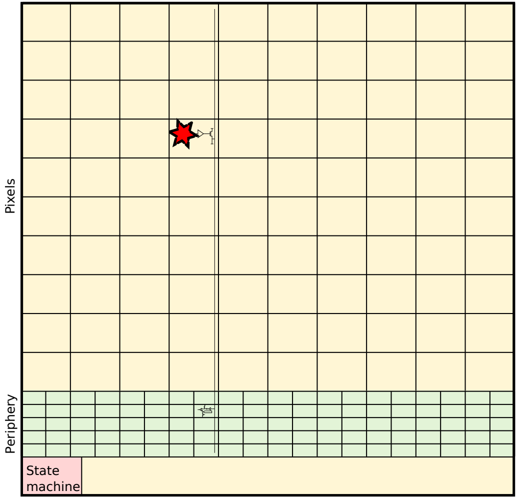


In the **partner cell**, the transition from analog to digital happens:

- an amplifier
- a comparator
- tuning capabilities

This separation protects the analog cell from digital crosstalk.

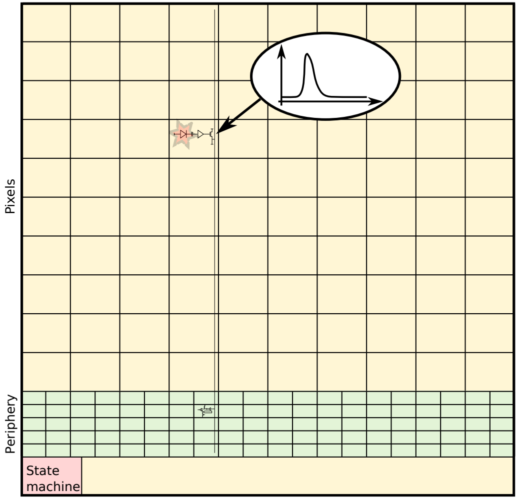
MuPix – Principle



All this results in a **non-shuttered**, **self-triggered** monolithic pixel chip.

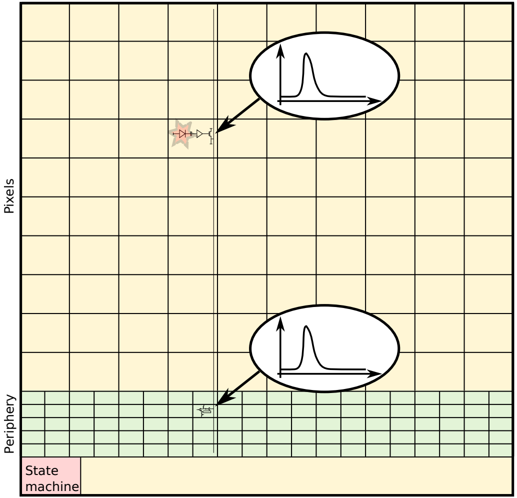
Upon a hit. . .

MuPix – Principle



. . . the charge sensitive amplifier sends a pulse proportional to the charge. . .

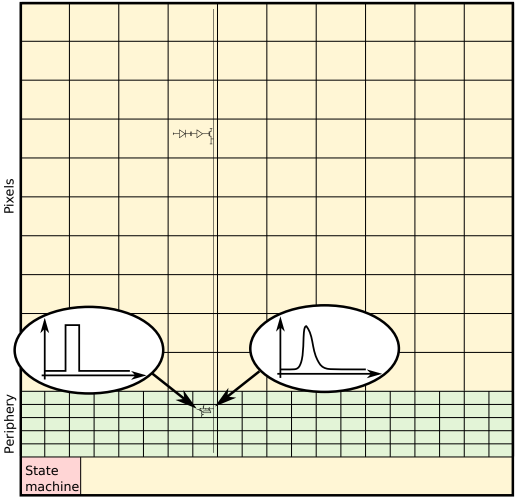
MuPix – Principle



. . . across the transmission line . . .

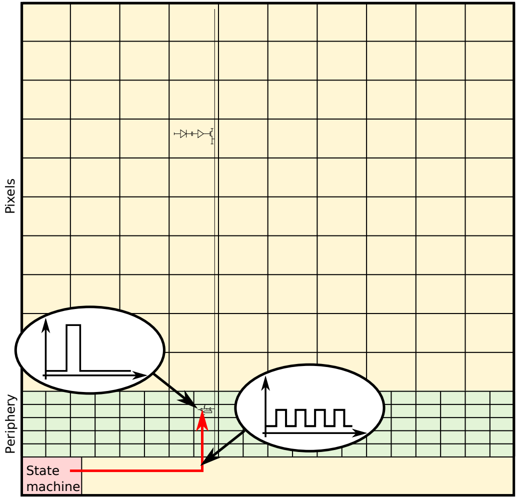
BTW: every pixel has its own transmission line

MuPix – Principle



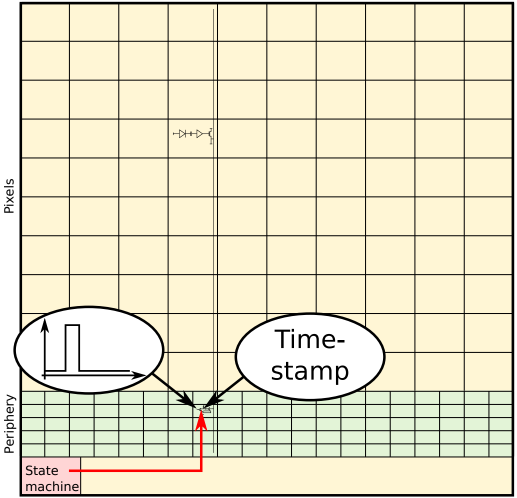
. . . and the comparator in the periphery creates a digital signal, if above threshold.

MuPix – Principle



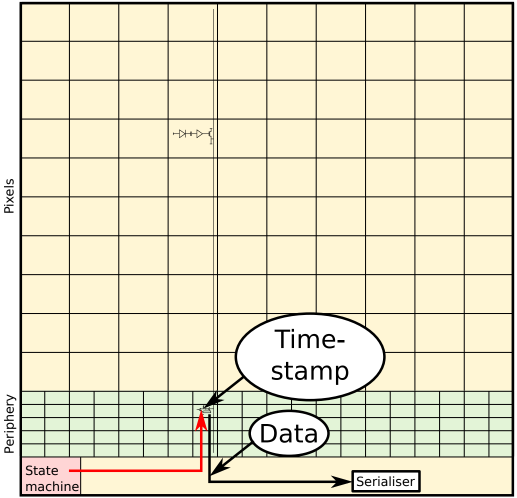
The state machine provides clock for a counter. . .

MuPix – Principle



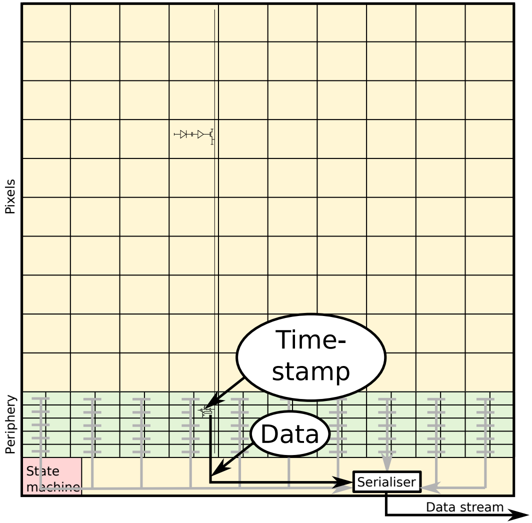
. . . in order to create a timestamp.

MuPix – Principle

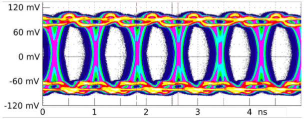


The data (pixel location, timestamp) goes through the serialiser. . .

MuPix – Principle



. . . and all the data is transmitted to the data stream at 1.25 Gbit/s.



MuPix

This design choice results in a

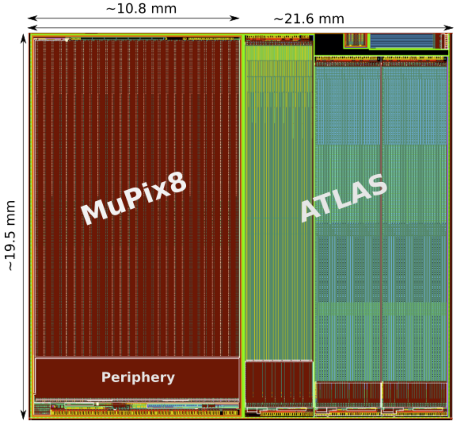
- pixel unit cell, that is always sensitive ⇒ „self-triggered“ and non-shuttered
- time-stamp allows event formation

This is tailored to our needs because we have

- no bunch structure
- no possibility for a reliable trigger with almost no material
- monolithic chips can be thinned to about 50 µm

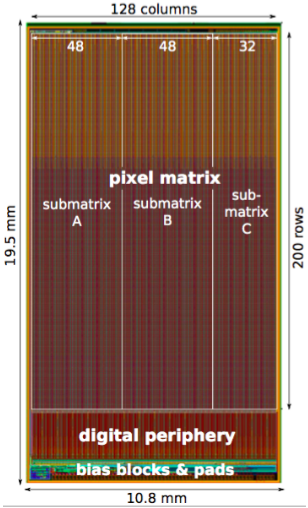
MuPix

- MuPix8 received in August 2017
- Column length close to final requirement
- 128 × 200 pixels
- 80 × 81 µm^2 pixel size
- 4 LVDS links at 1.25 Gbit/s
- 2 comparators allowing for ToT
- Pixel masking and tuning
- Temperature stabilised voltage reference
- On-chip thresholds
- Temperature diode

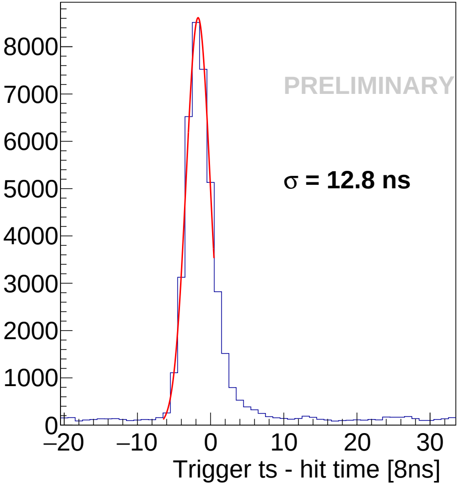


MuPix

- Matrix A similar to MuPix7, voltage transmission
- Matrices B and C use current transmission, not yet optimised
- A has much better time resolution
- Analyses focusing on matrix A
- Two test beam campaigns at DESY (positrons, 4 GeV)

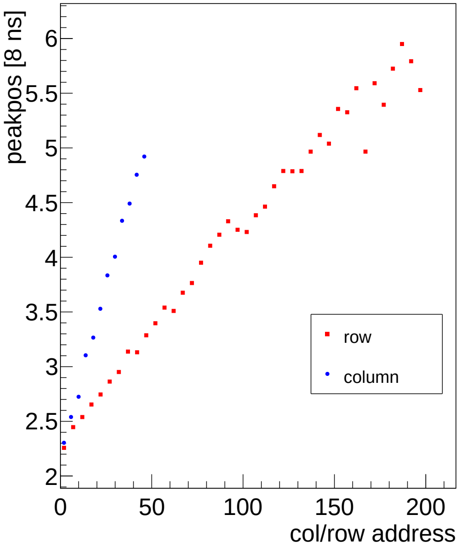


MuPix



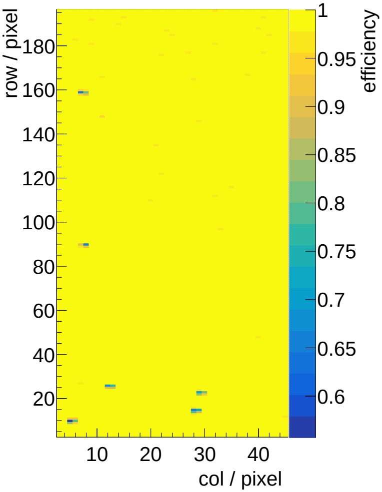
- Measured in telescope with two scintillating tiles as time references

MuPix

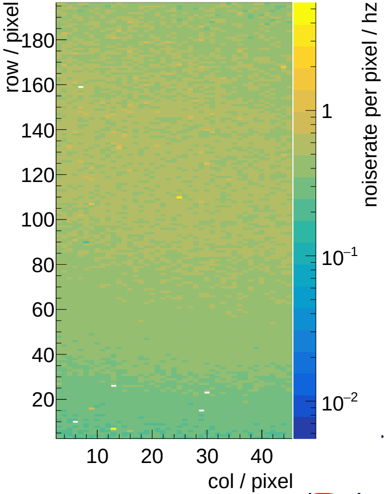


- We see propagation effects.

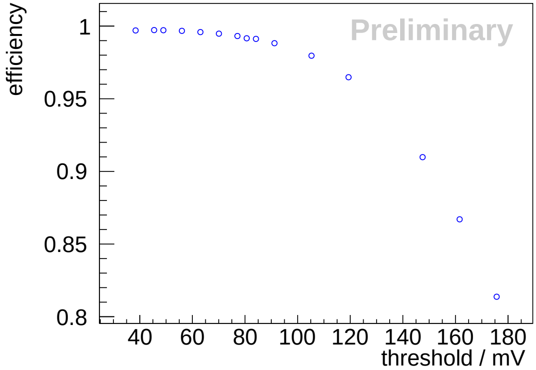
MuPix



- Chip is very efficient: 99.7% (hot pixel masked)
- Noise rate at low level of $\approx 0.2\,Hz$
- Chip untuned
- Measured overall power dissipation: $210 \pm 10\,\mathrm{mW/cm^2}$

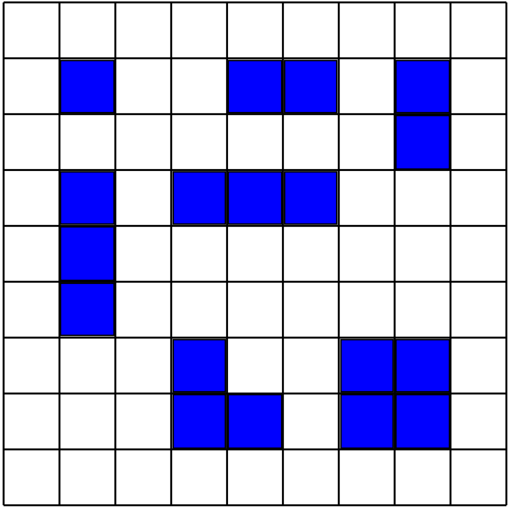


MuPix



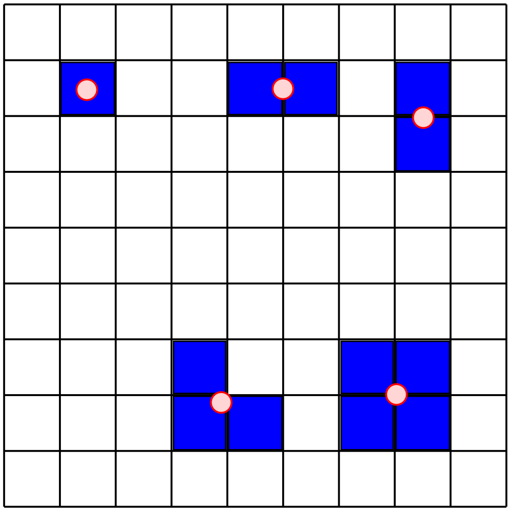
- Efficiency scan for an untuned chip
- Essentially noise free (as previous slide shown already)
- Bad pixels ignored in analysis

MuPix



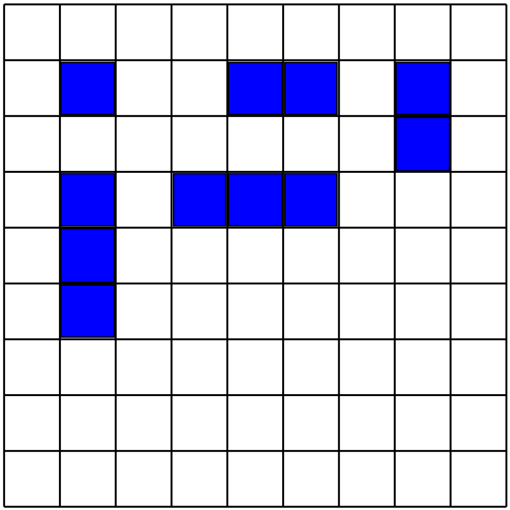
- Clusters larger than one come from charge sharing or crosstalk

MuPix



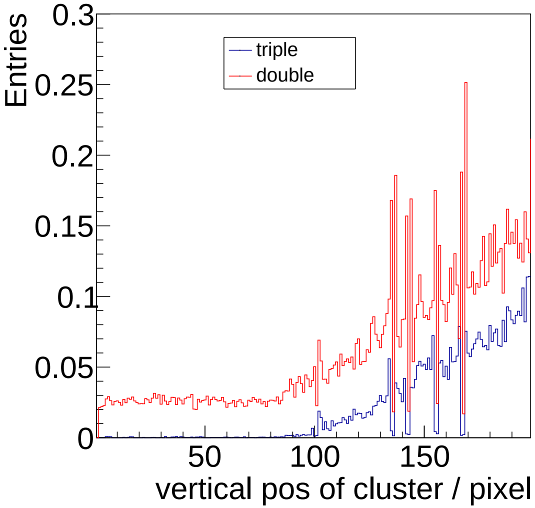
- Clusters larger than one come from charge sharing or crosstalk
- Charge sharing only for pixels sharing boundaries

MuPix



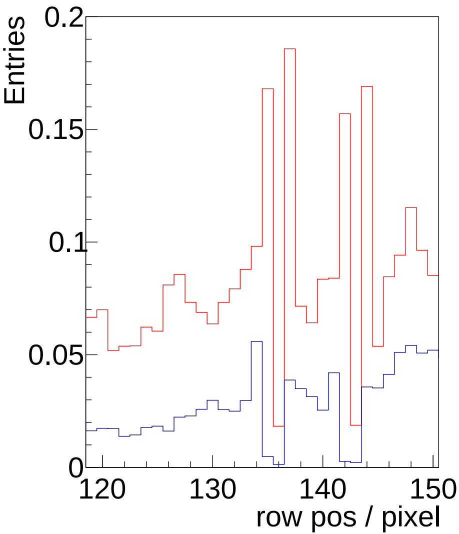
- Clusters larger than one come from charge sharing or crosstalk
- Crosstalk acts on neighbours, excluding some carge sharing cluster types but adding new ones

MuPix



- Clusters larger than one come from charge sharing or crosstalk
- Horizontal cluster size distribution uniform $\rightarrow$ attributed to charge sharing
- Plot shows trend in vertical direction
- Shown here: $\frac{N_{\text{cluster vert}} - N_{\text{cluster horiz}}}{N_{\text{cluster}}}$
- Estimates cross-talk from neighbouring transmission lines
- About the drops, see next slide. . .

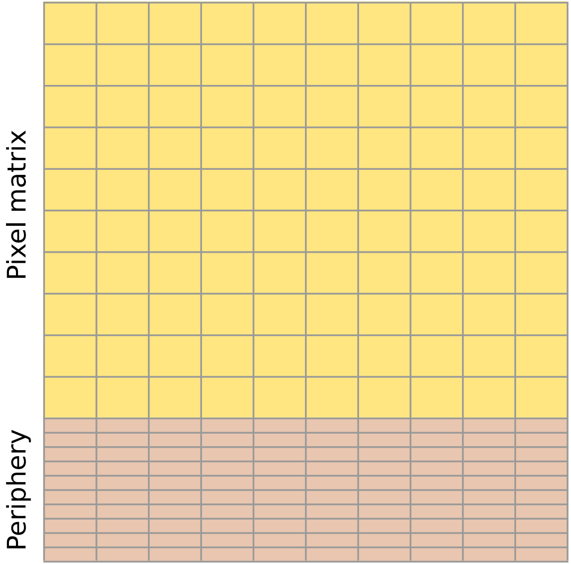
MuPix



Zoomed into previous plot.

- Recall the point-to-point connections pixel to periphery
- Cross-talk can happen between neighbouring transmission lines
- Some lines have wider spacing in design ⇒ drops
- Peaks are a normalisation effect

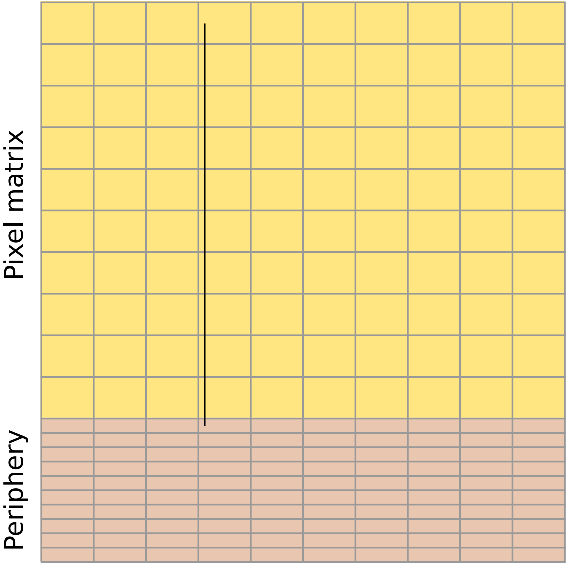
MuPix – Principle



Can we understand this?

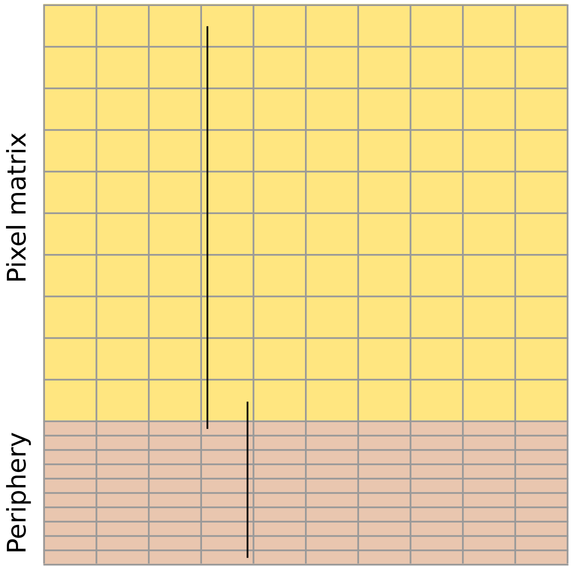
Here is a sketch of the pixel array and the corresponding mirror pixels in the periphery.

MuPix – Principle



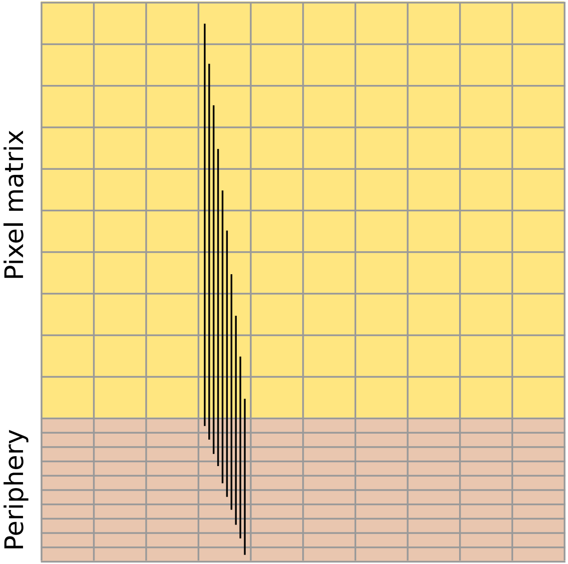
One pixel is connected via a transmisison line to its mirror pixel.

MuPix – Principle



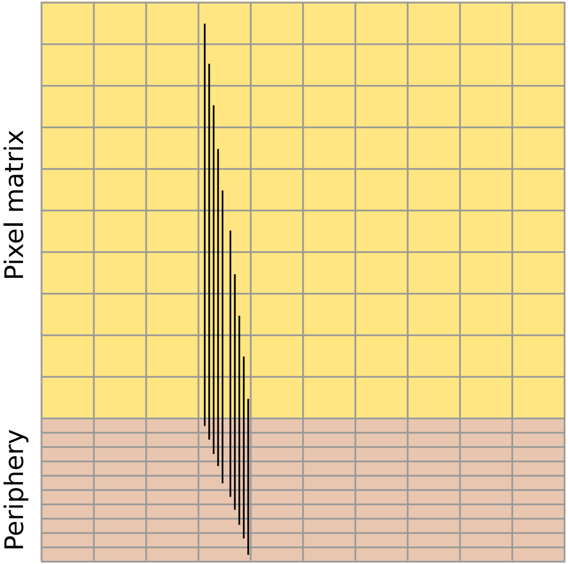
The lines do not have the same length.

MuPix – Principle



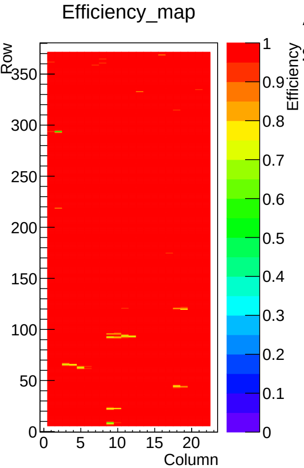
And the dense packaging allows for cross-talk between neighbouring lines.

MuPix – Principle



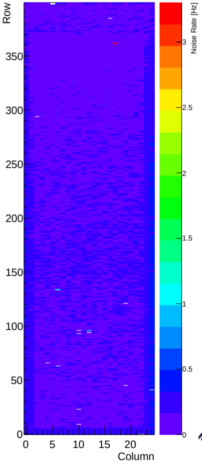
If, by chance, there is a pair with wider spacing, cross-talk probability goes down.

MuPix – AtlasPix



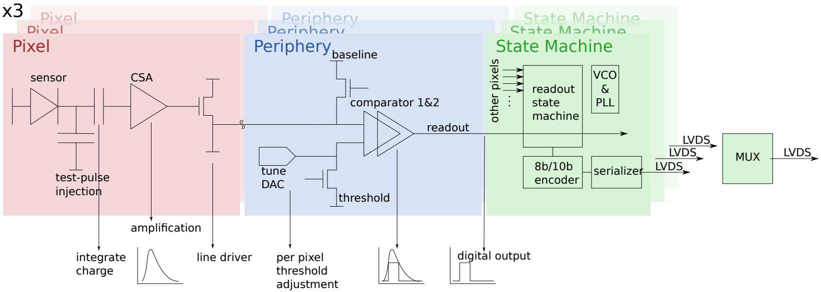
A few words about the AtlasPix (same submission)

- Similar design but comparator inside pixel cell (next slide)
- Is a design option for us as well
- Efficiency is good: 99.8% (hot pixels not excluded)
- Very promising: Cross-talk lower than in MuPix8 (data taking started later, analysis ongoing)

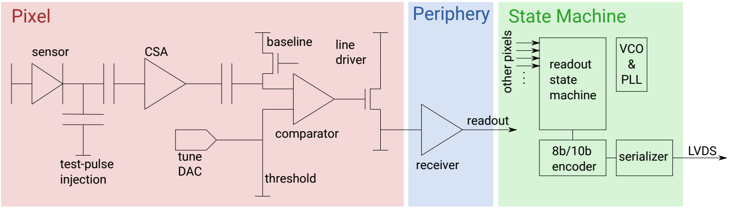


MuPix – AtlasPix

MuPix8



AtlasPix



MuPix – Plans

- **MuPix8** will be further tested, especially when good batch arrives
- **MuPix9** is a small scale chip for testing
  - system integration, mainly slow-control
  - powering

  Expected back in February. Test program prepared, electronics ready.
- We are preparing for **MuPix10**
  - the first full-scale chip with $20 \times 20\,\mathrm{mm}^2$ active area
  - submission foreseen this summer
  - will contain cross-talk mitigation (based on MuPix8 experience) and system integration aspects (based on MuPix9)

MuPix – preliminary summary

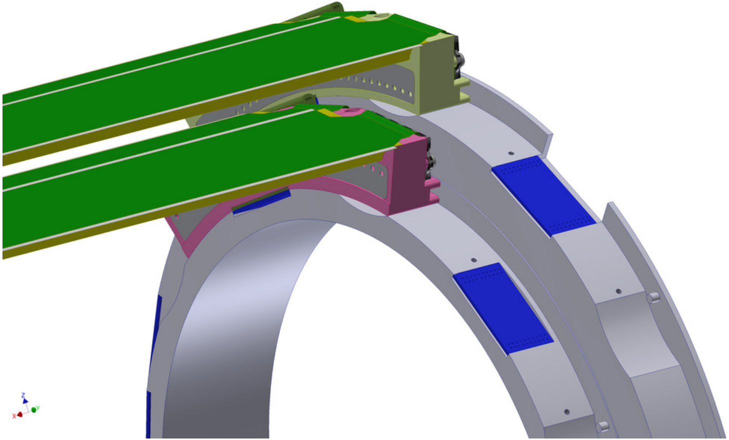
- MuPix8 well understood, **performs very well**
- Known issue: AMS reported **quality issues** with metal layer 3. Required some tweaks to overcome voltage drops inside chips.
- Good batch expected in March. Will repeat essential measurements.
- Crosstalk can be mitigated with
  - Rearranging transmission lines similar to Mupix7
  - Use ATLASpix scheme with comparator in pixel
- Plan for submission of **full-sized chip** in summer this year

Design status

Design status

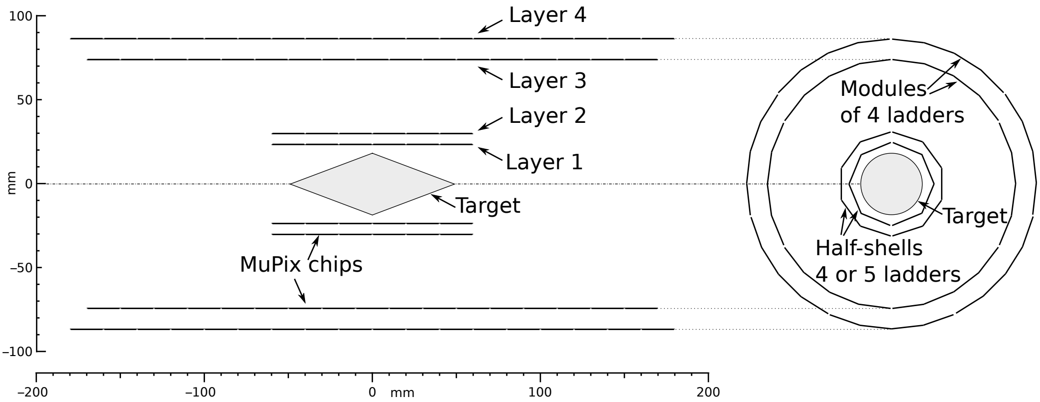
- Modular design of pixel detector presented last year.
- Refined parts and fabricated them with close-to-reality material.
- Extensive design work for cooling and cabling performed and almost final. Following slides try to explain.
- Mock-up parts available.

Design status



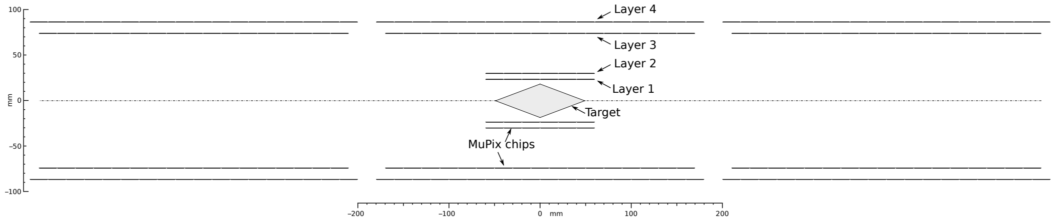
Shown: One one module per layer inserted.

Design status



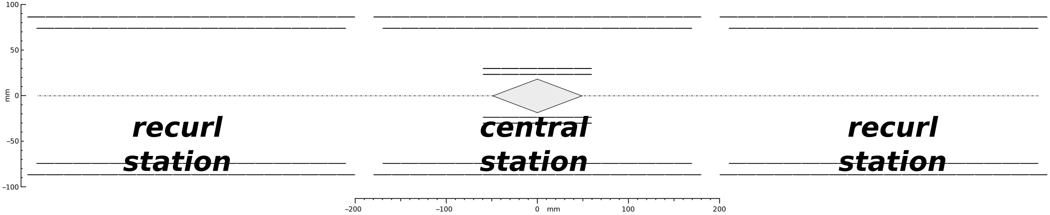
This shows central station only.

Design status



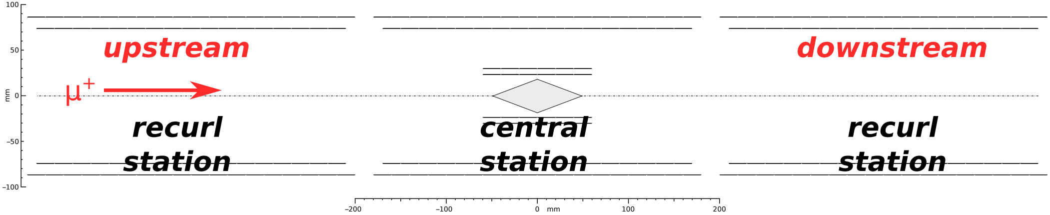
The pixel detector will be longer. . .

Design status



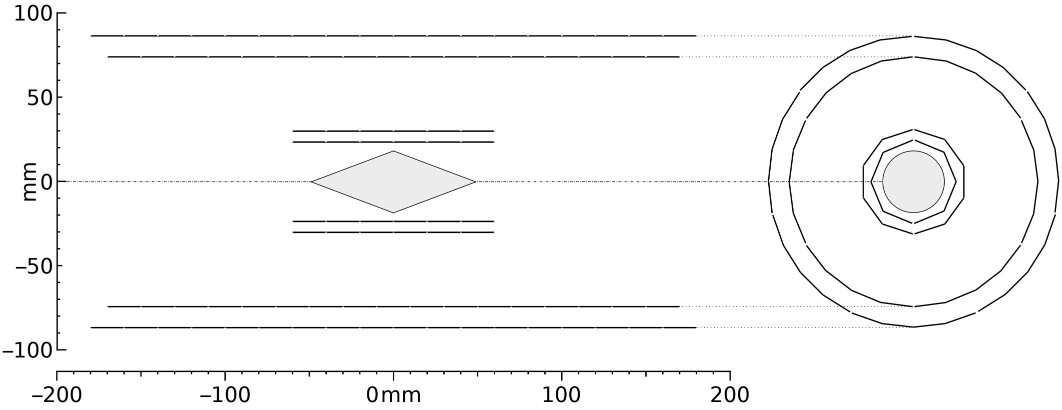
Configuration amended with two recurl stations (copies of layer-3/4 from central station).

Design status



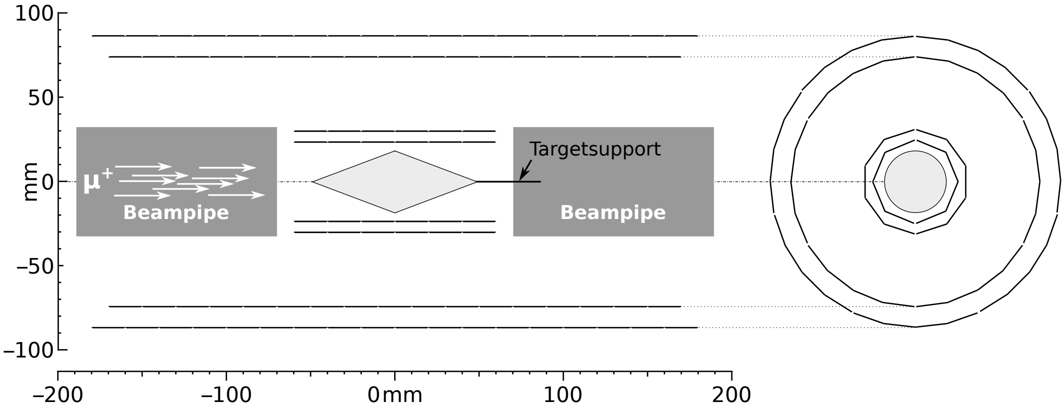
Stations distinguished by direction of muons entering the experiment.

Design status



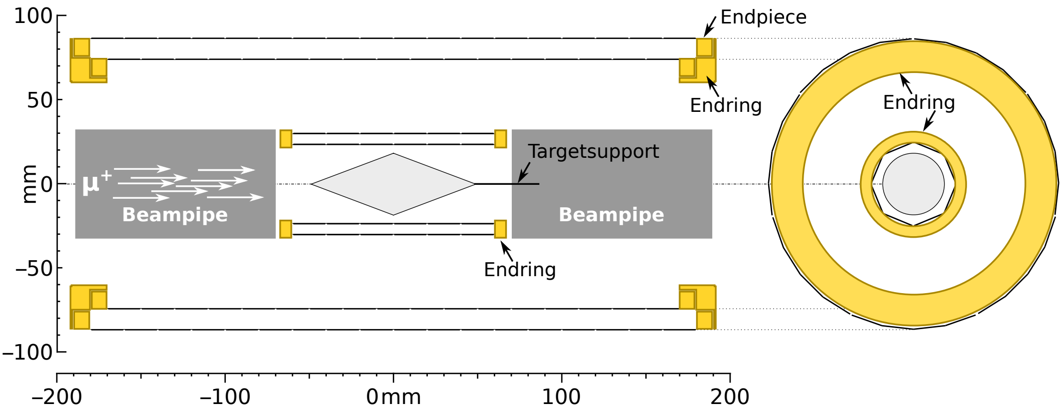
Let's go back to the central barrel.

Design status



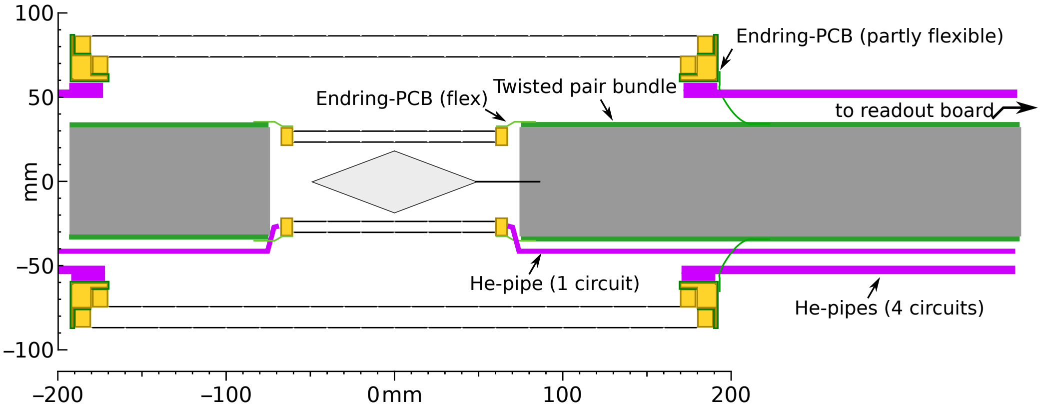
Add the beampipe. The target is fixed by a rod in the downstream beampipe.

Design status



The pixel barrels need some mechanical support, of course.

Design status



And some supplies: electrical connectivity and cooling circuits.

Design status – Pixel link counting

Central station:

Layer	Unit	units/layer	ladders/unit	chips/ladder	#chips	#links
1	half shell					
2	half shell					
3	module					
4	module					
Total						

Design status – Pixel link counting

Central station:

Layer	Unit	units/layer	ladders/unit	chips/ladder	#chips	#links
1	half shell	2				
2	half shell	2				
3	module	6				
4	module	7				
Total						

Design status – Pixel link counting

Central station:

Layer	Unit	units/layer	ladders/unit	chips/ladder	#chips	#links
1	half shell	2	4			
2	half shell	2	5			
3	module	6	4			
4	module	7	4			
Total						

Design status – Pixel link counting

Central station:

Layer	Unit	units/layer	ladders/unit	chips/ladder	#chips	#links
1	half shell	2	4	6		
2	half shell	2	5	6		
3	module	6	4	17		
4	module	7	4	18		
Total						

Design status – Pixel link counting

Central station:

Layer	Unit	units/layer	ladders/unit	chips/ladder	#chips	#links
1	half shell	2	4	6	48	
2	half shell	2	5	6	60	
3	module	6	4	17	408	
4	module	7	4	18	504	
Total					1020	

Design status – Pixel link counting

Central station:

Layer	Unit	units/layer	ladders/unit	chips/ladder	#chips	#links
1	half shell	2	4	6	48	144
2	half shell	2	5	6	60	180
3	module	6	4	17	408	408
4	module	7	4	18	504	504
Total					1020	1236

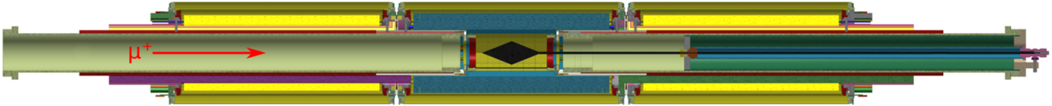
Design status – Pixel link counting

Central station plus two recurl stations:

Layer	Unit	units/layer	ladders/unit	chips/ladder	#chips	#links
1	half shell	2	4	6	48	144
2	half shell	2	5	6	60	180
3	module	6	4	17	1224	1224
4	module	7	4	18	1512	1512
Total					2844	3060

Design status

This is a cut view from the side:

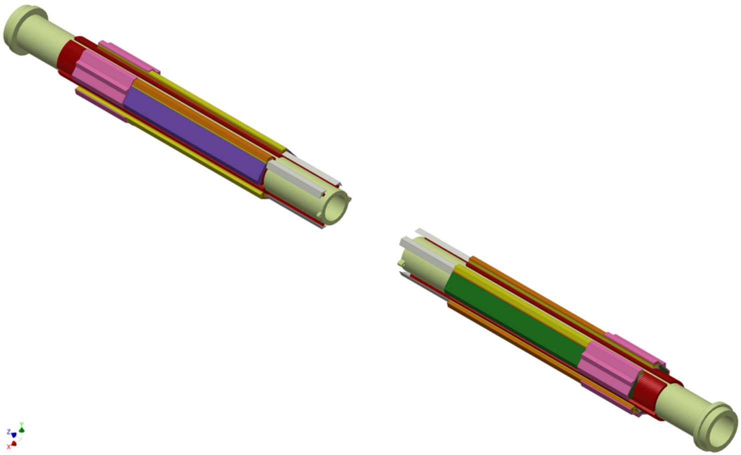


- Full CAD model, contains all parts at current design state.
- Includes cooling pipes, helium ducts, cabling for power, control and readout.
- Basis for simulation studies shown later.
- Will focus on some detail aspects.

Design status – Assembly procedure

- The following slides show a step-by-stepmounting procedure
- Order of sequence has certain freedoms. This is one possible choice.

Design status

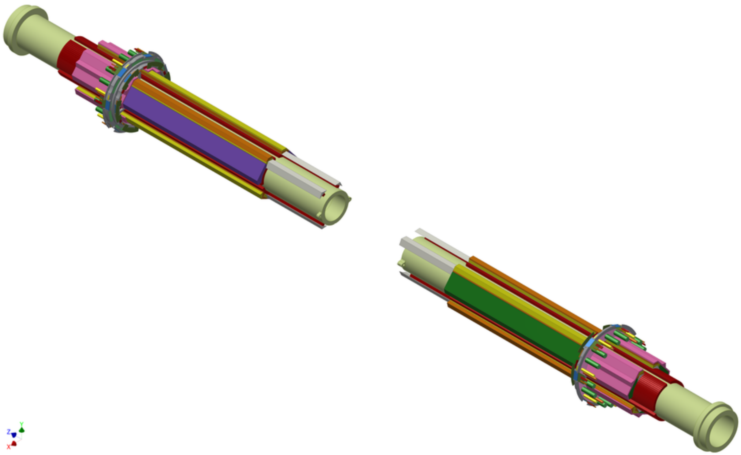


We start with the two beampipes.

Already mounted:
copper bars and helium ducts.

Two beampipes still allowed to be mechanically independent for first few steps.

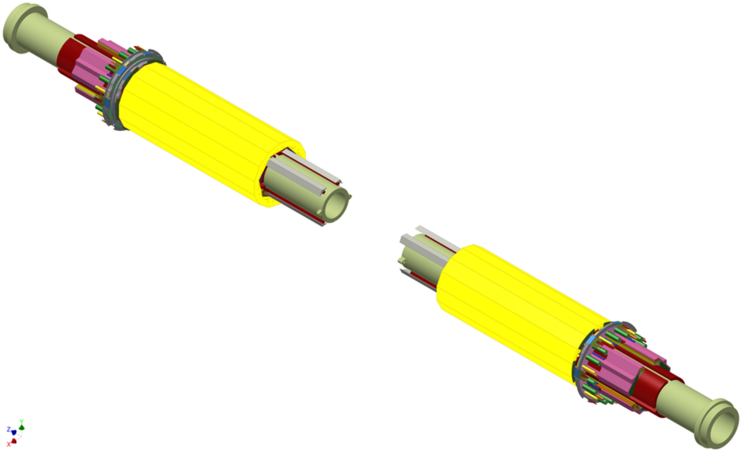
Design status



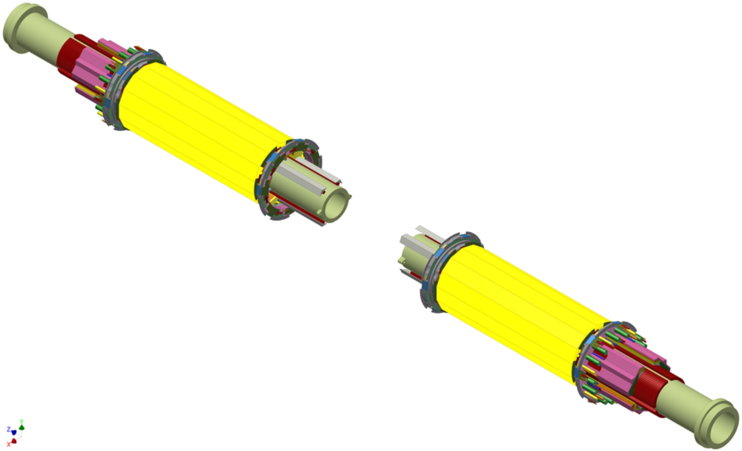
Outermost endrings

Design status

Tile detectors

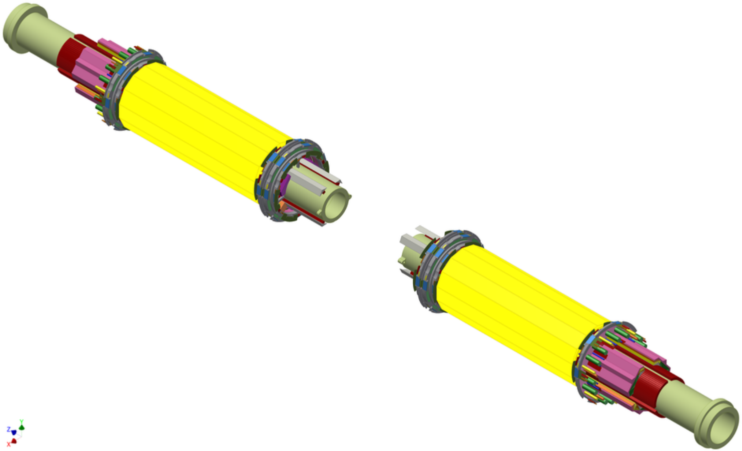


Design status



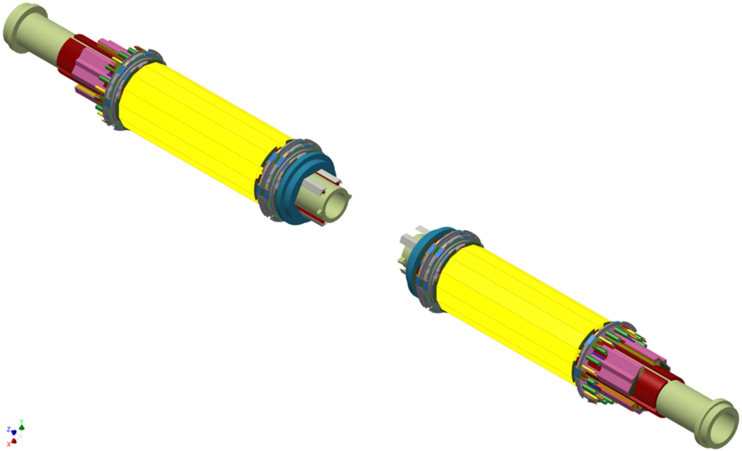
Second endrings for recoil stations

Design status



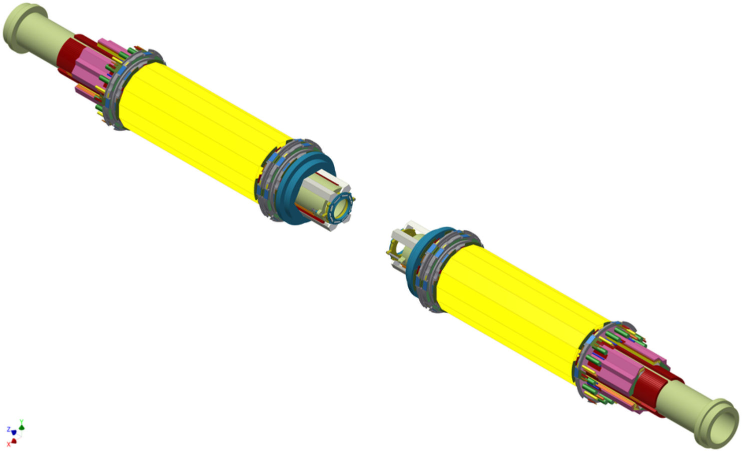
Endrings for central station

Design status



Mounting frame for SciFi

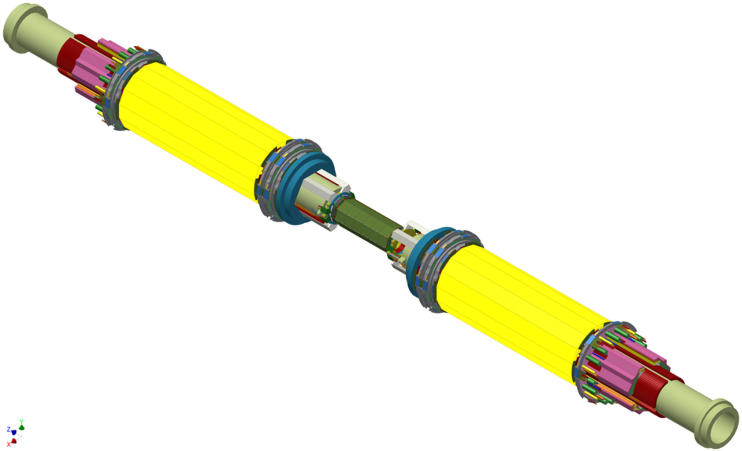
Design status



Endrings for L1/2

Note: Until now, no mechanical connection between US/DS.

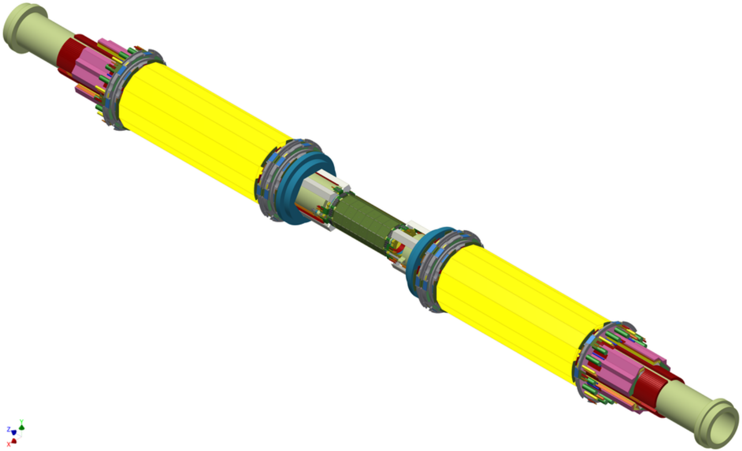
Design status



Two half-shells for L1

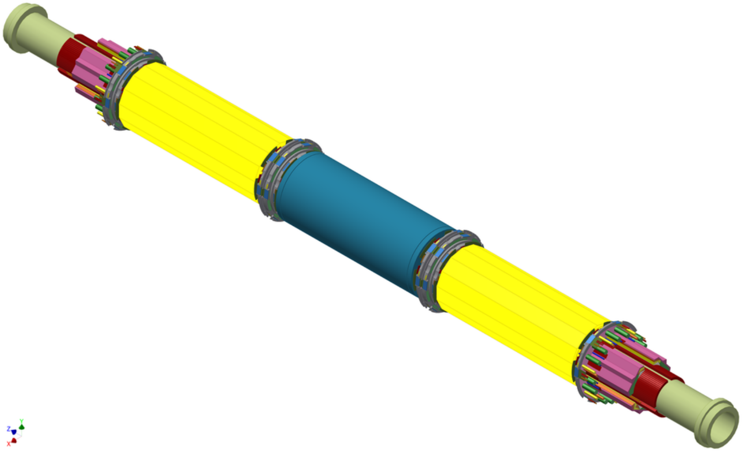
Note: From now on everything is in experiment frame and beampipes must be aligned.

Design status



and same for L2

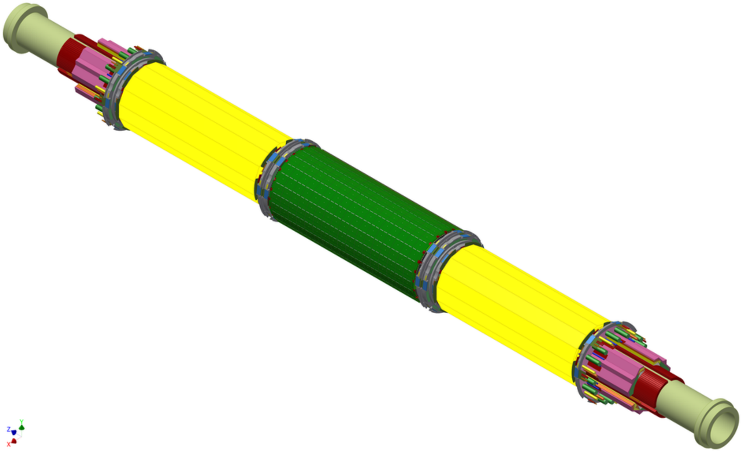
Design status



Insert SciFi modules

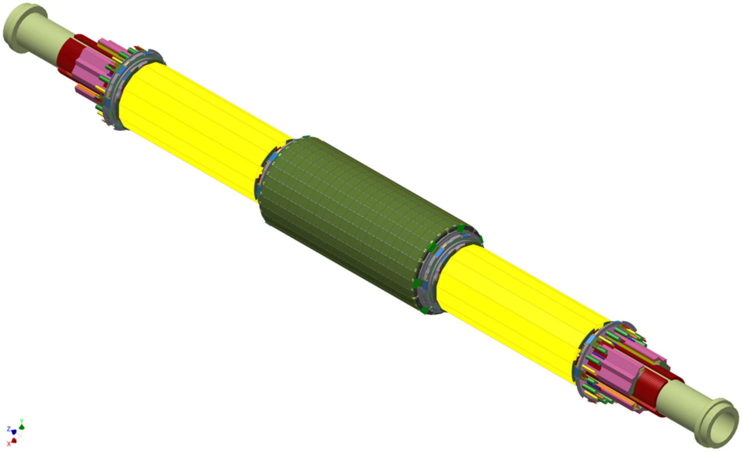
Design status

Insert pixel L3 modules



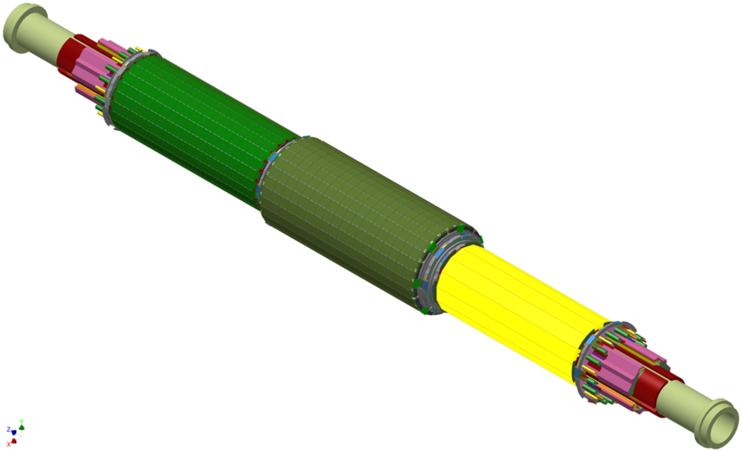
Design status

and L4



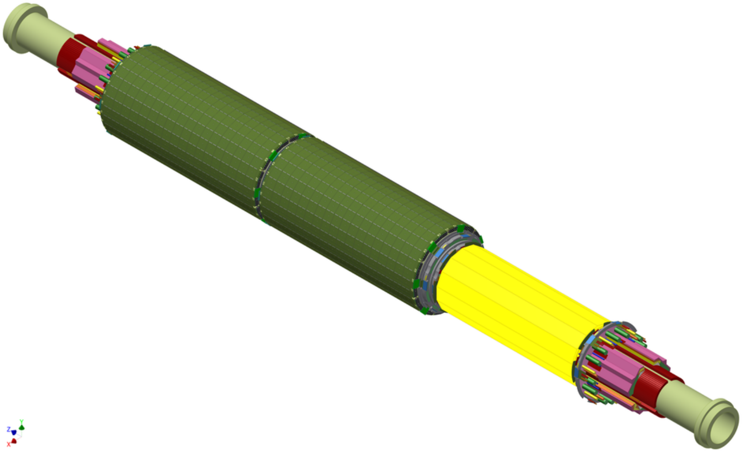
Design status

L3 of US recoil station



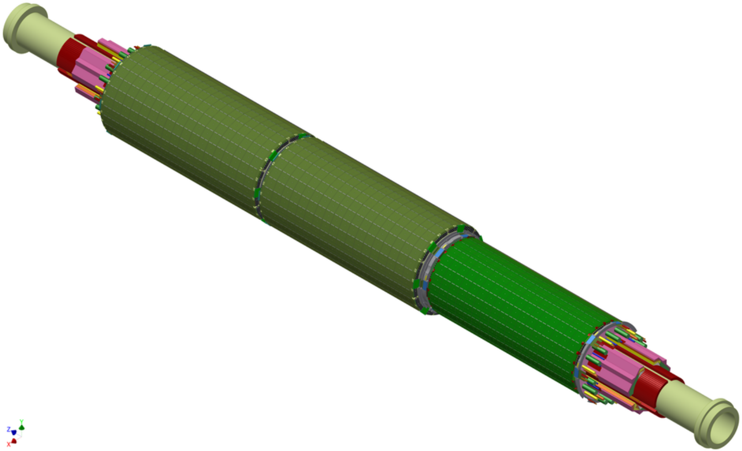
Design status

L4

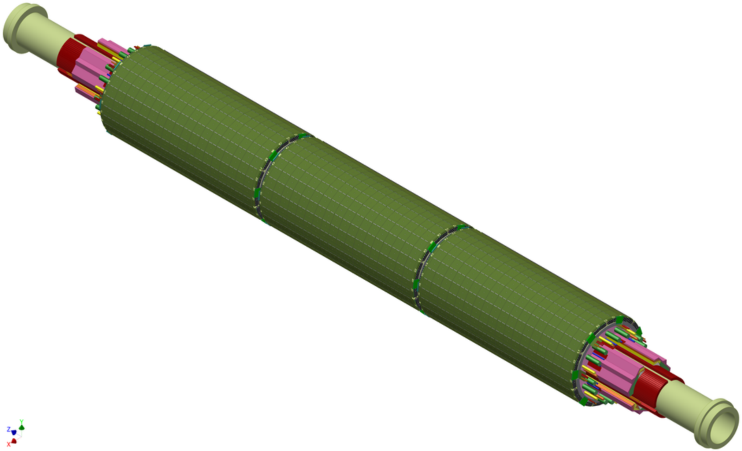


Design status

L3 of DS recoil station



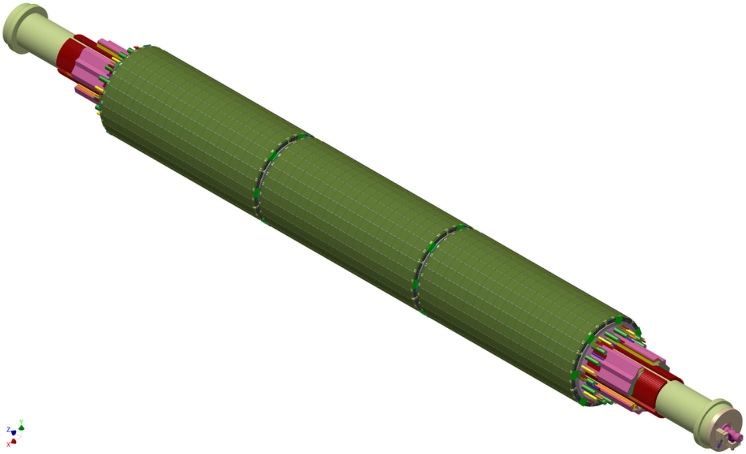
Design status



L4

Now detector is in principle ready for insertion into magnet.

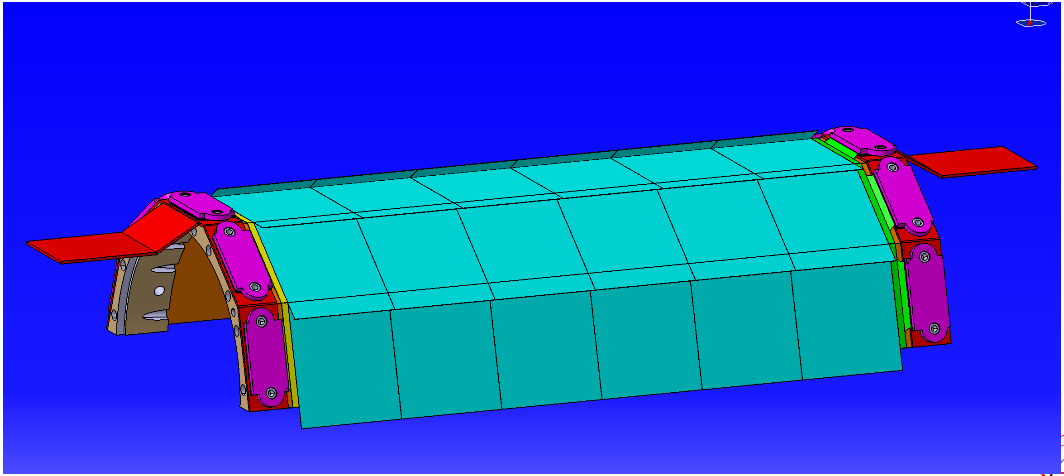
Design status



And finally: insert target from DS

Design status – Layers 1/2

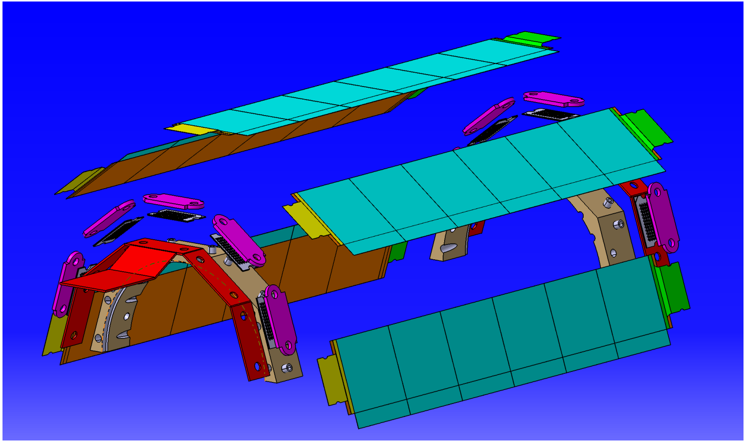
Modules layer 2 design (1 is similar, one facet less)



Inner modules have ladders of 6 chips each. Observe: No V-folds here.

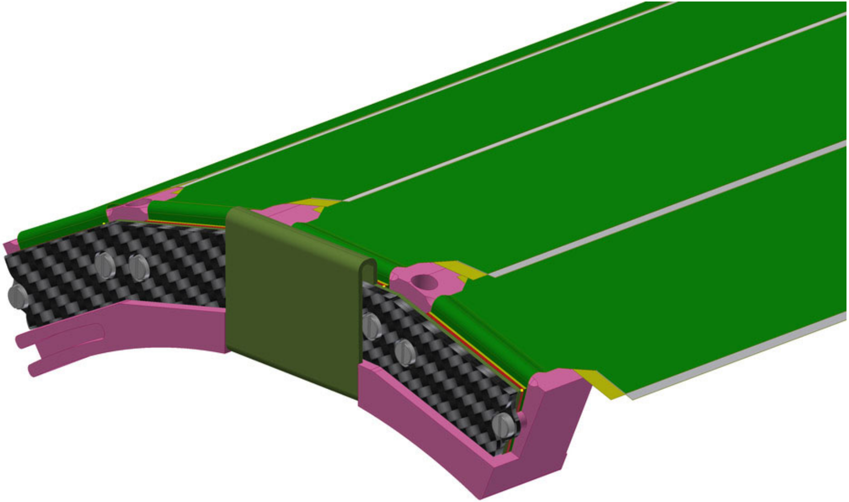
Design status – Layers 1/2

Modules layer 2 design (1 is similar, one facet less)

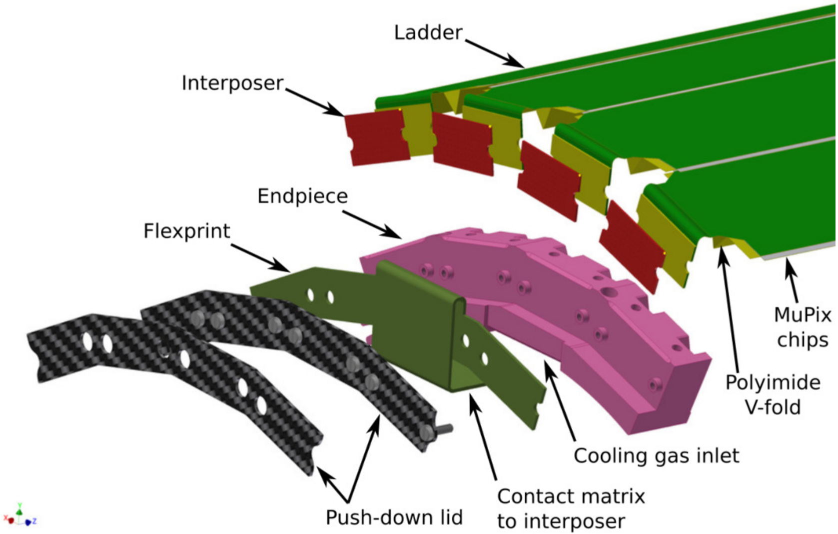


Exploded view of same part.

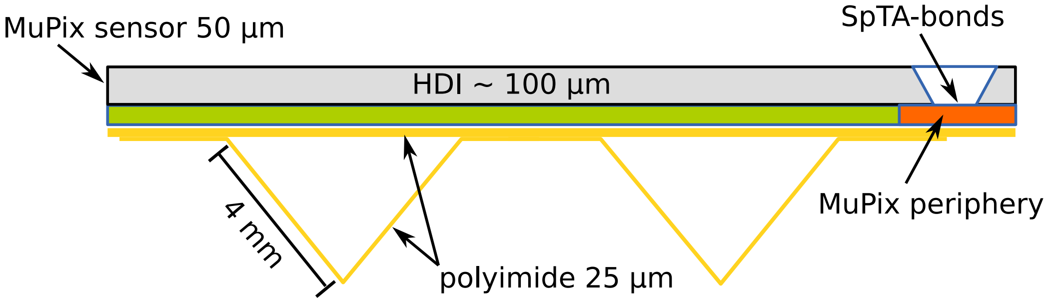
Design status – Layers 3/4



Design status – Layers 3/4



Design status



Radiation length: $\approx 0.1\% \, x/X_0$

Design status

- Design tested with 3d-printed parts and works well
- L4 endpiece also available in milled PEI and assembled to thermo-mechanical mock-up modules
- Assembly used final tooling

Design status – Supplies

- The detector needs power, signals to and from it, plus cooling.
- Every barrel needs supplies from both sides $\Rightarrow$ 2+6 sides.
- Outward facing sides of recurl stations easy.
- Others need to be routed along beampipes under tile detector.

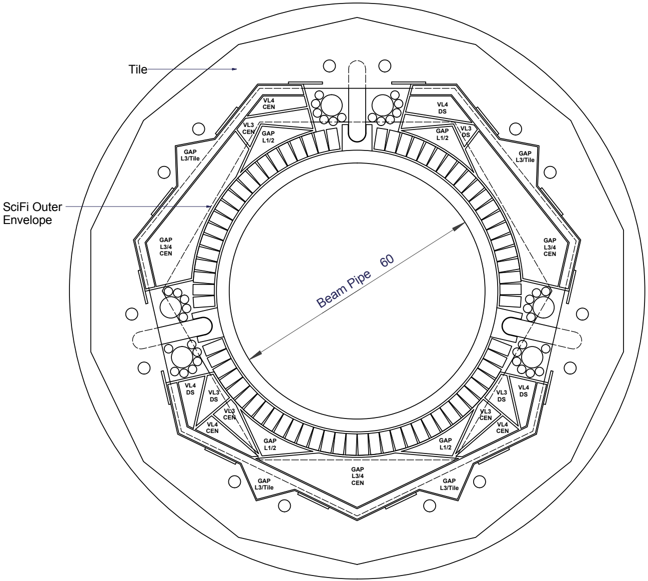
Design status – Supplies

Required target flows per helium circuit:

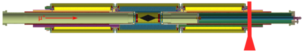
Volume	He flow speed m/s	Cross-section cm^2	Volume cm^3	Occurence times	Volumetric flow m^3/min
Gap L1/L2	10	12	148	1	0.72
Gap SciFi/L3	10	39	1320	1	2.3
Gap Tile/L3	10	34	1150	2	4.2
V-folds L3	20	3.3	114	3	1.2
Gap L3/L4	10	60	2185	3	10.8
V-folds L4	20	3.9	141	3	1.4
Global flow	0.5	7600	912000	1	23
Total		7750			43

$\Rightarrow$ Volumes differ up to factor ≈ 20

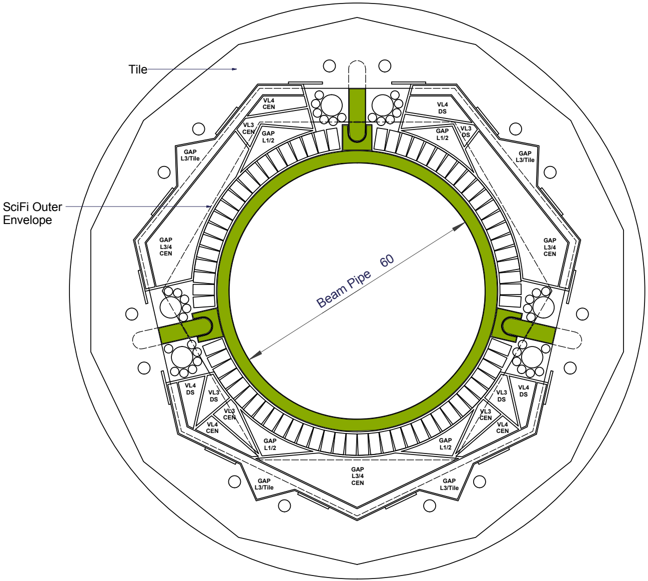
Design status – Supplies



Cross section of beampipe under one of the recurl stations.



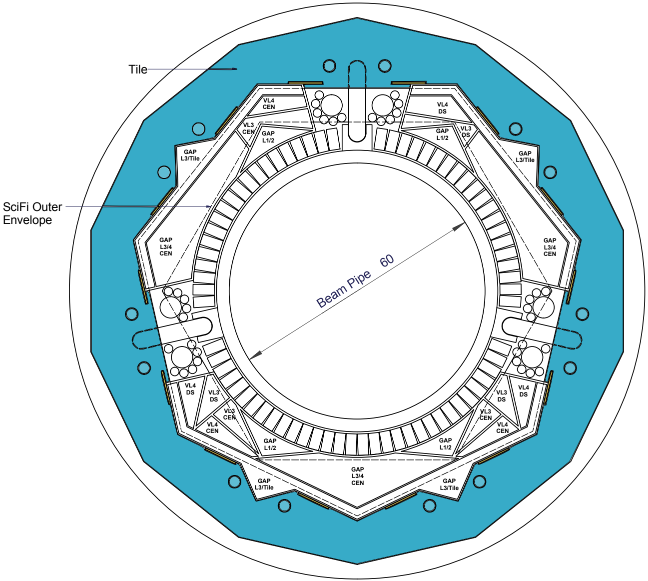
Design status – Supplies



This is the **beampipe**.

Major change: Round shape, no cooling grooves any more.

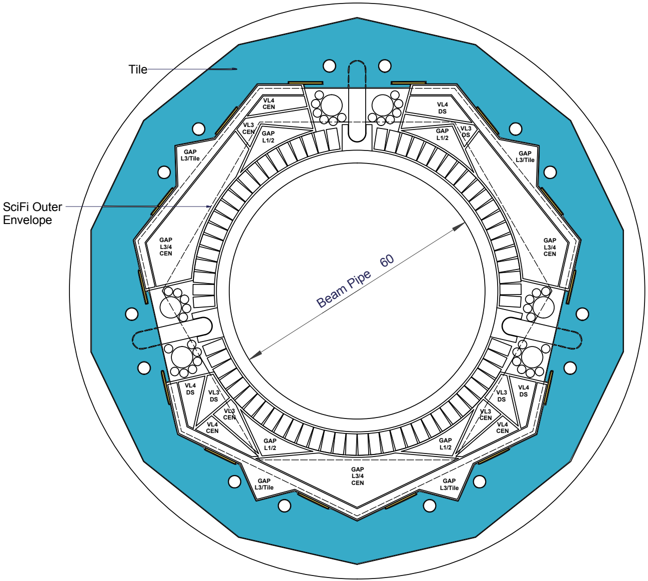
Design status – Supplies



Scintillating tile detector is here.

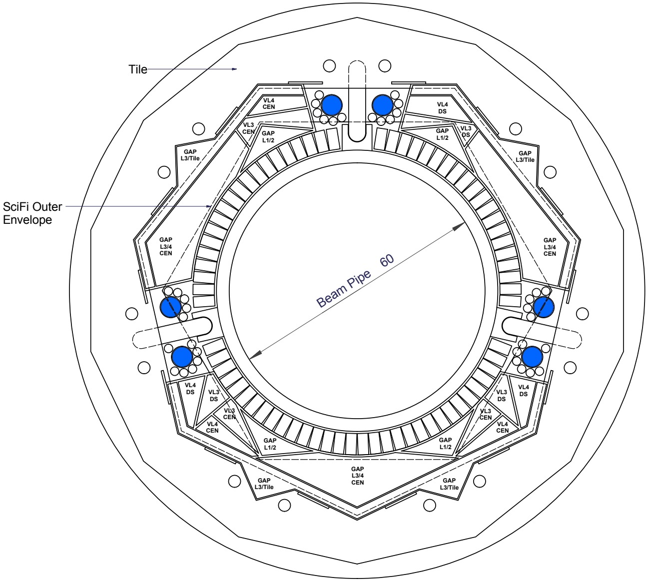
Al-frames became lower, tiles shortened by 0.5 mm to gain some space for He ducts.

Design status – Supplies



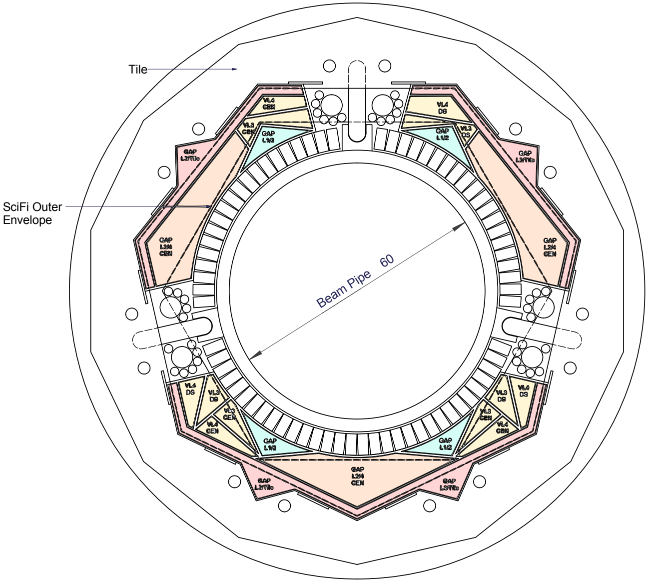
Cooling pipes for scintillating tile. . .

Design status – Supplies



... and cooling pipes for the scintillating fibres.

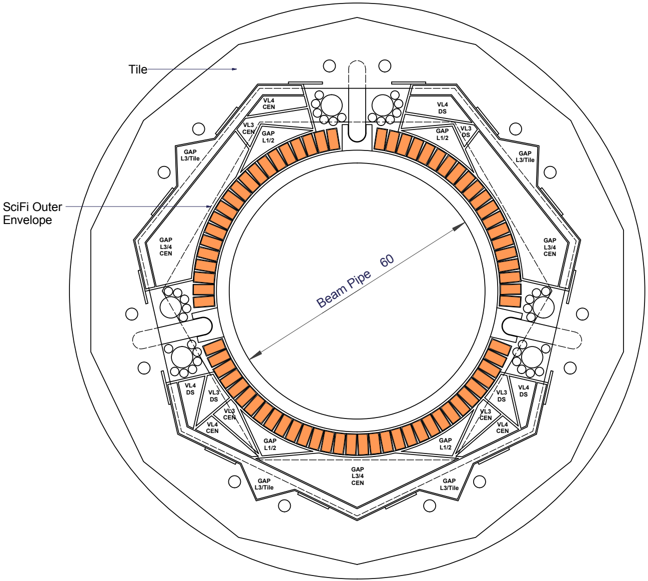
Design status – Supplies



Helium ducts. Shapes made from carbon fibre sheet material, cross-sections optimised for all sub-circuits.

Cross sections level flow speed to keep pressure drop similar for all duct. See simulation part.

Design status – Supplies

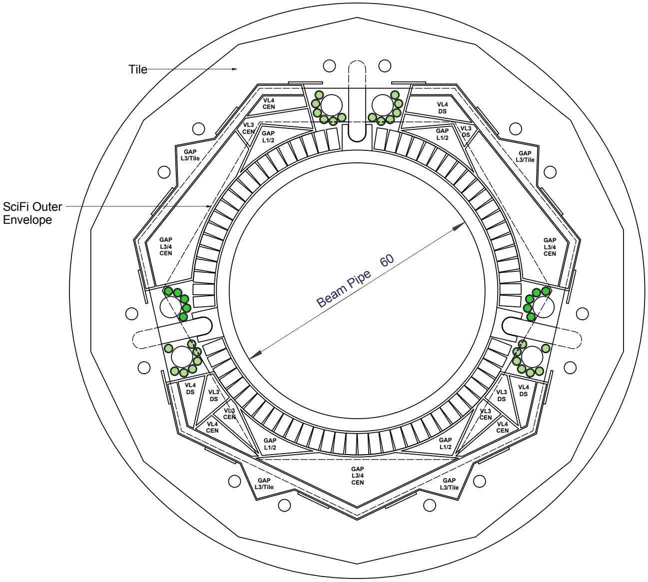


Copper bars for powering. 72 bars for 36 circuits.

Powers pixels (central station and two times one half of a recurl station) plus SciFi.

Power dissipation ≈150 W per side. Conductively cooled from outward facing end.

Design status – Supplies

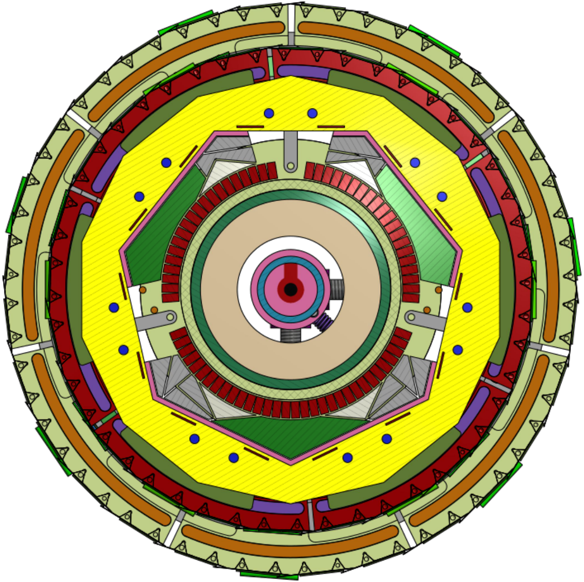


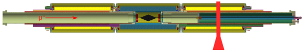
Signals now in bundles of 50 **twisted-pair cables**.

This is a lossy transmission line at lower impedance, requiring matched drivers and impedance matching.

Still pursuing use of flex cables with proper $Z_{\text{diff}} = 100\,\Omega$. Twisted pairs easier to mount, easier alternative.

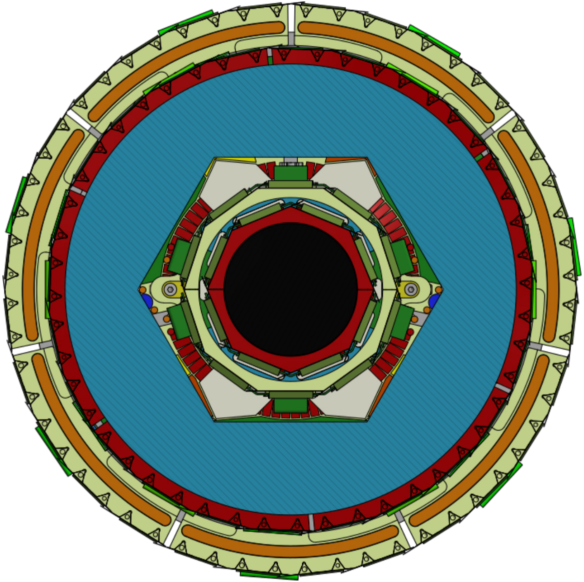
Design status – Supplies

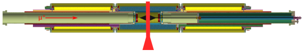




Similar cut inside SciTile

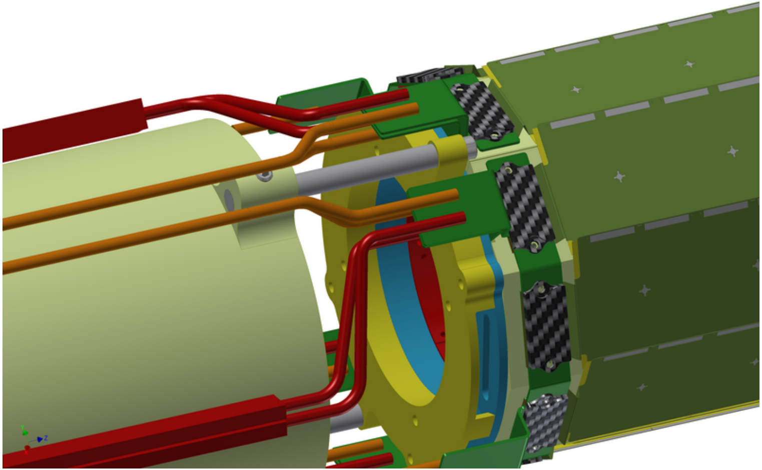
Design status – Supplies





Cut through target.
Observe: SciFi not in here.

Design status



A complete wiring scheme exists in CAD.

Example: Cabling L1/L2 one half shell

Orange: signals
Red: power/GND

Very time-consuming in CAD. Will build **cabling mock-up** this year.

Cooling simulations

Cooling simulations

- Cooling simulations have been repeated
- Two power dissipation cases:
  - 400 mW/cm^2 (pessimistic)
  - 250 mW/cm^2 (realistic)
- The two cases scale linearly, hence show 400 mW/cm^2 only
- Also pressure drop across ducts and detector volumes have been simulated

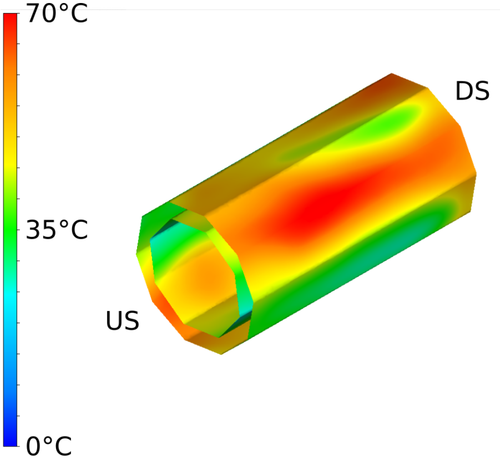
Cooling simulations

Simulated flows:

Volume	Flow speed (m/s)	Direction
Gap L1/L2	10	DS $\rightarrow$ US
Gap SciFi/L3	5	US $\rightarrow$ DS
V-folds L3/L4	20	DS $\rightarrow$ US
Gap L3/L4	10	DS $\rightarrow$ US
Global	0.5	US $\rightarrow$ DS

Following pages show temperature of silicon as heat maps. Other parts removed for clarity.

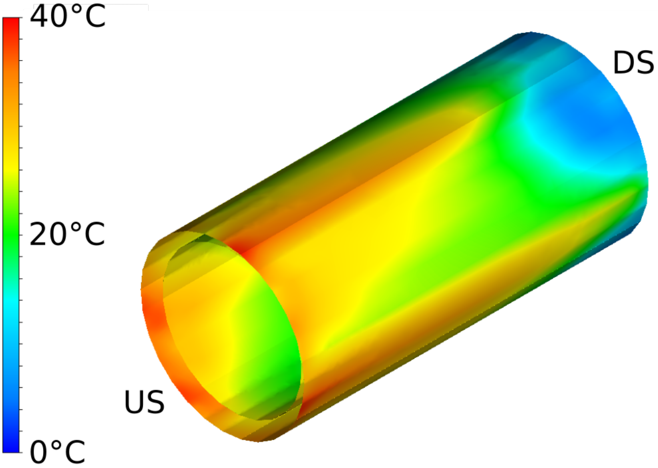
Cooling simulations



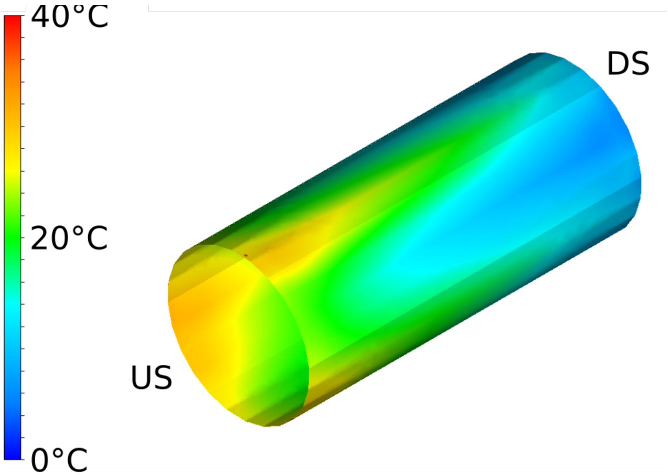
L1/2

Cooling simulations

L3/4



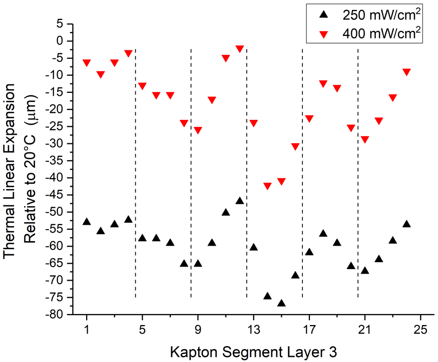
Cooling simulations

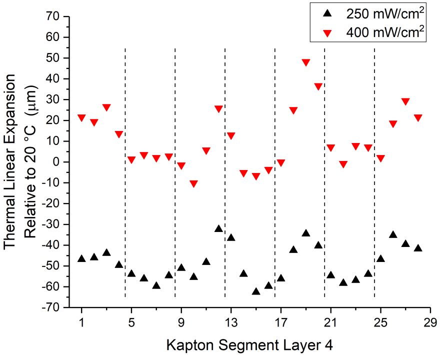


L3 only

Cooling simulations

Average temperature of ladder translated into thermal expansion of polyimide:





Note: This is a result calling for more studies. Plan is to optimise gas inlets. Interplay with duct layout, hence non-trivial.

Cooling simulations

Expected **pressure drops** in the circuits from same simulation:

Circuit	Duct IN	Flange	**Detector**	Flange	Duct OUT
Gap L1/L2	25	7	$< \mathbf{1}$	9	24
Gap SciFi/L3	6	< 1	**3**	28	–
V-folds L3	25–50	80–90	**10–20**	50–70	25–25
Gap L3/L4	8	25	$< \mathbf{1}$	11	–
V-folds L4	30–50	60–70	**10–20**	50–70	20

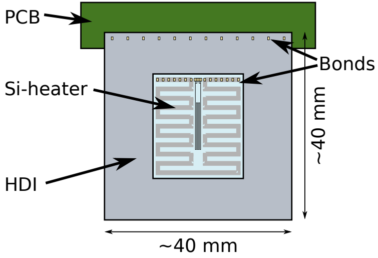
All pressure values in mbar. If range given: min/max observed per compartment.

Some gaps vent to global volume.

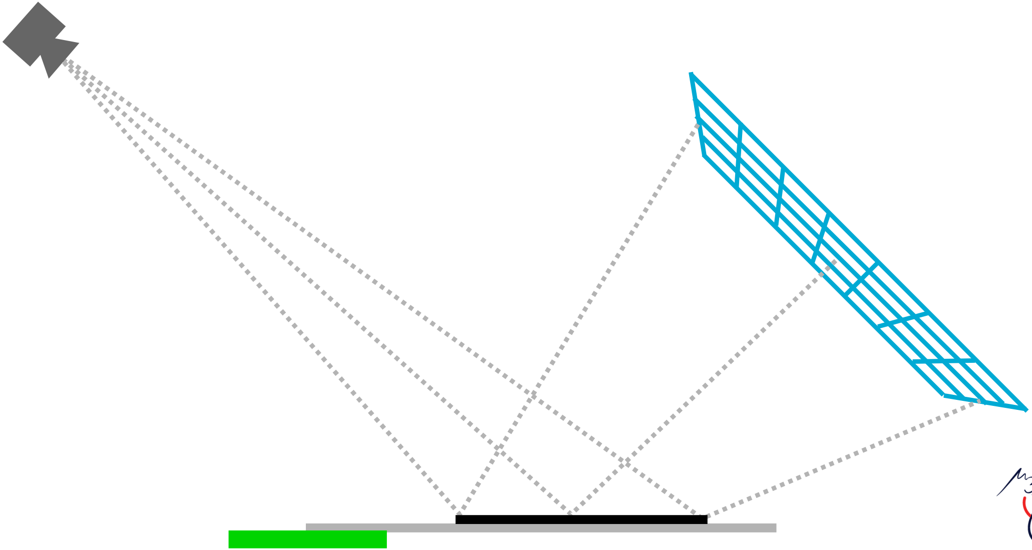
This seems manageable and the detector shouldn't „pump up".

Cooling simulations

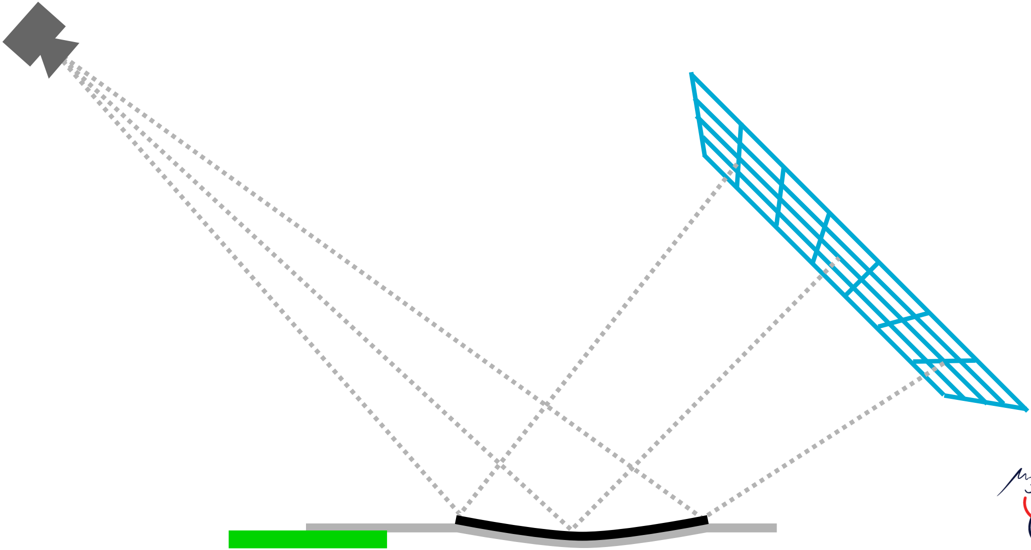
- We've prepared single silicon heater assemblies.
- Consists of heater (sputtered aluminium on silicon, thinned down to 50 µm) and a flex HDI (2 layers Al/polyimide). **Veryclose to final design.**
- Heater designed to dissipate up to 400 mW/cm^2.
- Has a 1000 Ω RTD on it
- Next set of slides: graph paper viewed reflected on back of silicon heater



Cooling simulations

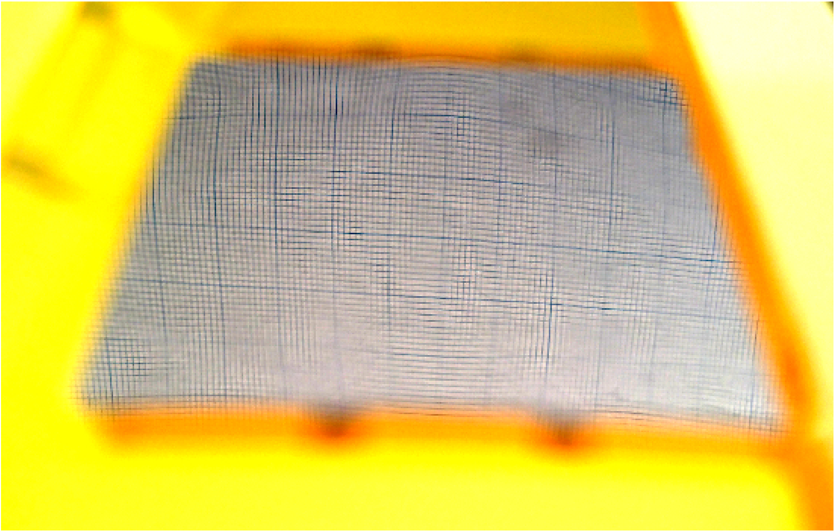


Cooling simulations



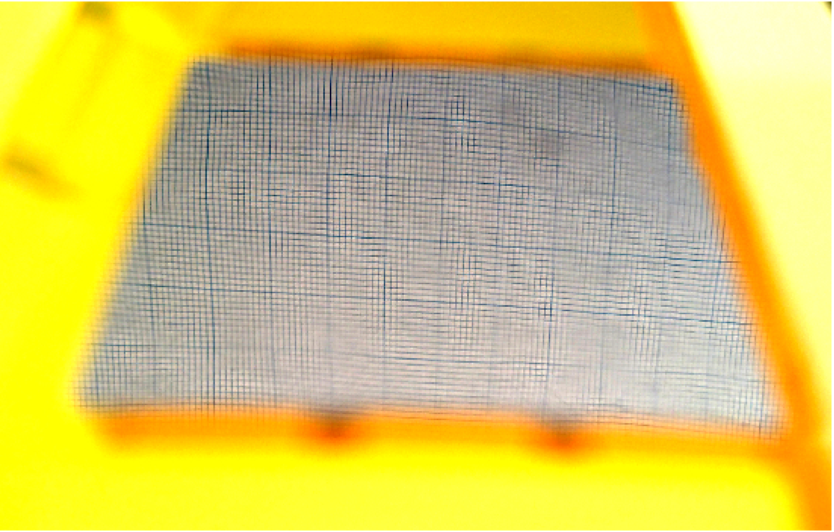
Cooling simulations

$\vartheta = 30\,°C$



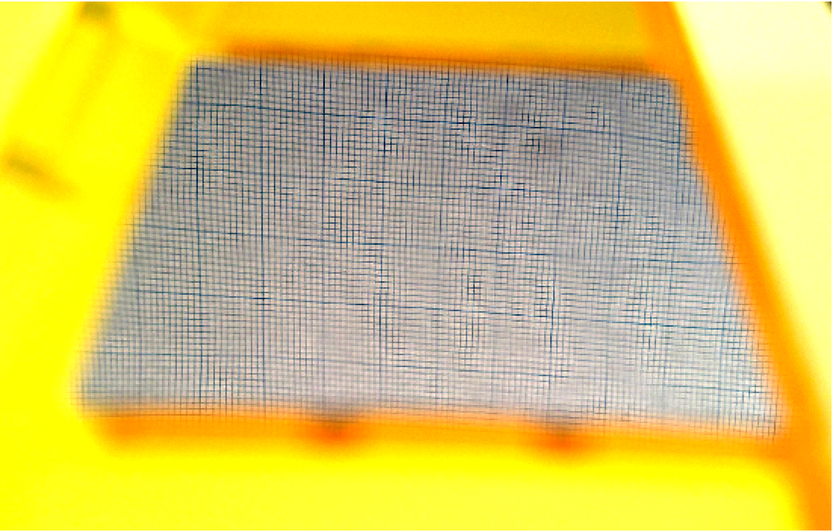
Cooling simulations

$\vartheta = 40\,°C$



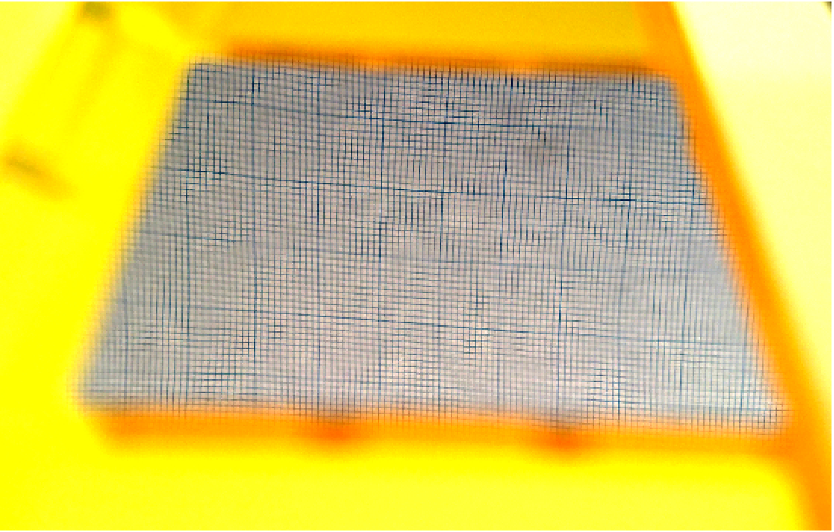
Cooling simulations

$\vartheta = 50\,^{\circ}\mathrm{C}$



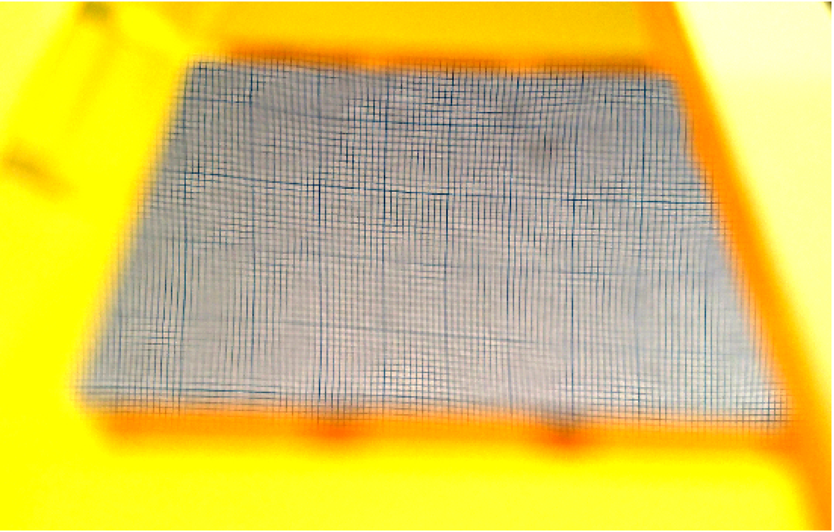
Cooling simulations

$\vartheta = 60\,^{\circ}\mathrm{C}$

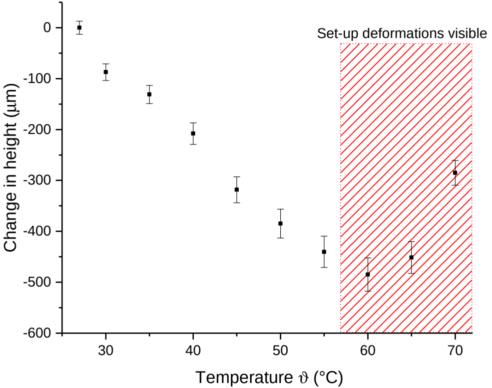


Cooling simulations

$\vartheta = 70\,°C$



Cooling simulations



Error bars show systematic error

Before you get too shocked:

- About the magnitude expected from **CTE mismatch polyimide-silicon**.
- Glue pattern has **not been optimised** yet.
- Will calibrate finite element simulations and optimise glue pattern in simulation.
- If detector is in thermal equilibrium and stable over time, **track-based alignment can handle this**.
- Thermal mass is small, hence equilibrium will be reached fast.

Cooling simulations

- Volume between L3 and SciFi has been added compared to earlier simulations
- Temperature distribution looks fine
- Pressure drops are fine
- Thermal expansion of ladders within module not evenly distributed. Optimisation process ongoing and believed to be solvable.

Mock-up preparation

Mock-up preparation

- Thermo-mechanical mock-up in preparation, first parts dropping in.
- Cabling mock-up planned, CAD model already looks doable.
  This will allow to revisit use of flex prints instead of twisted pair cables
- Modules will also be made using silicon heaters
- Will test all critical components of modules except the MuPix chip

Schedule

Schedule

Milestone	Quarter
Cabling mock-up	Q2/18
Finalising design for all detectors	Q3/18
MuPix9 characterisation	Q2/18
MuPix10 submission	Q3/18
MuPix10 characterisation	Q2/19
Thermo-mechanical mock-up, production process development	Q3/18
Test setup and plans for ladder/module testing	Q3/18
Single chip testing / wafer probing	Q1/19
Demonstrator modules with final MuPix (MuPix10 is critical)	Q3/19
Production process readiness	Q4/19
Production	Q1/20
Subdetector ready for integration	Q2/20

Further readout aspects discussed in detector integration talk.

Conclusions

Conclusions

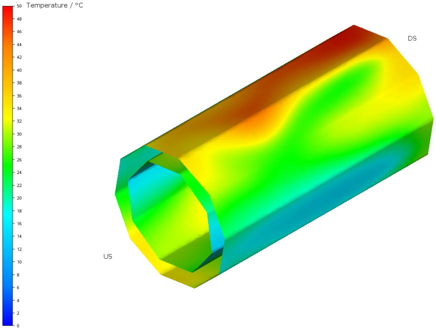
- **MuPix8 is performing very well** allowing us to move on. MuPix10 is planned for this year.
- Design well advanced, **module manufacturing** started with parts for thermo-mechanical mock-up.
  Will allow to verify thermal simulations.
- Cabling and He cooling duct puzzle solved, **mock-up** planned.
- **Chip remains the most critical component**.
  (Chip turnaround at foundry caused severe delays in the past already.)

ENCORE

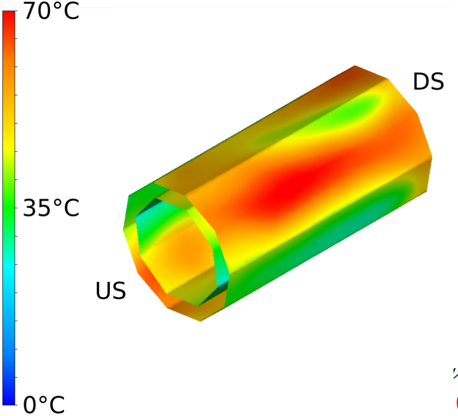
Cooling simulation realistic/pessimistic

L1/2

250 mW/cm^2



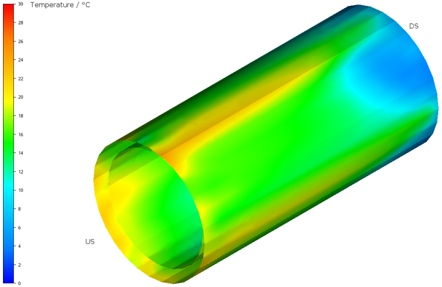
400 mW/cm^2



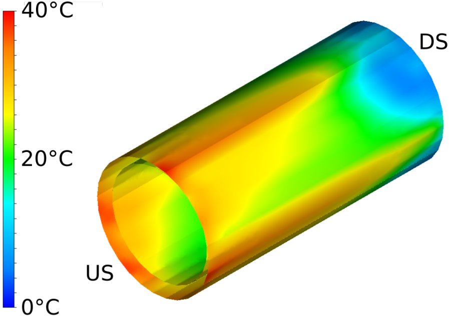
Cooling simulation realistic/pessimistic

L3/4

$250\,\mathrm{mW/cm^2}$



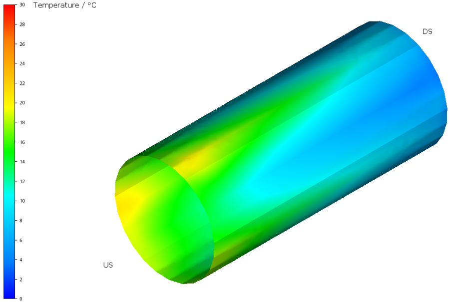
$400\,\mathrm{mW/cm^2}$



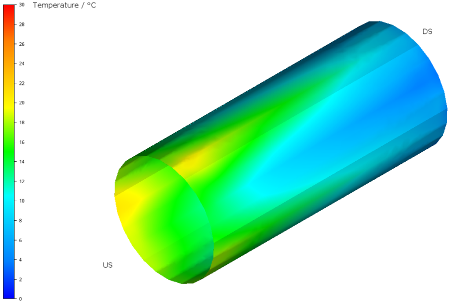
Cooling simulation realistic/pessimistic

L3 only

250 mW/cm^2

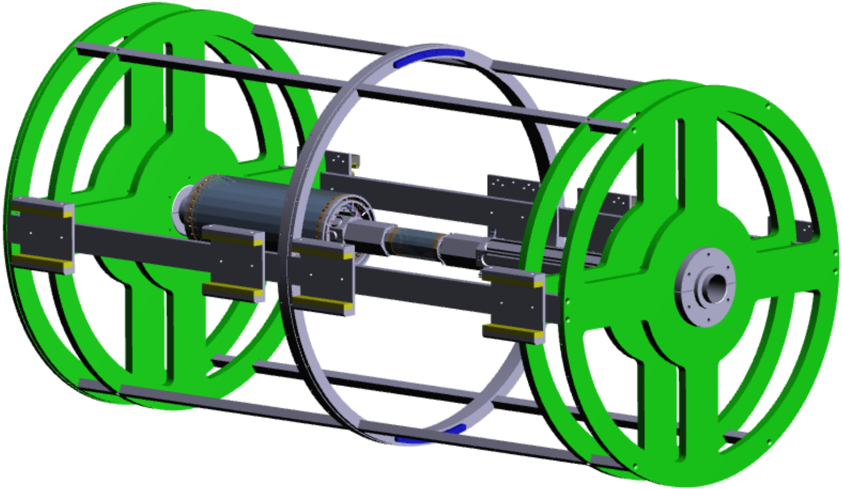


400 mW/cm^2



Module fabrication

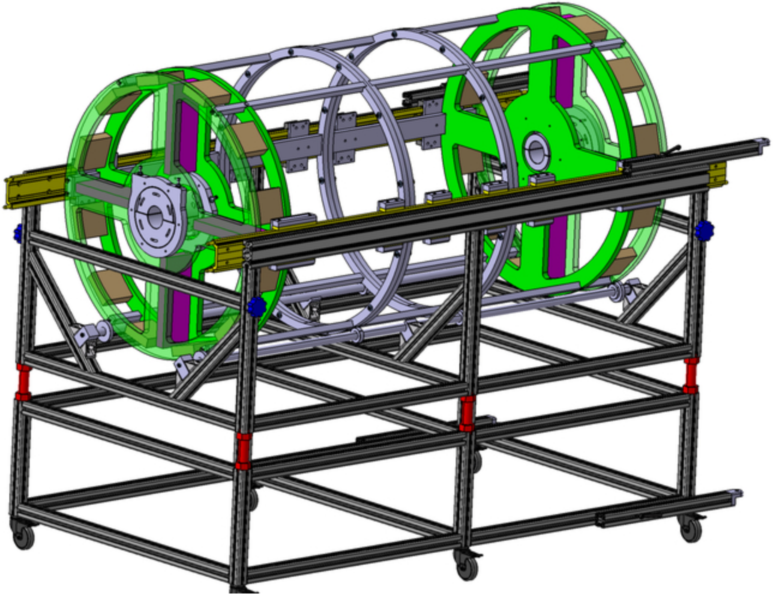
An „experiment cage“ acts as the mechanical frame holding both beampipes in position and houses the supplies:



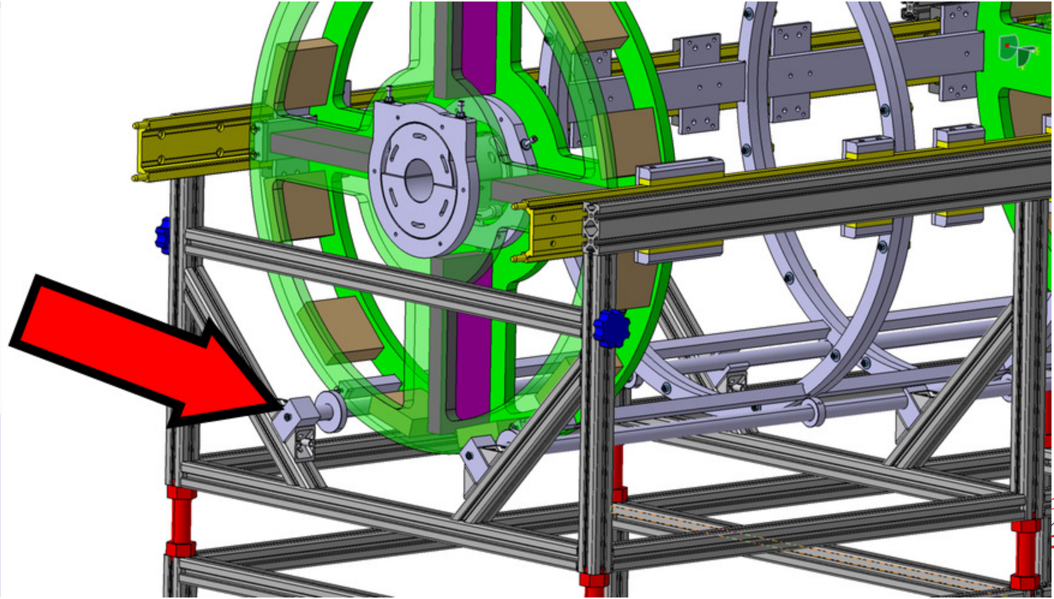
Module fabrication

- Prototype exists where the rings were made with PVC intead of GFK (glass fibre reinforced polymer).
- PVC is much cheaper but has less stiffness.
- Mounting shafts for beampipes allow for precise adjustments of beampipes in pointing angle and (small) rotations around z
- Beampipe (end) dip by less than 1 mm under a load of 10 kg attached to the loose end.
- FE simulation started to predict situation with GFK and develop stiffening strategy.
- Current detector design has loose bearings and can handle a dip up to 1 mm but less is preferred.
- Especially crucial because during mounting, the detector will be rotated around the z-axis.

Module fabrication



Module fabrication

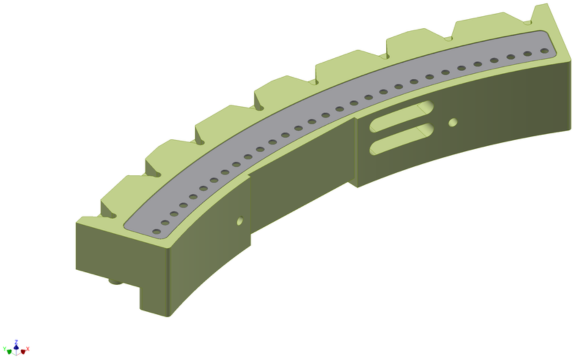


Module fabrication

Few comments beforehand:

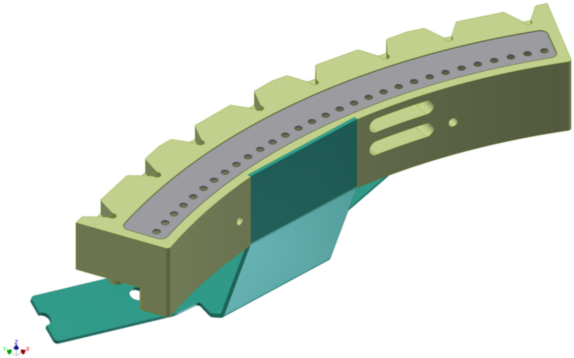
- Shown with drawings of L4. L3 is similar.
- There are tools for this, which are not shown. Emphasis is on bare procedure.

Module fabrication



Take endpiece. Glue gas cavity lid.

Module fabrication

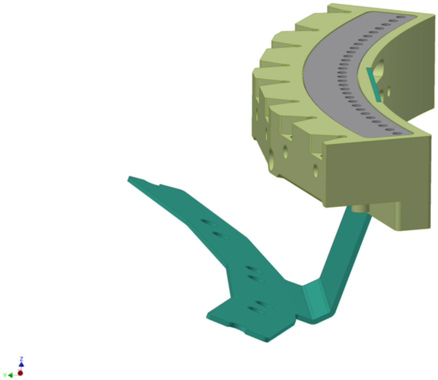


Pre-fold flexprint, glue it to endpiece. Let glue cure.

Note: Flexprint has nothing mounted on it. All you see are traces and the BGA-arrays.

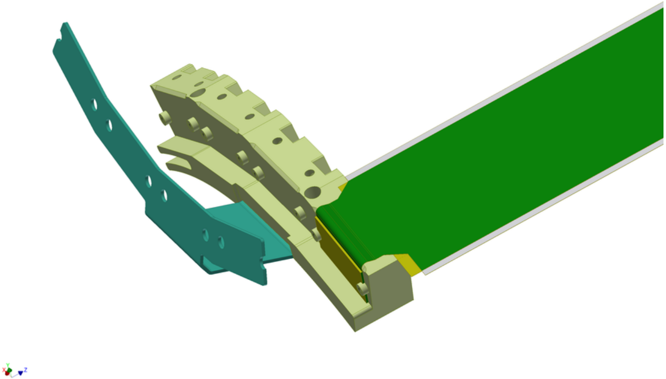
Gluing must be to precision $< 100\,\mu m$ w.r.t. endpiece reference.

Module fabrication



Turn it and . . .

Module fabrication

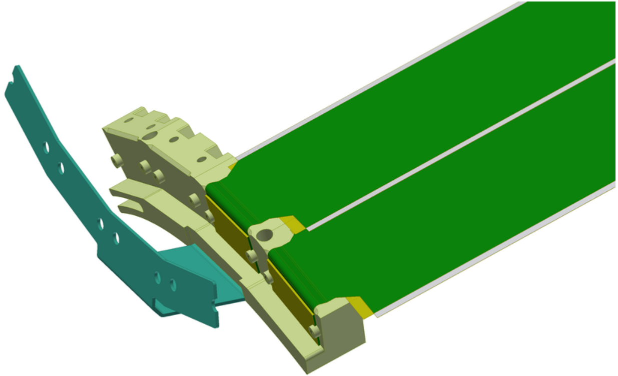


. . . place it on mounting jig (not shown). Secure with two screws (big holes).

Apply glue, place first ladder.

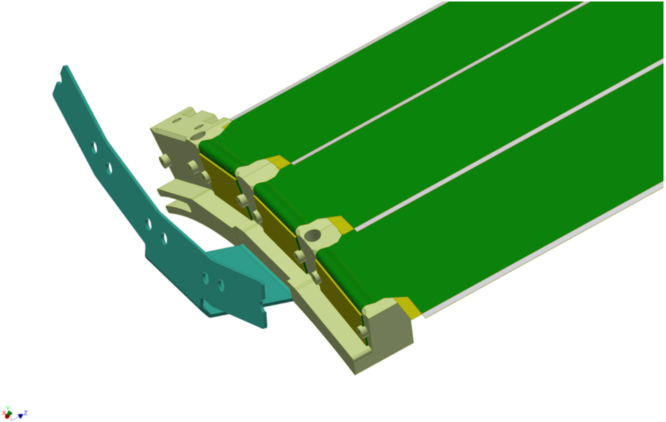
Remember: Ladder has a small flex at both ends with BGA array for interposer.

Module fabrication



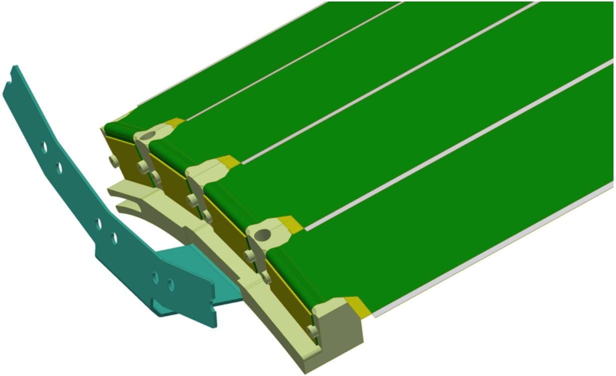
Repeat for second ladder. . .

Module fabrication



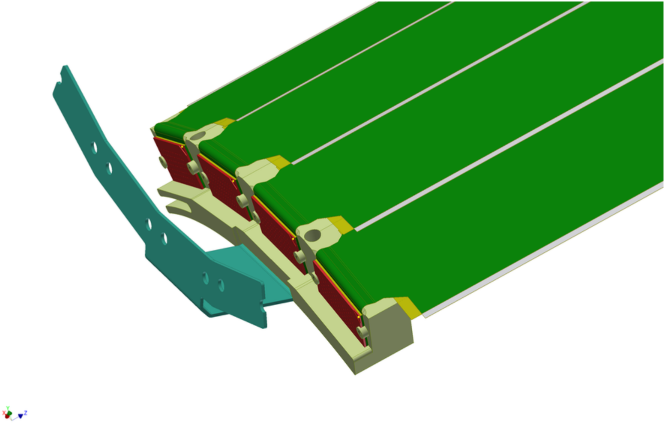
. . . third, and. . .

Module fabrication



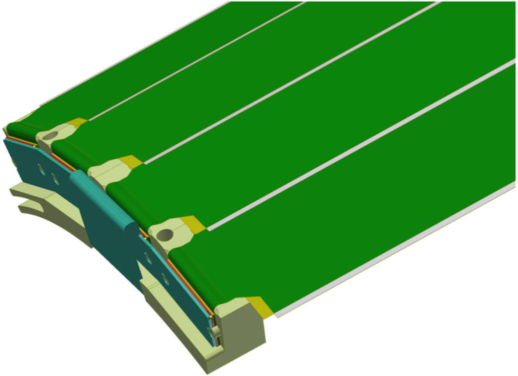
fourth ladder.

Module fabrication



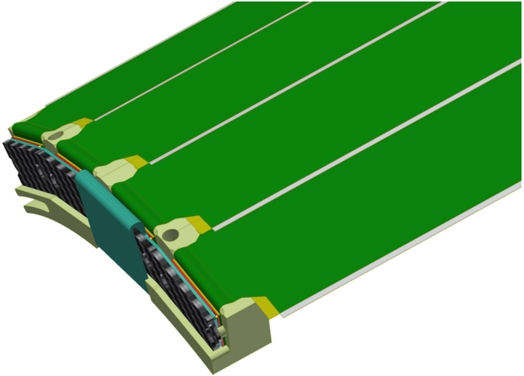
Place interposer (4 times).

Module fabrication



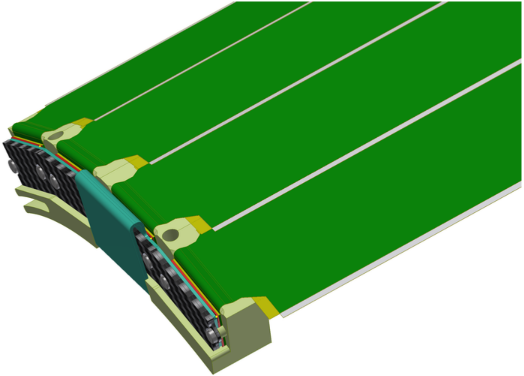
Fold in flexprint.

Module fabrication



Add compression bar (slides in from left under hair-pin loop)

Module fabrication



Secure everything with screws, 8 in total.

Seal V-folds from back side.

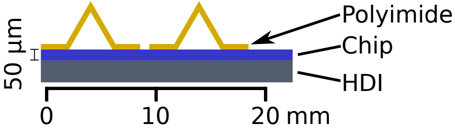
Ladder fabrication: gluing of V-folds

Process steps or tools in need of some improvements (A: asap, B: important, C: nice-to-have)

- **Curing weight** (A). To be made of silicone rubber. Sketch exists. UHD can do that but fine if others pick up (we will not use it...). So far we used metal weights but glue
- **V-fold suction bar** (B). Currently made with sintered aluminium. Sometimes suction not everywhere ok. Solid Al bar with row of small holes (i.d. 0.7 mm or slightly bigger) could be an advantage.
- **V-fold machine sometimes produces waves** (B). Usually fixed by pulling more, but reason not understood. Position of blades could be optimised.
- **Thinner polyimide** (C). Currently we use 25 μm thickness. Thinner material is available but hasn't been tested.
- **Helium leak test** (B). Ladders should be tested for leaks after gluing. Small rubber pieces with cutouts, measure flow and pressure drop? Visual inspection is also important. Maybe add dye to Araldite (traces of Methylene blue or Fluoresceine, . . .) for better visibility

Ladder fabrication: gluing of V-folds

Let's have a look at gluing V-folds on ladders. This is the outcome:

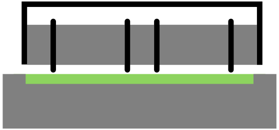


Ladder fabrication: gluing of V-folds

1.

Fill reservoir
with 50 µm
layer of glue

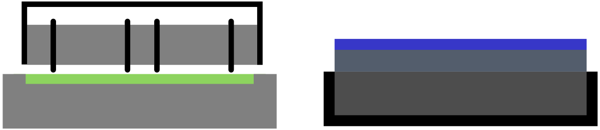
Ladder fabrication: gluing of V-folds



2.

Dip stamp
into reservoir

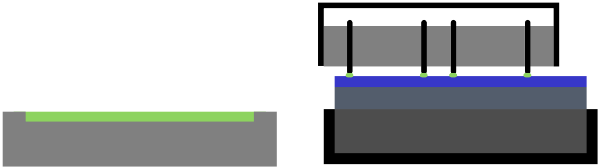
Ladder fabrication: gluing of V-folds



3.

Place bare
ladder on jig

Ladder fabrication: gluing of V-folds



4.

Apply glue

Ladder fabrication: gluing of V-folds

5.

Place V-folds
on jig

Ladder fabrication: gluing of V-folds

5.

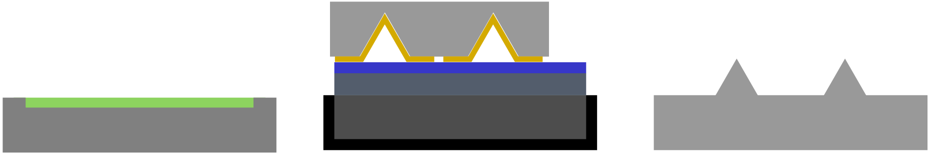
Place V-folds on jig

Ladder fabrication: gluing of V-folds

6.

Pick V-folds

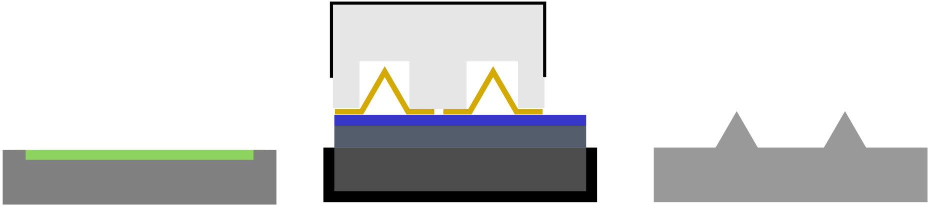
Ladder fabrication: gluing of V-folds



7.

Lower V-folds down

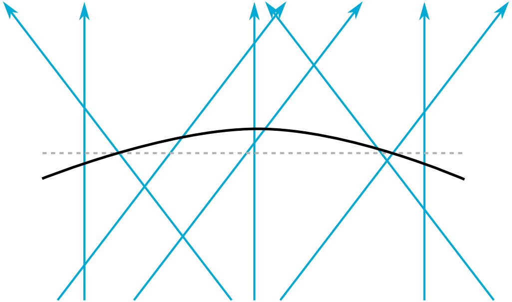
Ladder fabrication: gluing of V-folds



8.

Place curing weight
Let glue cure

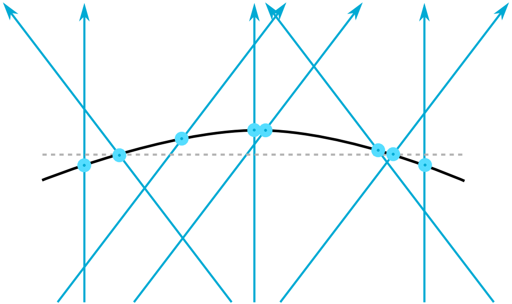
Alignment –



Consider a bent detector chip.

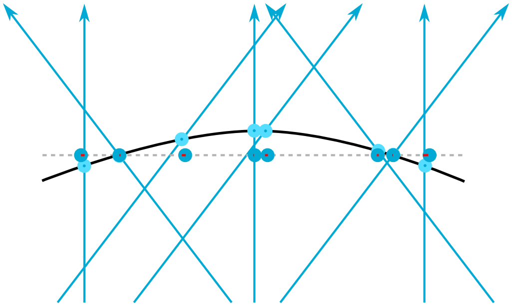
Multiple tracks have been recorded at different positions and with various track angles.

Alignment –



The chip records hits at the real position. . .

Alignment –



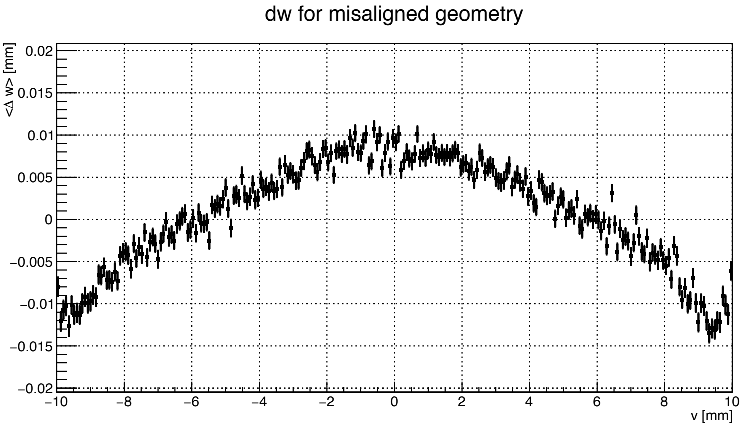
. . . but if you didn't take this into account, you assume different positions.

This leads to substantial residuals, e.g. for a 45° track and a 100 µm deformation this is a residual of 100 µm, more than a pixel pitch.

Global track algorithms have proven to be sensitive to much smaller deformations (e.g. arXiv 1010.2039).

Alignment

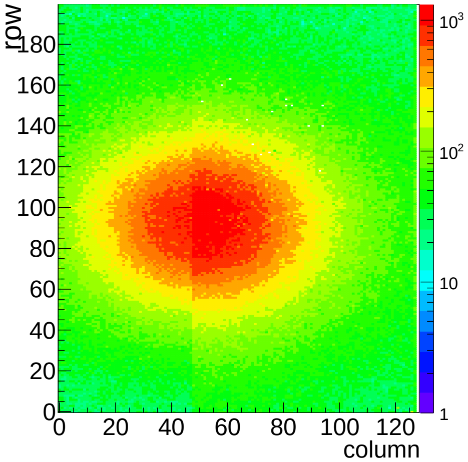
Residual plot for a deformed MuPix chip:



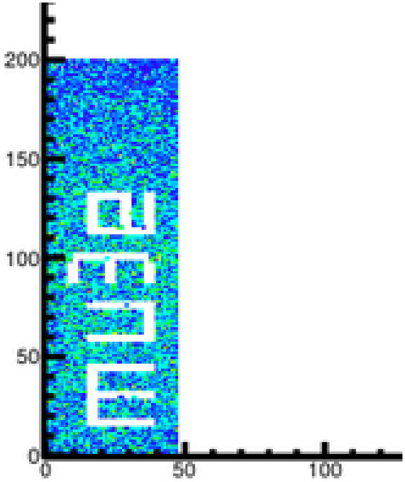
Result obtained using Mu3e track reconstruction and geometry.

MuPix8 –

MuPix8 hitmap, Sr-source



MuPix8 –



MuPix8 pixel masking demo

MuPix8 –

Timewalk and time over threshold (ToT)