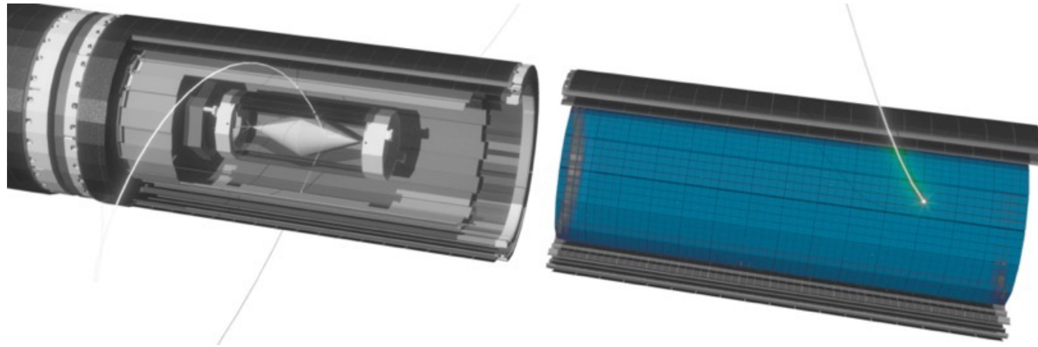
Tile Detector

BVR 49, PSI
February 12, 2018

Yonathan Munwes on behalf of the Tile Detector group



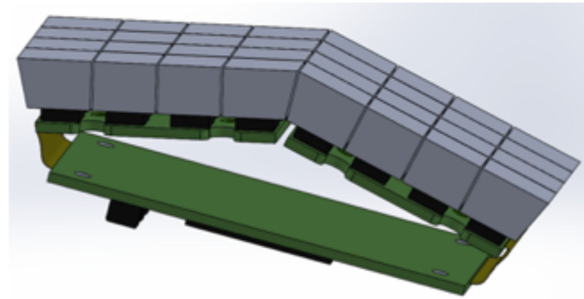
Requirements

- Detection efficiency close to 100%
- Time resolution better than 100 ps
- Maximum hit rate up to 60 kHz/channel
- Enough energy resolution for time walk correction

Background suppression factor

Tracker hits	Fibers	Tiles	Both
≧ 4	35	5.3	72
≧ 6	44	5.3	102

Detector Overview



<u>Submodule</u>

- In total 32 channel
- 3x3 mm^2 SiPMs
- FEBA – flex printed PCB
- MuTrig ASIC in BGA package
- Scintillator tiles Ej-228
  ~6.5x6.5x5 mm^3 , two type (center and edge)
- ESR reflected foil, individual tile wrapping

<u>Moudule</u>

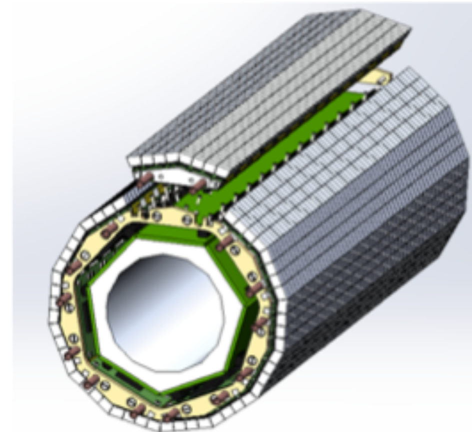
- 14 submodule mounted on the cooling structure
- Water cooling
- 448 channels

<u>Recurl station</u>

- 7 modules mounted on end rings
- Total length 368 cm
- 3136 channels

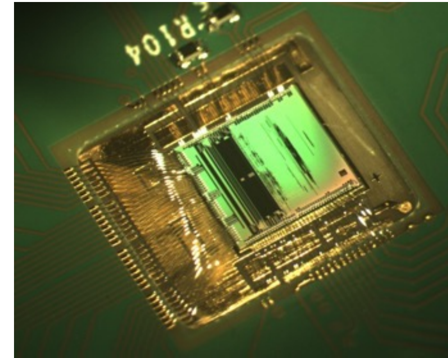
<u>Full detector phase I</u>

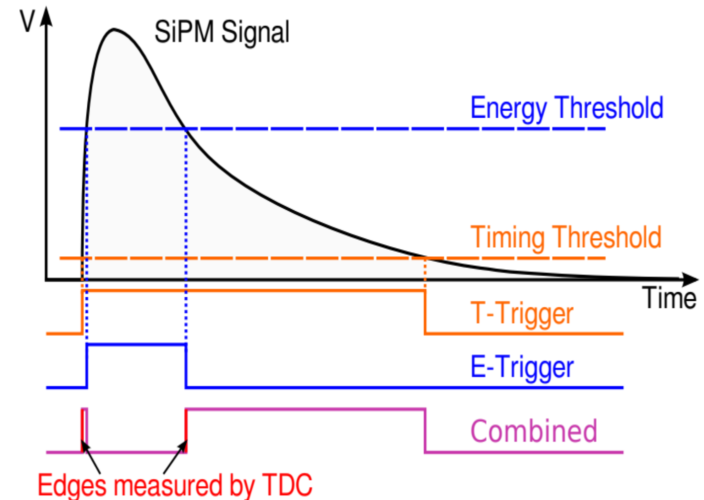
- 2 recurl station – total of 6272 channels



MuTrig ASIC status

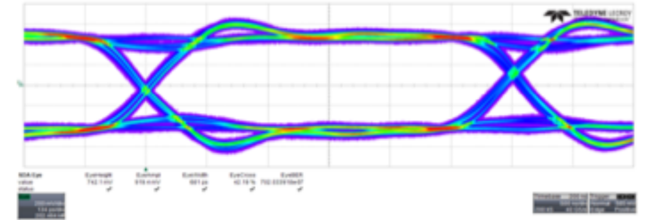
- 32 channels successor of STiCv3 – same front-end
- Preserve the timing performance of STiC 3.1
- Increase the event rate capability
  - Gigabit serial data link (1.25 Gbps)
  - Switchable event length
- Add more digital functionalities (with compare to STiC 3.1)



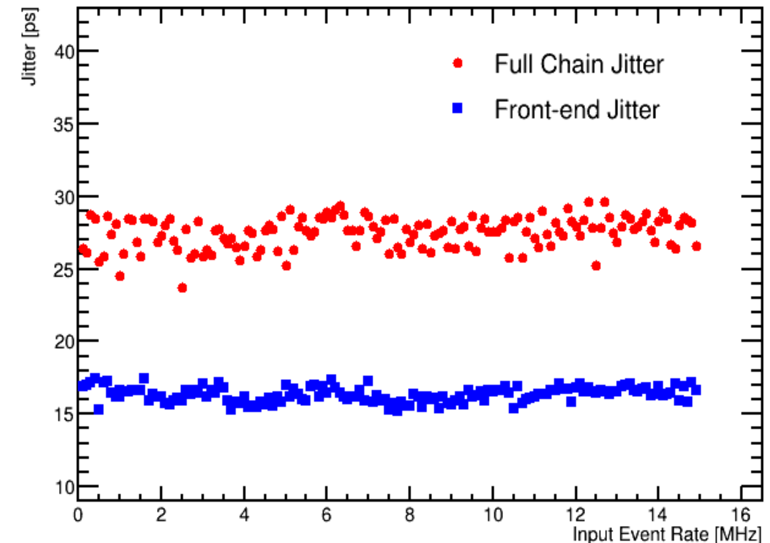


MuTrig characterization

- Customized LVDS TX: Opened eye diagram with 8b/10b encoded RPBS data pattern @ 1.25 Gbps
- Bit Error Rate (BER) upper limit of O(10^{-15}) for bit rate up to 1.9 Gbps.



- 460 fC charge injection over 15pF, input signal frequency up to 15MHz
- Use on-chip TDC for time stamp digitization
- Analog Fornt-End jitter < 18 ps
- Full Chain jitter < 31 ps



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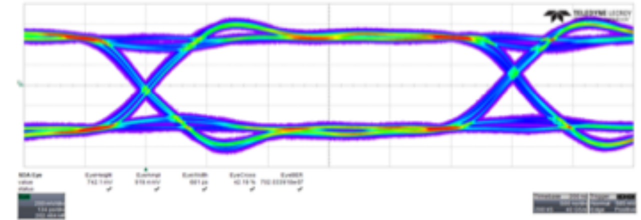

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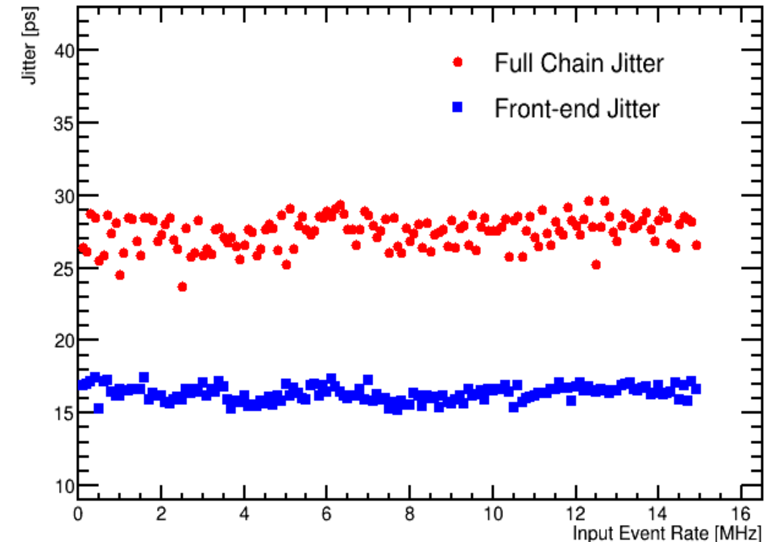
Will be tested in Desy Testbeam

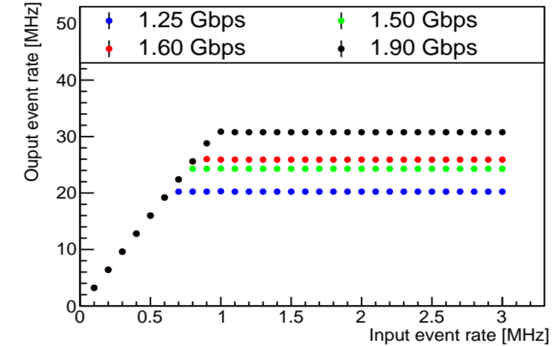


Digital Functionality Verification Results

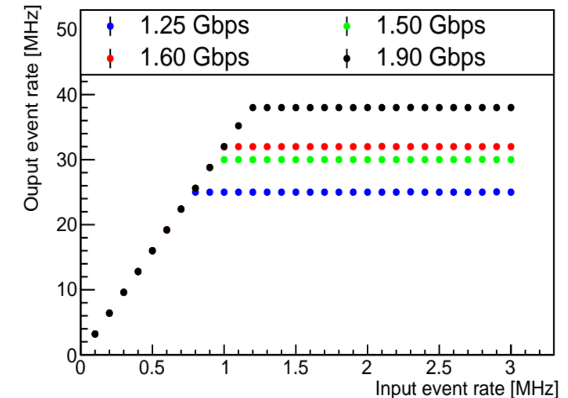
Two readout option:

- 48 bit/event:
  - both time and energy info
  - Event Rate limit: 20.24 MHz (632 kHz/ch)
  - Limited by the serial data link rate
- 27 bit/event:
  - time info. + 1 bit energy info.
  - Event rate limit: 25 MHz (781 kHz/ch) @ 1.25 Gbps
  - Limited by the on-chip digital circuit (will be fixed in the next tape-out)
  - Expected event rate limit: 35MHz (1.1MHz/channel)

Standard



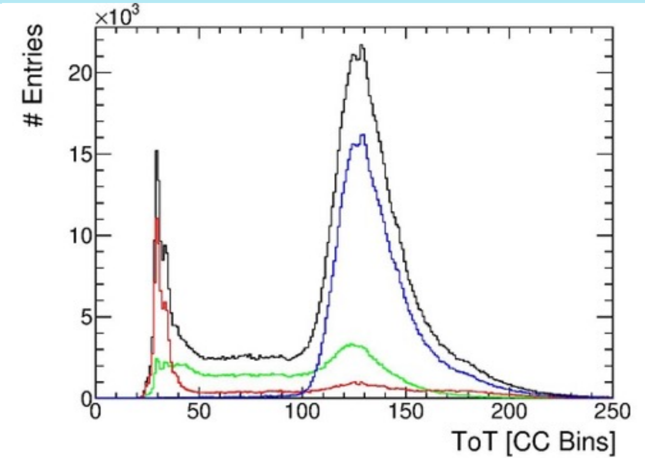
Short



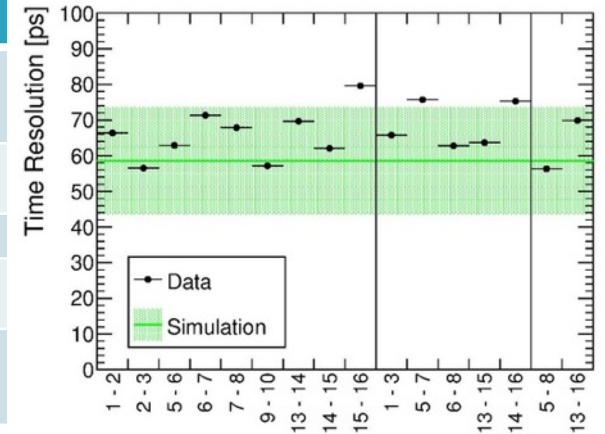
Bit rate	SER_CLK freq.	Max. Event Rate (std event)	Max. Event Rate (short event)
1.25 Gbps	625 MHz	20.24 MHz (632 kHz/ch)	25 MHz (781 kHz/ch)
1.50 Gbps	750 MHz	24.29 MHz (759 kHz/ch)	30 MHz (938 kHz/ch)
1.60 Gbps	800 MHz	25.91 MHz (810 kHz/ch)	32 MHz (1 MHz/ch)
1.90 Gbps	950 MHz	30.77 MHz (962 kHz/ch)	38 MHz (1.188 MHz/ch)

Old Prototype – Reminder

- From ToT "energy" spectrum ->time walk correction
- Showed excellent time resolution σ=70 ps
- STiC2 "feature" caused lower efficiency



	Old Prototype	Current Prototype	Reason	Expected Impact
ASIC	STiC V2	STiC V3.1	Bug fix,	DNL correction possible (can shift Higher Efficiency
Tile Size	8.5x7.5x5.0 mm^3	6.5x6.5x5.0 mm^3	Shorter Module	Smaller light yield – worse time resolution
Scintillator	BC408	BC418/Ej-228	Faster rise time	Better time resolution
Scintillator coating	TiO_2 paint (5 sides)	ESR foil	Higher light yield/less CT	Better time resolution
SiPM/ Scintillator coupling	Optical grease	Optical clear adhesive	must	Better light yield



The technical prototype: Overview

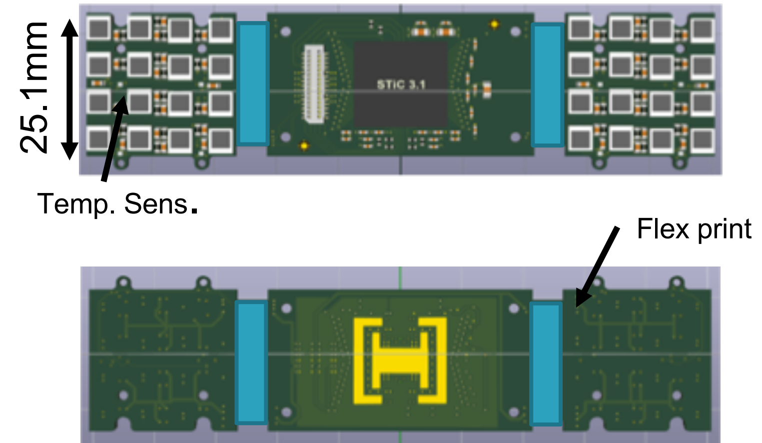
<u>Goals</u>

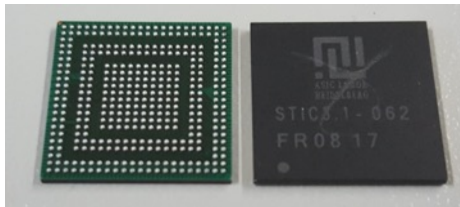
- Produce a module as close to design as possible
- Test mechanical support
- ASiC integration
- Cooling tests
- Learn and develop tools for assembly
- Develop test benches for detector characterization and quality control
- Measure detector performance
- Finalize detector design

The technical prototype: Front-end board

- Develop and produce the front-end board in the summer 2017
- Using the STiC 3.1 packaged ASIC (not MuTrig)
- Hamamatsu SiPMs S13360-3050PE

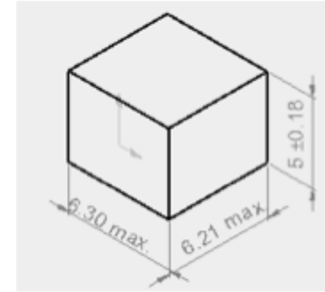
- New test board to test the packaged chips before assembly
  - Charge injection test: functionality and noise performance

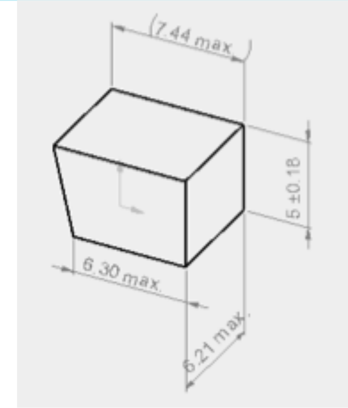


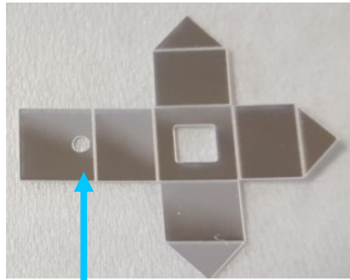


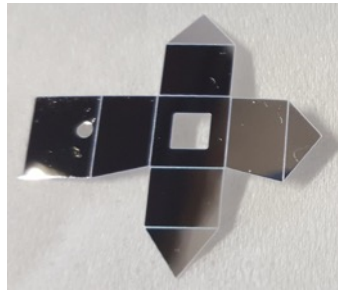
Tile production and wrapping

- Scintillator material Ej-228 (equivalent to BC-418)
- KIP workshop produced 180 tiles
- Foil design to maximize reflection (ESR 3M foil)







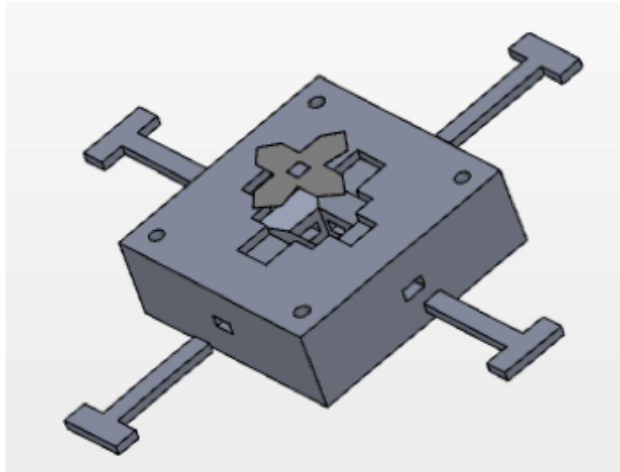


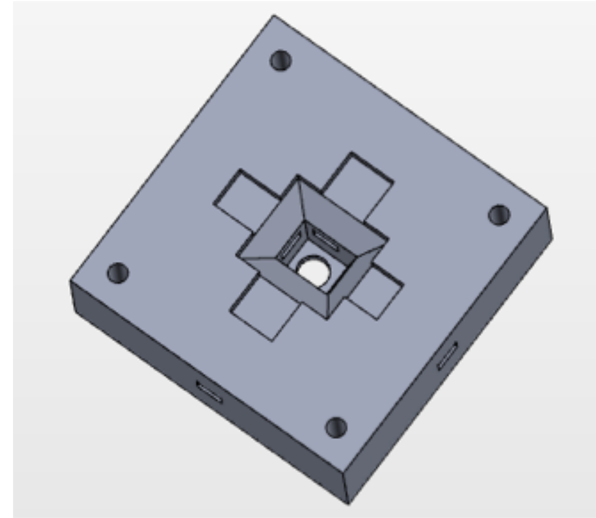
Hole for monitoring the glue quality

The technical prototype: Tile Wrapping

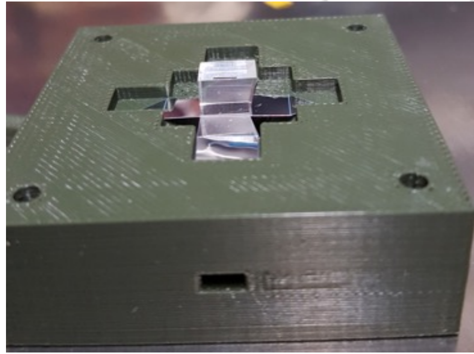
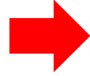
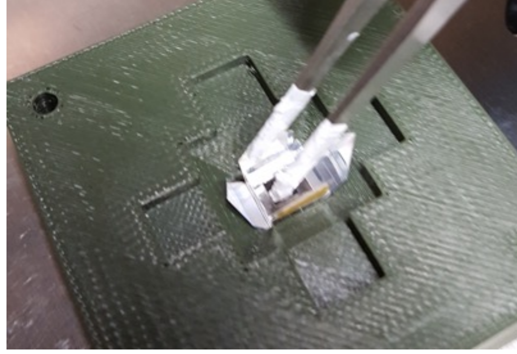
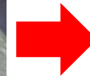
Wrapping tools:

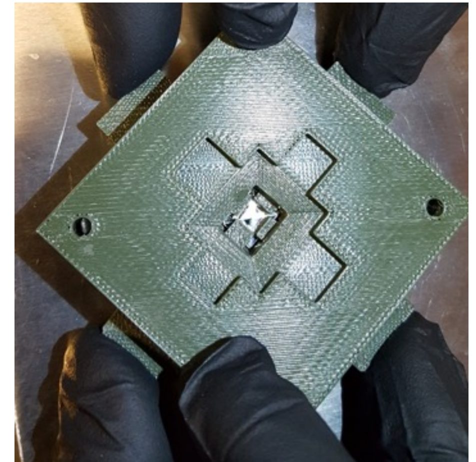
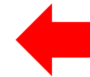
- Produce two for different type of tile
- Assembly of half module (16 channels) ~30min

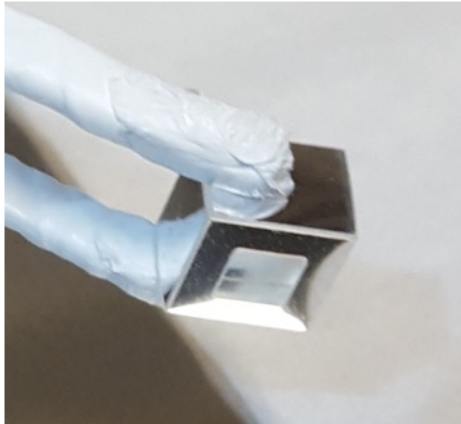




The technical prototype: Tile Wrapping work flow

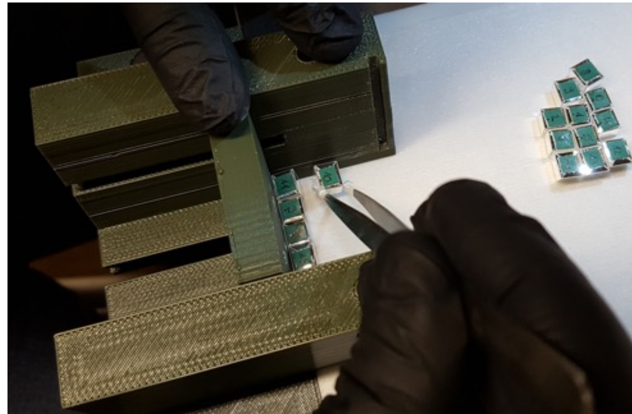







Submodule assembly

- Testing the ASIC and fully equipped the PCB (electronic lab)
- First measurement (DCR, Laser)
- Using micrometer for tolerance check of the tile size before wrapping
- Tile wrapping
- Glue 16 channel together, to avoid tolerance issues
- Dispense glue
- Monitor for bubbles after 24h of curing



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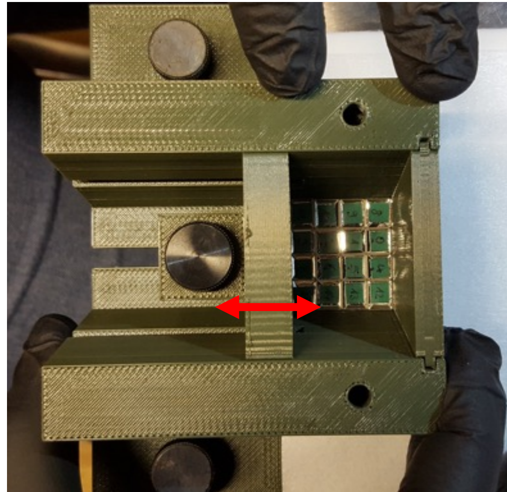

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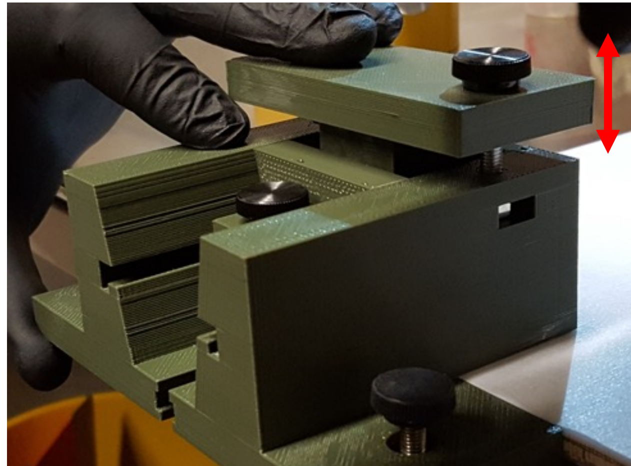

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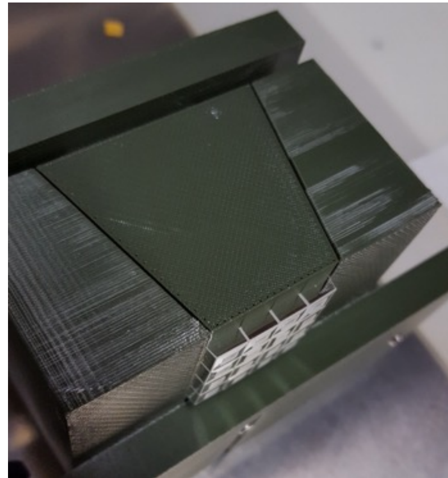

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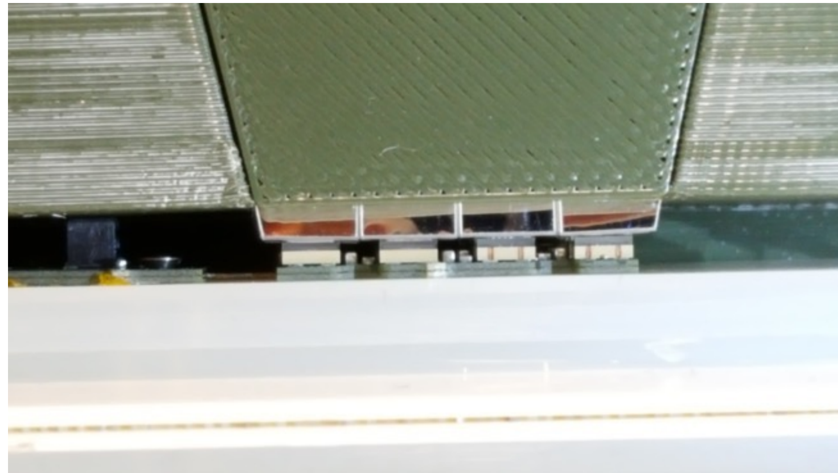

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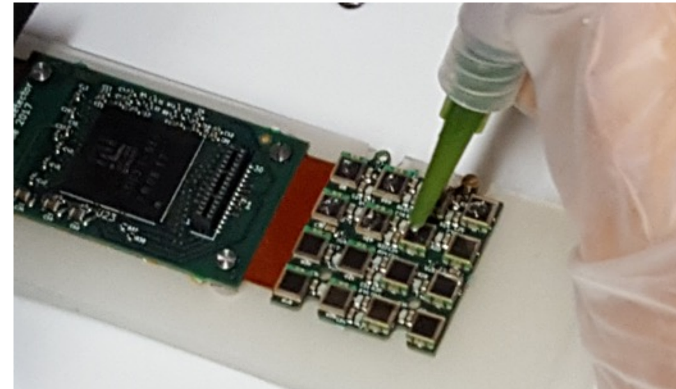

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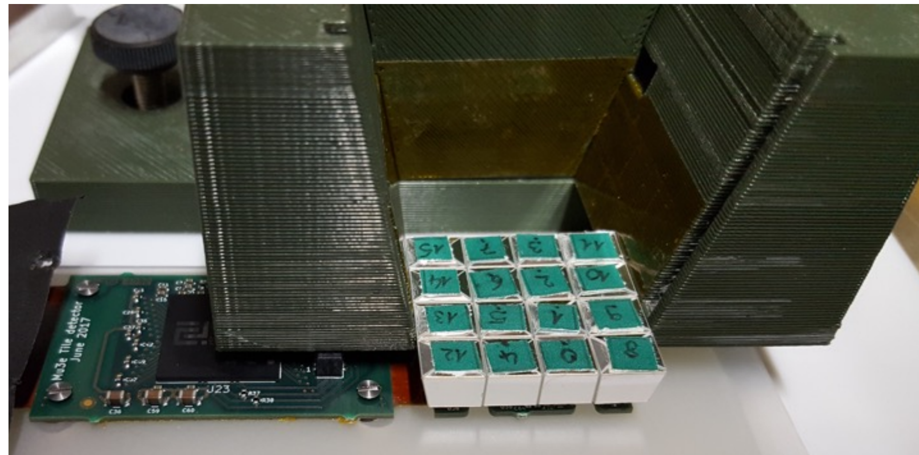
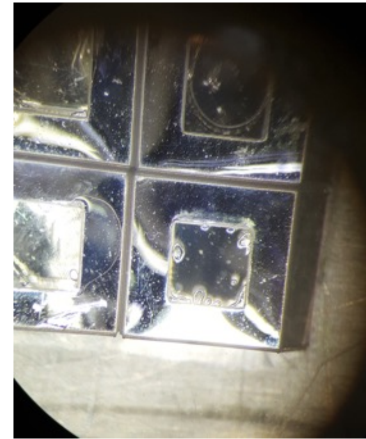
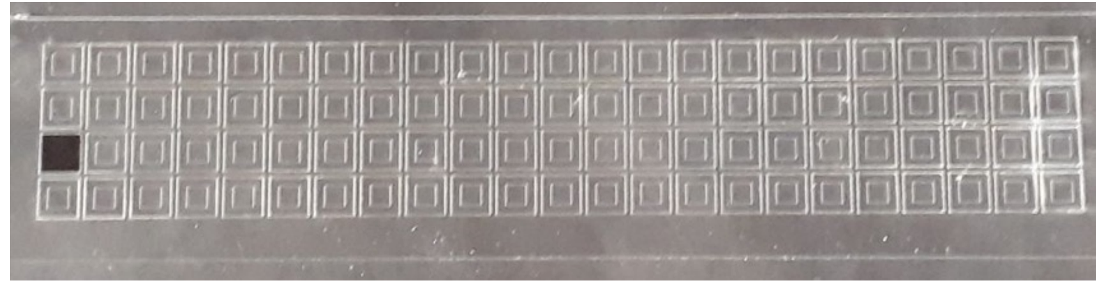


Submodule assembly – Glue issues

- Very important to monitor for bubbles – can reduce light yield by 50%
- After several trial, updates assembly tools and find the correct amount of glue, we managed to have a full matrix without bubbles
- New solution under test:
  - 3M OCA- layer of adhesive 125um protective film from both sides (125um)
  - Cut desired shape using the laser cutter
  - Only press, no bubbles!



Submodule assembly – new glue solution



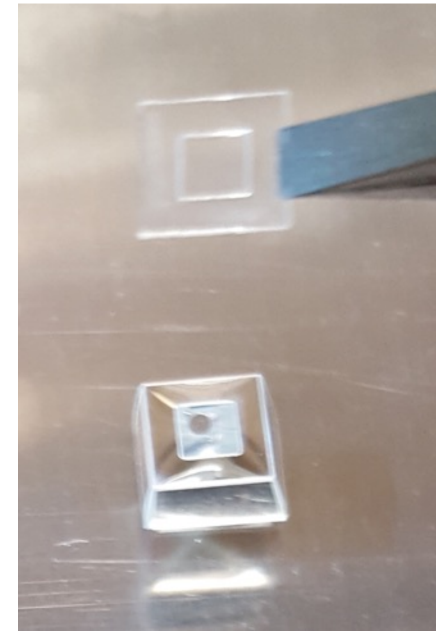
<u>Pros</u>

- Save most of the cure time
- The process is more uniform
- Match one-to-one to tile
- No bubbles!

<u>Cons</u>

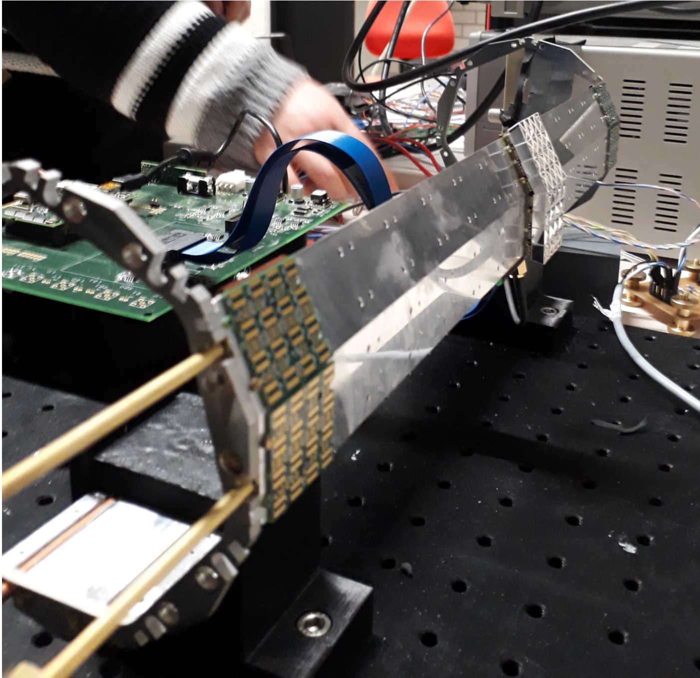
- Assemble under microscope (can be improve)
- Currently Slower process
- Min purchase 60cmx180m

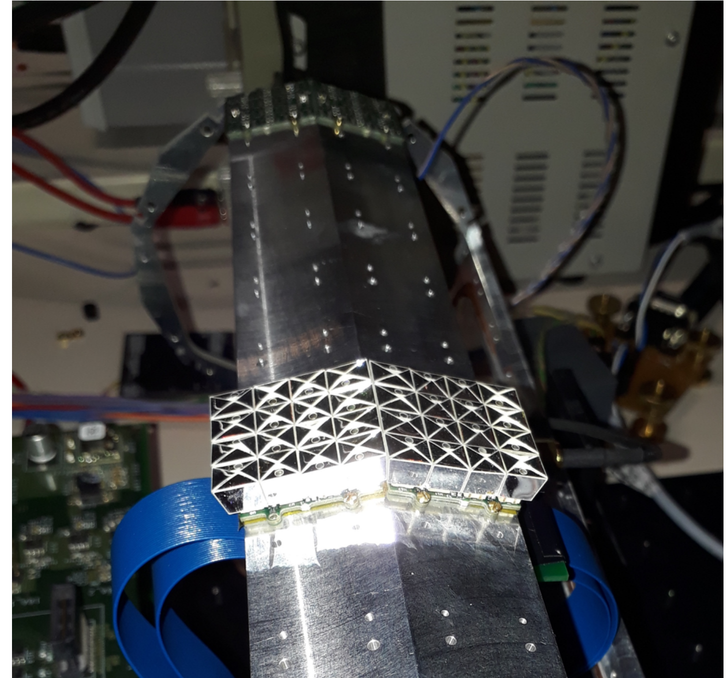
- Testing light yield for both glues (ongoing)



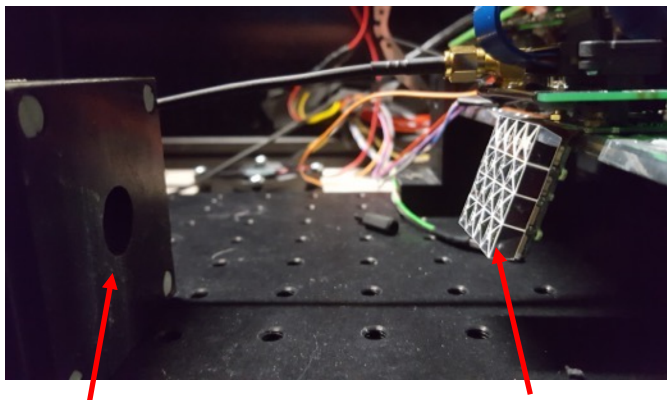
The technical prototype: Production status

- Mechanics – endrings+ 3 cooling support structure
- In Total we fully assembled 3 submodules (96 channels)
- Stand alone module – 16 channel, readout MuTrig/Scope (see following slides)



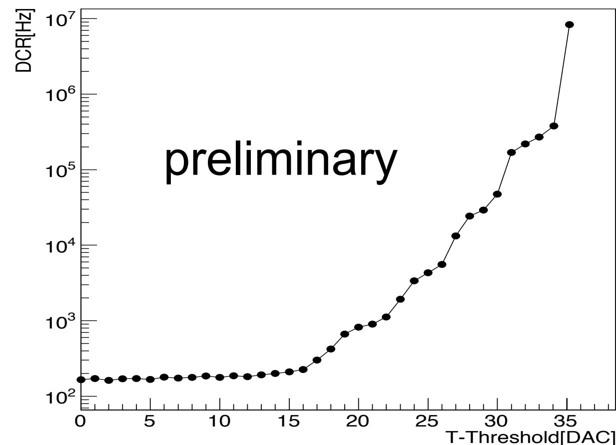


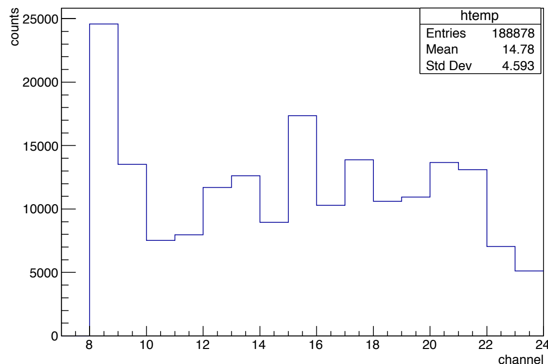
The technical prototype: Lab measurements ongoing

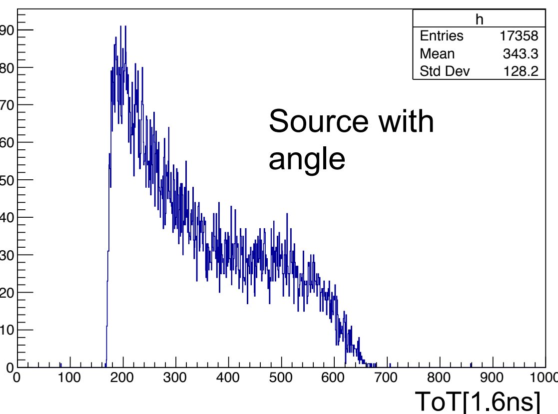


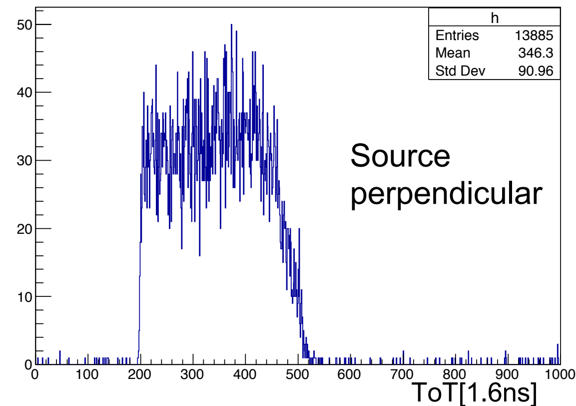
Source Sr90

submodule





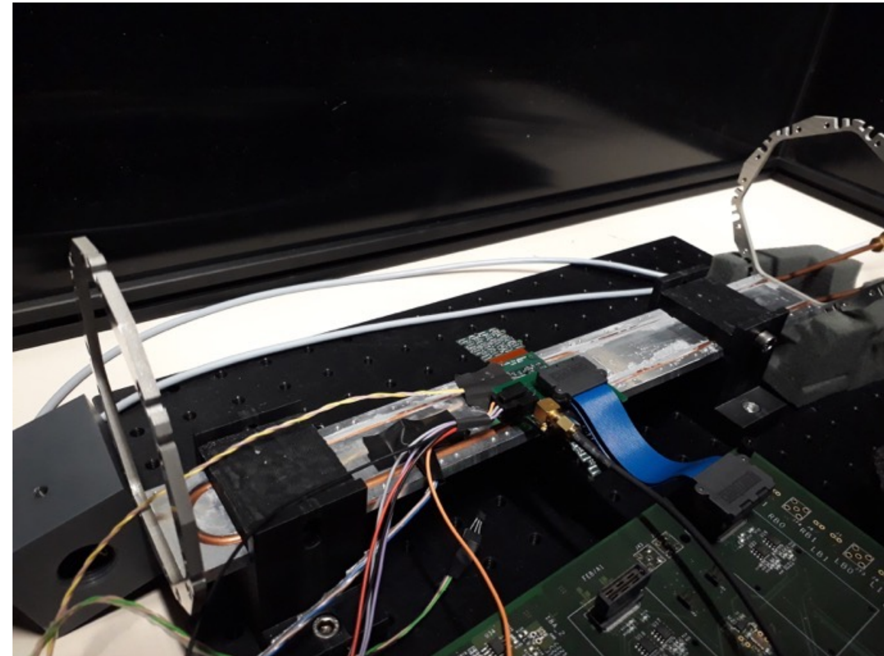




The technical prototype: Cooling studies

Aim

- Test the current mechanical design under lab condition
- Thermal simulation of full device under lab condition
- Extrapolate to experiment condition
- Once the simulation is reliable, test feasibility for different design modification needed (see integration talk)

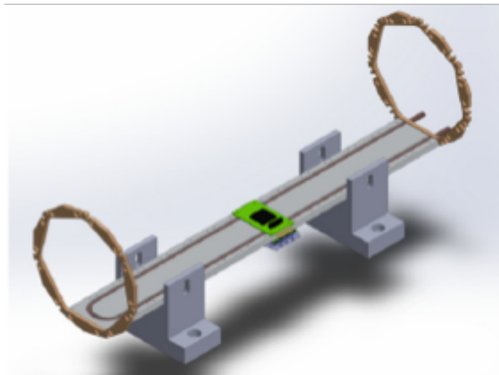


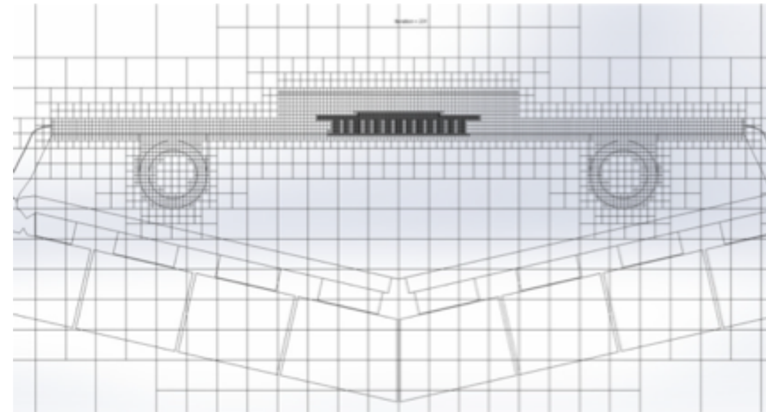
Lab setup

- Single submodule + mechanical structure
- Temperature sensors- on ASIC, lab, water in/out, cooling plate
- Measure water flow speed
- Tested at different ASIC conditions (different power consumption)

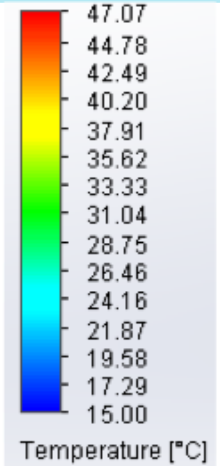
The technical prototype: Cooling studies

- Flow simulation in SolidWorks
- Construct the same setup as the lab setup
- Build a realistic model of the package ASIC and the PCB (include the thermal vias)
- Input (from lab measurements):
  - water temperature in 15°C
  - lab temp 21°C
  - Water flow peak 1m/s (0.63m/s on average)
  - ASIC power consumption (same as table)
- Measure the temperature of the top of the package

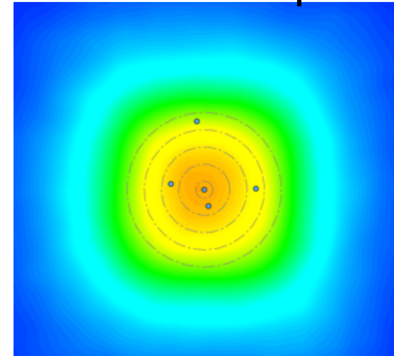




Example results for highest power consumption:

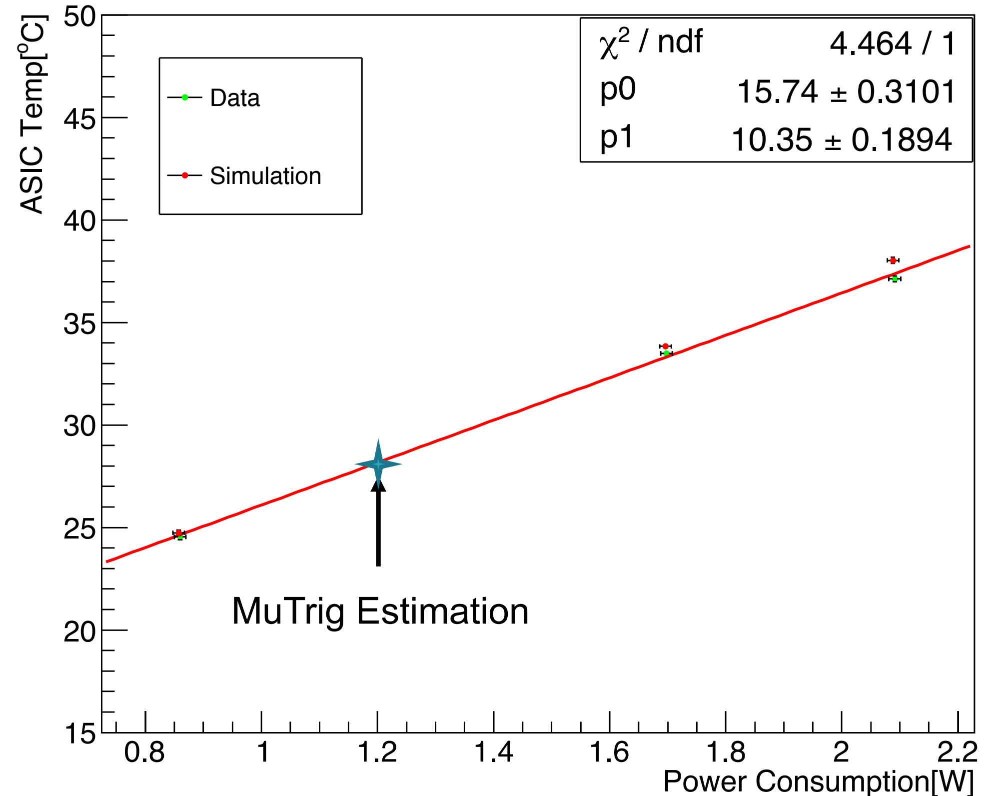


ASIC top



The technical prototype: Cooling studies

- Repeat at different power consumption of the ASIC
- Very good agreement to data (<1°C
- Small systematic error (Integration area of the temp. sensor is too small)
- Next step full module (ongoing)



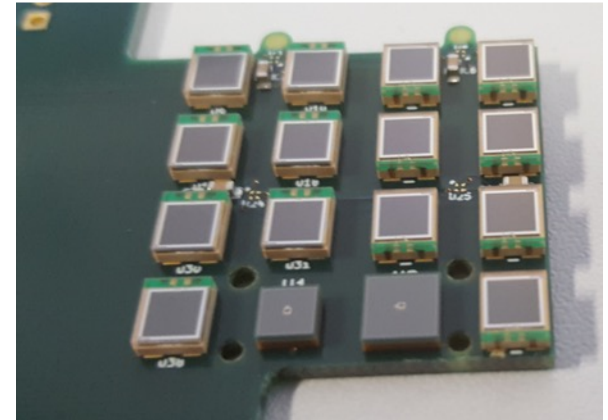
The technical prototype: test beam plans

Goals Submodule

- Module calibration
- Time resolution with respect to incident angle
- Measure the detection efficiency and crosstalk

Stand alone setup

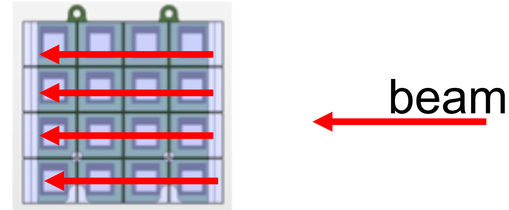
- Evaluate the performance of 2 new SiPMs: (hole wire bonding) 3x3 mm^2, 4x4 mm^2
- Readout option:
  - MuTrig evaluation board
  - Scope

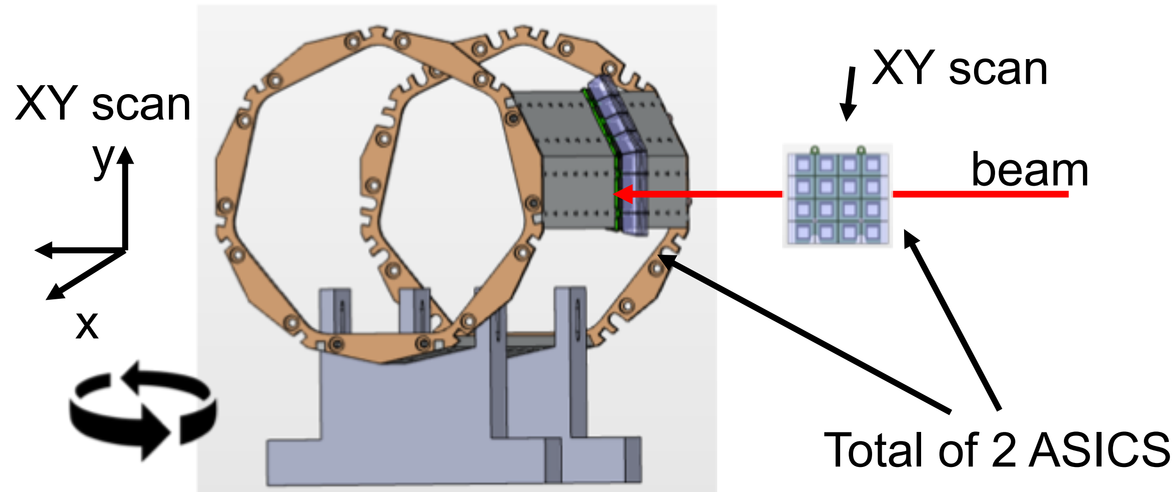


The technical prototype: test beam Setup

Trigger

- ~6.5x5.0mm^2 x4
- $T=\Sigma t_i/4$, $\sigma= \sigma_i/2$
- Larger energy deposition





Outlook 2018

Milestone	BVR 48	BVR 49
Prototype of support structure & cooling	Q2/17	✓
prototype of TileFEB (with STiC3.1)	Q3/17	✓
32 channel technical prototype (support, cooling, FEB, STiC3.1)	Q4/17	✓ (96 ch)
MuTRiG test	Q4/17	✓
MuTrig Integration	Q4/17	Q3/18
Develop QA scheme	Q1/18	Q2/18
Mass production strategy	Q1/18	Q2/18
Readout integration into DAQ and slow control	Q2/18	Q3/18
Cooling simulation for full detector		Q1/18
Full prototype –modified mechanics, MuTrig	Q4/18	Q4/18*

*based on funds

Production Schedule

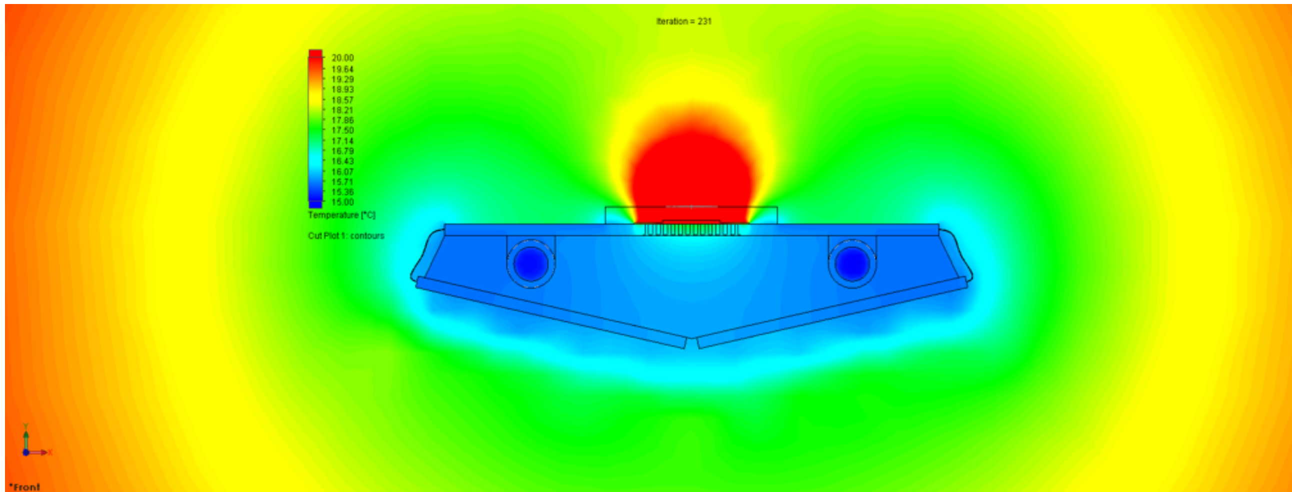
Expected starting at March 2019

Production step	Schedule	comments
Tile production	Q2 2019	3 month
Mechanical production	Q2 2019	3 month
PCB assembly+ASIC testing	Q2 2019	196 boards
Submodule assembly	Q3 2019	4 a day total of 10 weeks
commissioning	Q4 2019	4 month

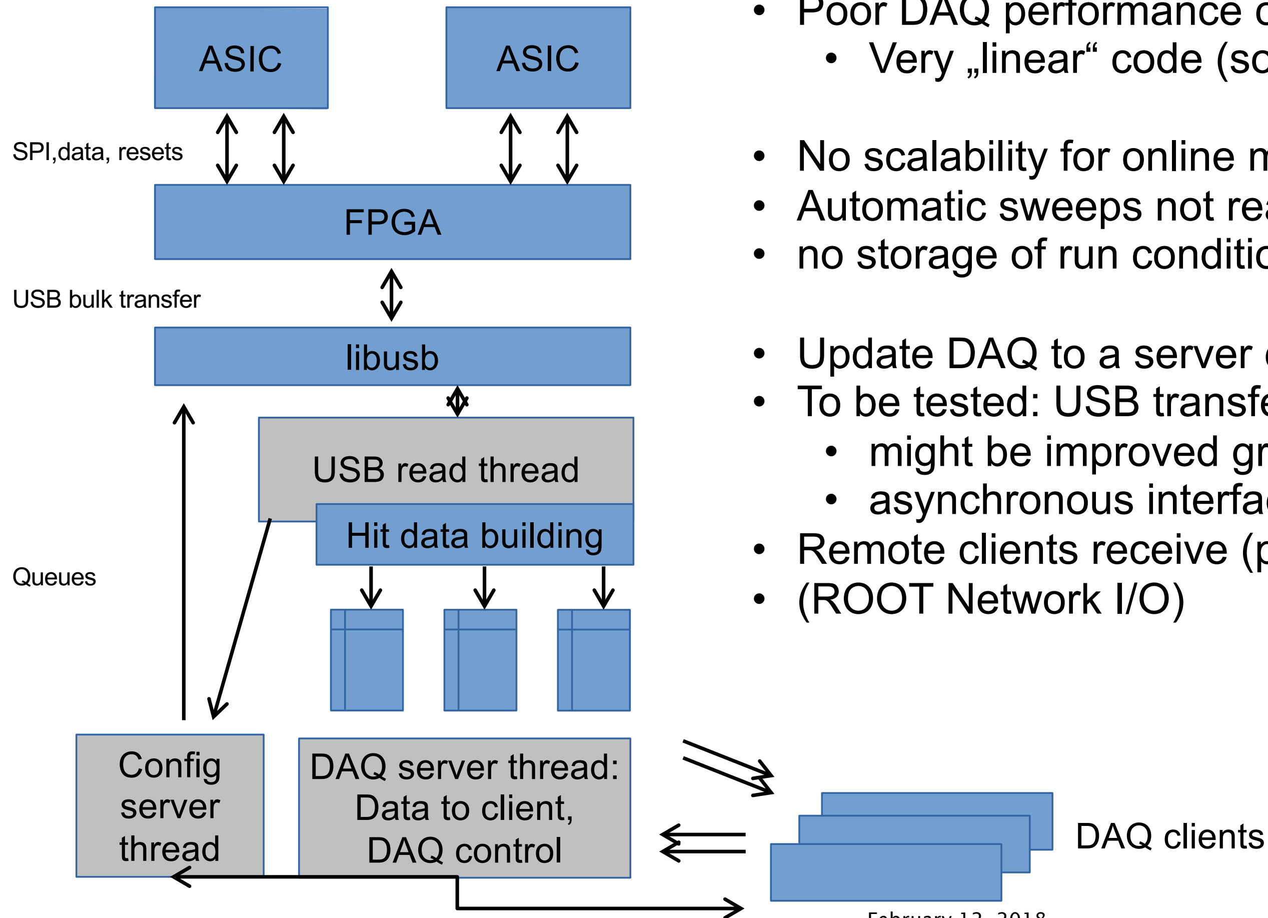
Summary

- MuTrig ASIC is working!
- Technical prototype produced with 96 working channels!
- Assembly tools were design and tested, will be finalize for mass production soon
- Detector performance will be tested next week (DESY)
- Full prototype including MuTrig and DAQ integration is expected this year!
- Will be ready for the vertical slice demonstrator by the end of the year!

BK slides


Iteration = 231
20.00
19.64
19.29
18.93
18.57
18.21
17.86
17.50
17.14
16.79
16.43
16.07
15.71
15.36
15.00
Temperature [°C]
Cut Plot 1: contours
*Front

The technical prototype: test beam DAQ scheme



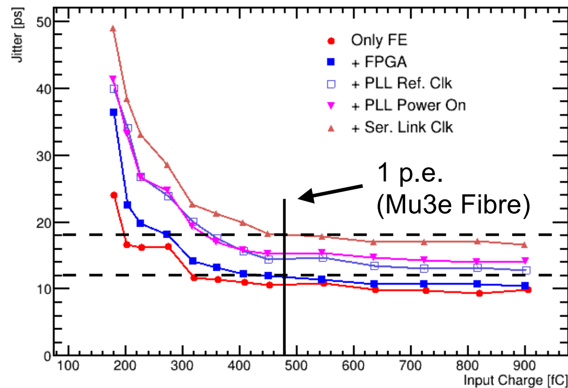
- Poor DAQ performance compared to USB limit
  - Very „linear“ code (some sleep statements)

- No scalability for online monitoring
- Automatic sweeps not really possible,
- no storage of run conditions

- Update DAQ to a server client, parallelized system
- To be tested: USB transfer rate
  - might be improved greatly using libusb's
  - asynchronous interface
- Remote clients receive (prescaled) data over TCP
- (ROOT Network I/O)

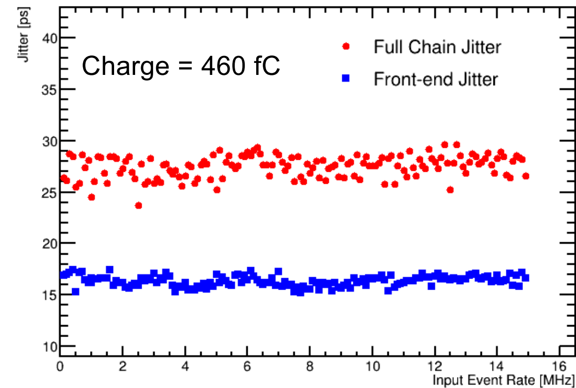
Timing Performance Characterization Results

Analog Front-End Jitter Performance



- Charge injection over 15pF Capacitance
- Only analog FE: FE Jitter < 11 ps for charges > 500 fC
- Full operation: FE Jitter < 18 ps for charges > 500 fC
- Degradation due to digital activity (pollution over PCB)

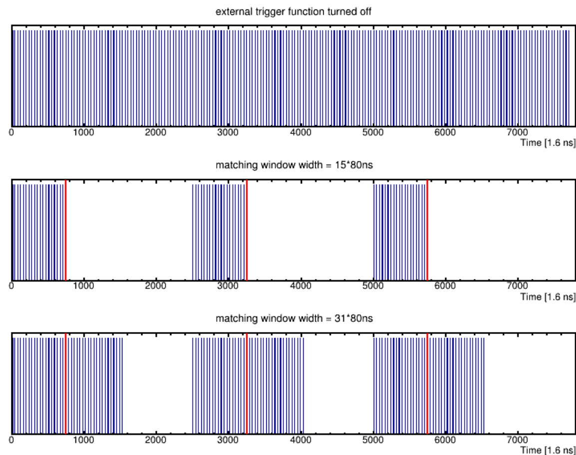
Full-Chain Jitter Performance



- 460fC charge injection over 15pF, input signal frequency up to 15MHz
- Use on-chip TDC for time stamp digitization
- FE jitter < 18 ps
- FC jitter < 31 ps

Digital Functionality Verification Results

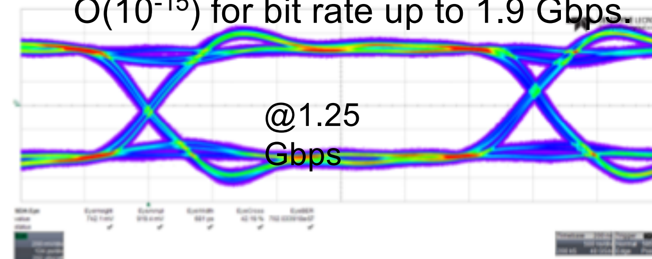
Validation of the External Trigger Functionality



Event distribution in one data frame for different external trigger configurations

Serial data link quality characterization

- Customized LVDS TX: Opened eye diagram with 8b/10b encoded RPBS data pattern @ 1.25 Gbps
- Bit Error Rate (BER) upper limit of O(10^{-15}) for bit rate up to 1.9 Gbps.

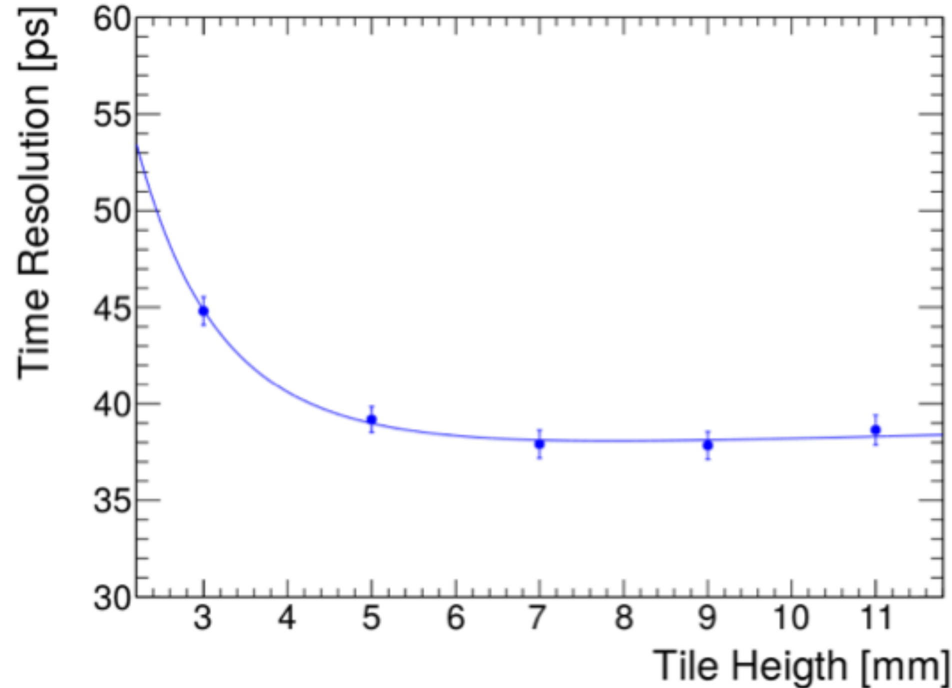


Bit rate	BER
1.25 Gbps	< 5.90E-15
1.50 Gbps	< 4.34E-15
1.60 Gbps	< 4.63E-15
1.90 Gbps	< 3.65E-15

Lines from one recurl station

- 5 power lines
- 14x(2x spi, 2x reset, 2xcec * ,4xclock_diff ,2xdata ,2xpll_test_diff, external trigger *,2xI2C,2xHV)
- Shared (2x SPI) x7
- Total of 1911 per recurl station (294 are optional)

Time resolution for different tile height



- the time resolution is not dominated by photon statistics (for which black might maybe be better) but by noise - so we want as much signal as possible.
- reflected photons arrive only a couple of 10 picoseconds later because the tile is so small