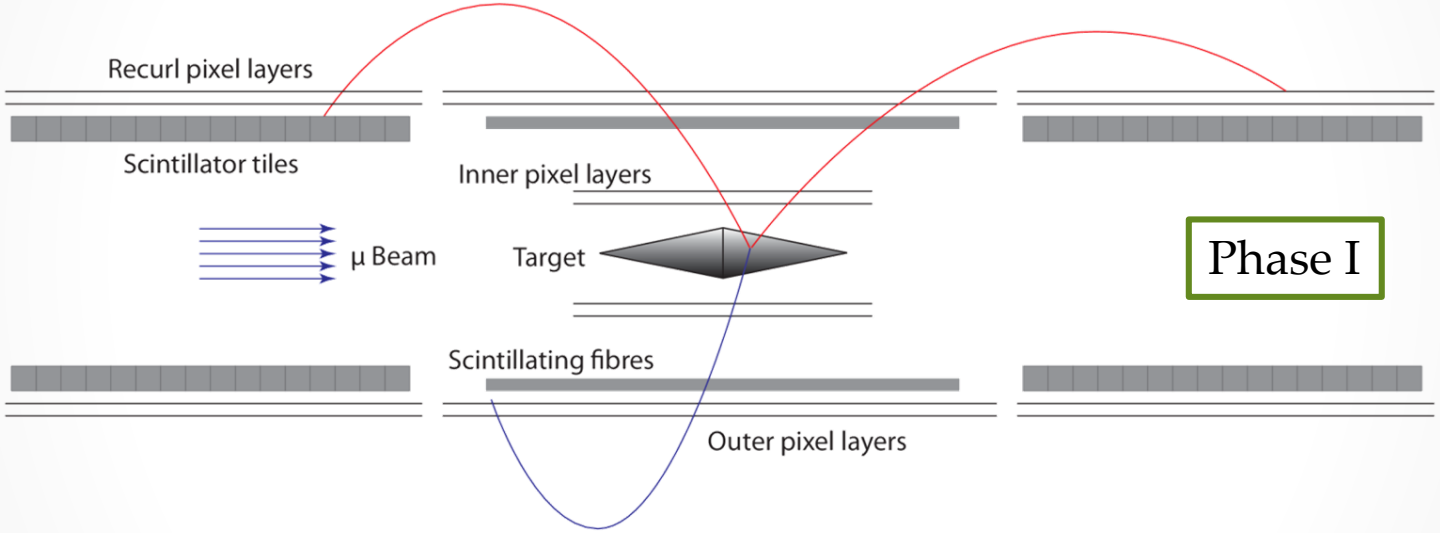
Detector R&D for Mu3e

Dirk Wiedner on behalf of Mu3e

February 2018

Phase I Experiment

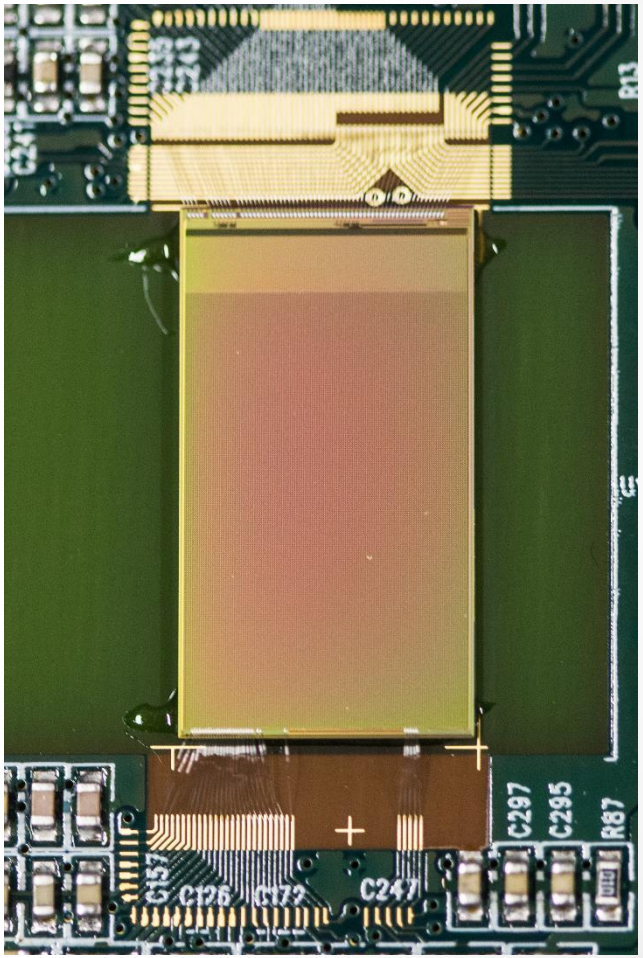


- Muon beam O(10^8/s)
- Helium atmosphere
- 1 T B-field

- Target double hollow cone
- Silicon pixel tracker
- Scintillating Fiber detector
- Tile detector

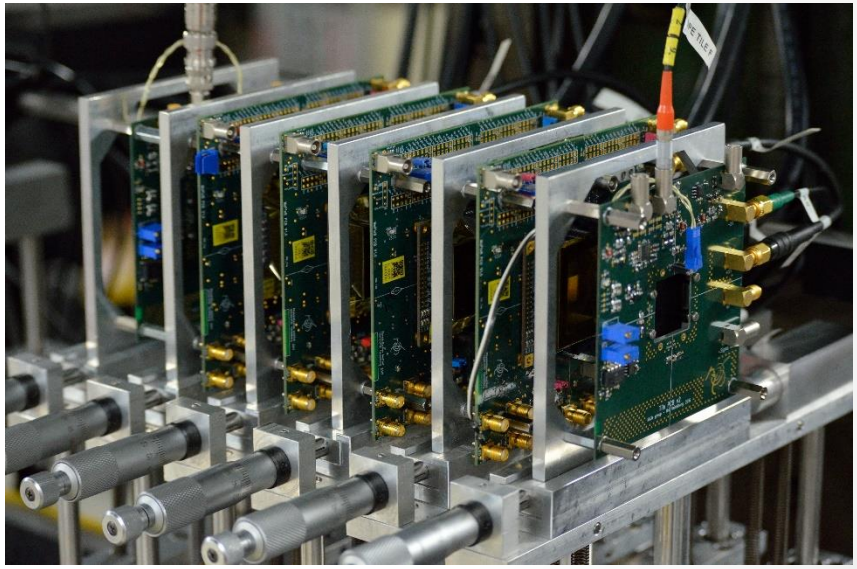
Pixel detector R&D

- Pixel sensor
  - Crutial for ultra thin Mu3e tracker design
  - MuPix8 first large prototype
  - Full characterization
  - So far very promising results
    - >99.5% efficiency
    - <1Hz per pixel noise
    - <10ns time resolution
    - <250mW/cm^2 power



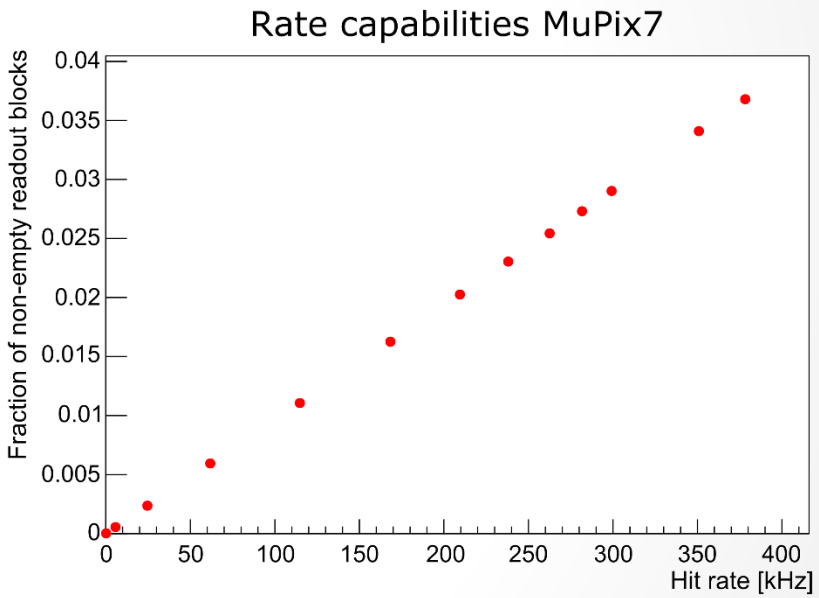
Test beam setup

- MuPix8 telescope
  - Beam telescope
  - 4 layers of MuPix8 pixel sensors
  - Includes DUT
  - Scitillators as time reference



Test beam requirements

- High rate stability test
  - Requires beam with 20kHz to >1 MHz particle rate
  - MuPix8 test
  - Readout system test
- Scans of operational parameters
  - HV-scan
  - Bias current scans
  - ➢ Many events required
  - ➢ High beam rate required



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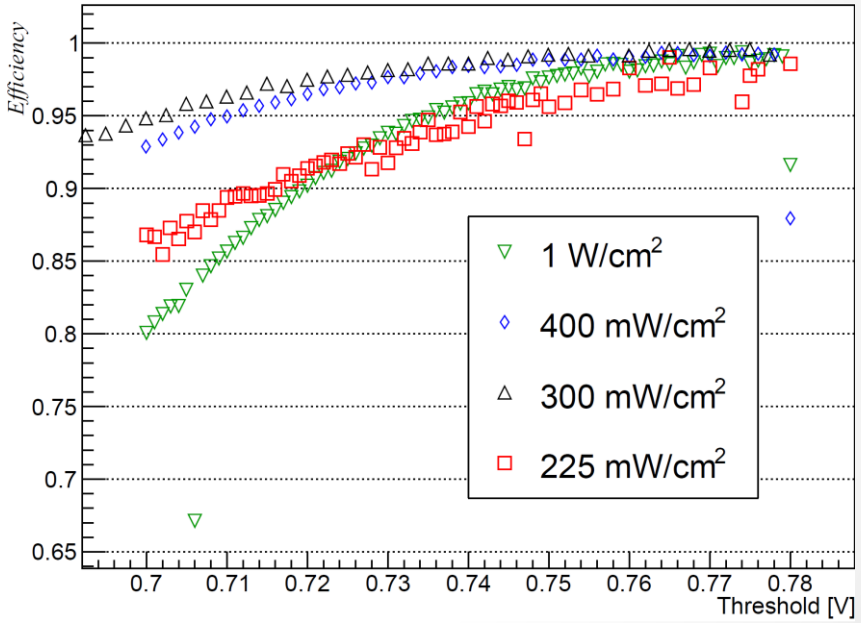
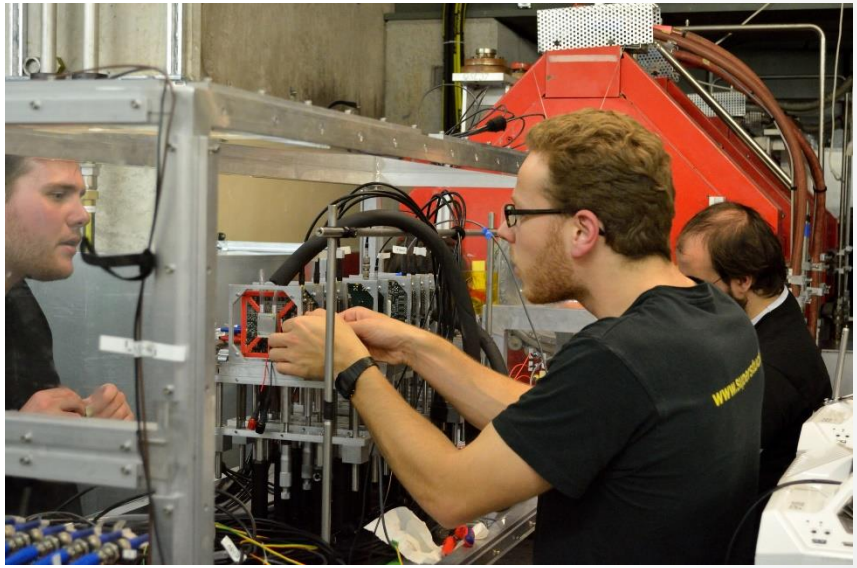


Scan of MuPix7 bias settings taken at piM1

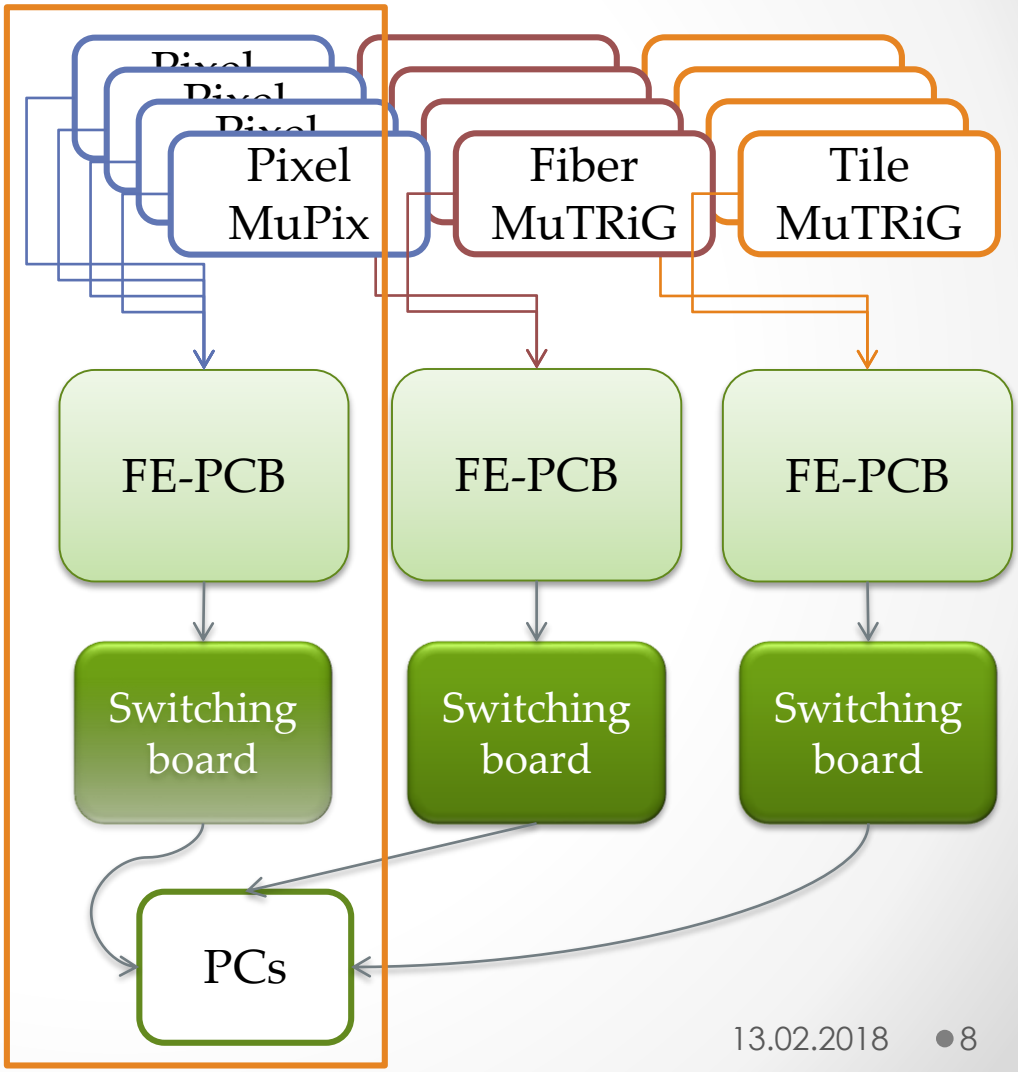
Integration Challenges

- System tests
  - Pixel chips
  - Data acquisition system
  - Monitoring and Data quality
  - Control system
  - Services
    - Low voltage system
    - High voltage system
    - Cooling
- Vertical slice test



Readout Vertical Slice Test

- Pixel detector
  - HV-MAPS (MuPix8)
    - ✓Large prototype
- Front end board
- Switching board
  - PCIe40
  - Delivery 2018
- PC



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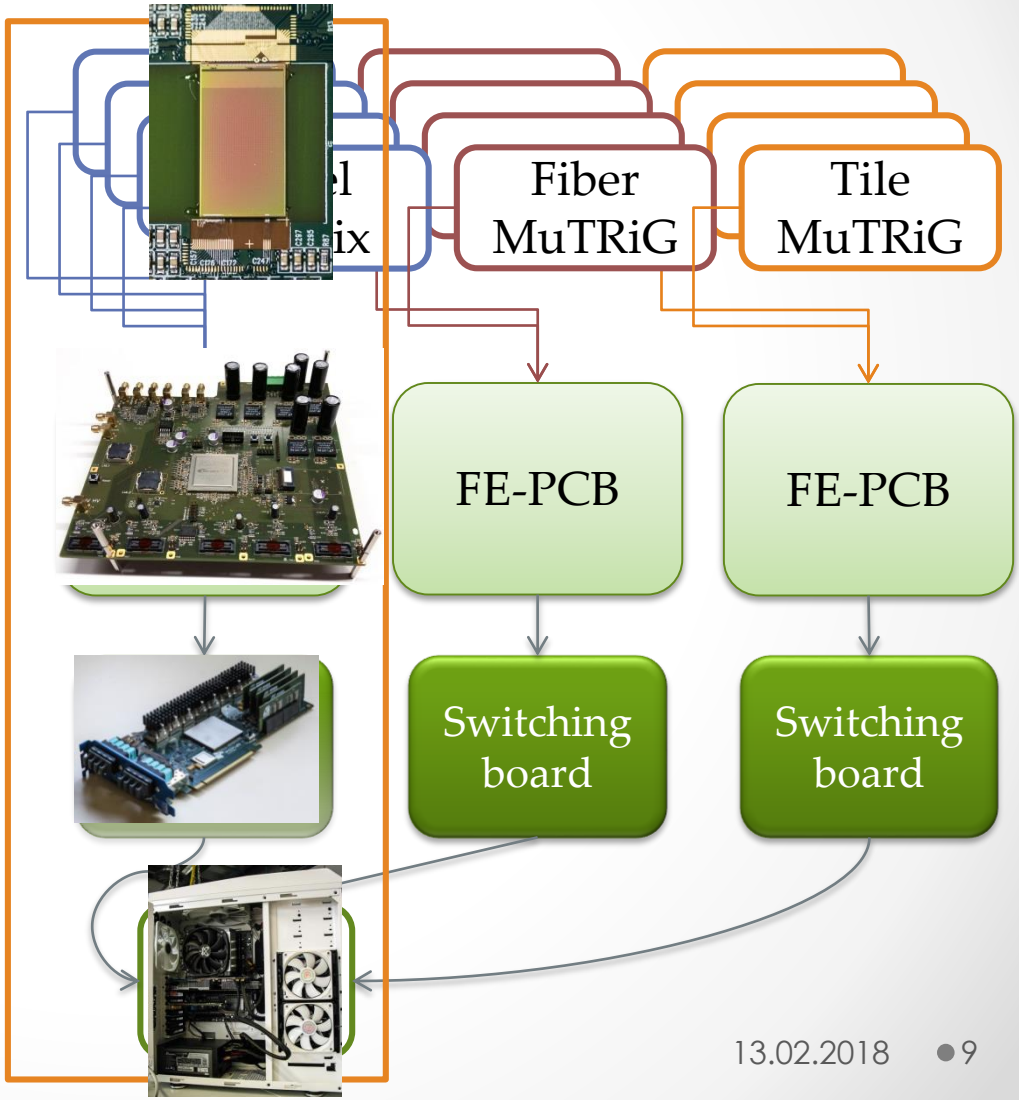
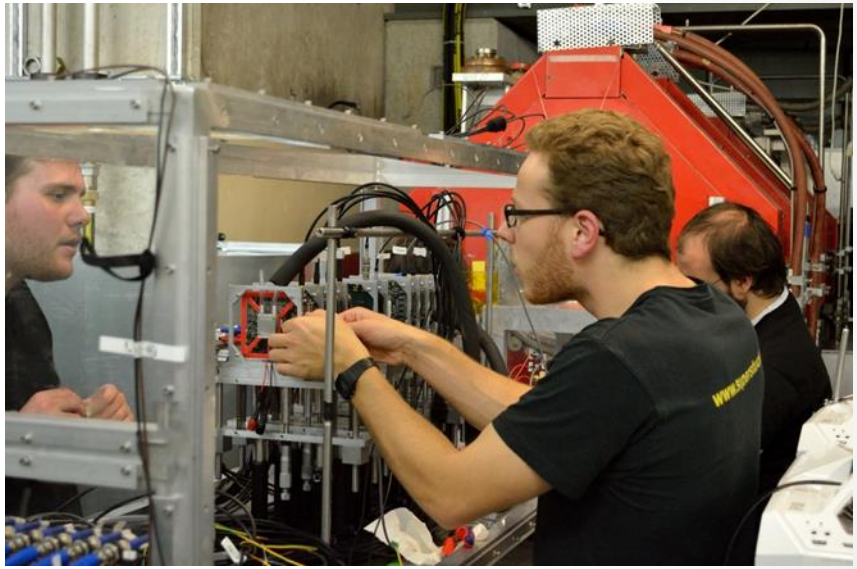
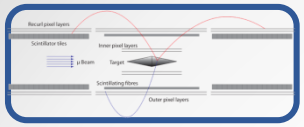


Summary

- Mu3e requests 1 week of test beam for pixel system
- Continue successful R&D monolithic pixel sensor MuPix
- 20kHz to >1MHz of rate
  - High rate test
  - Large parameter scans
- Vertical slice test for data acquisition system



Backup Slides

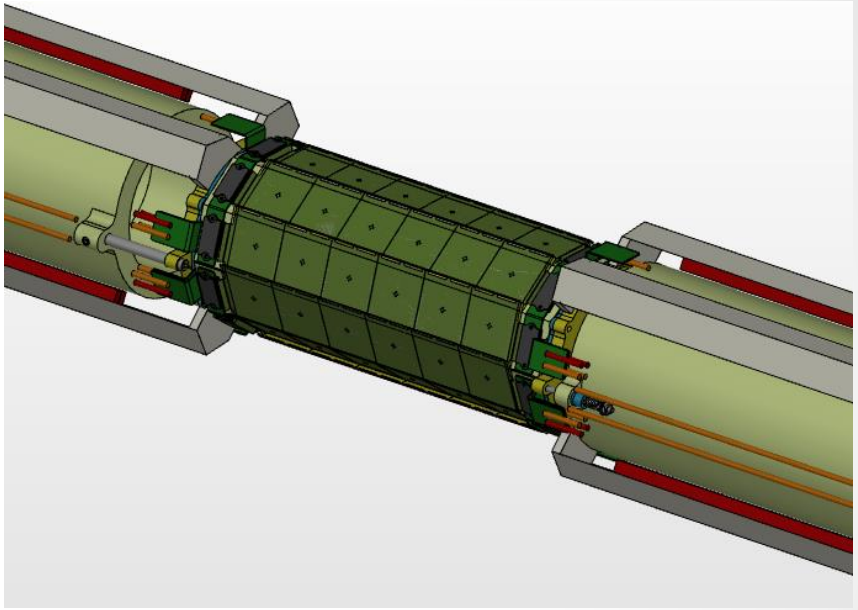


Pixel Tracker

- ✓ Successful **feasibility** studies for:
  - ✓ Module mechanics
  - ✓ He-cooling with low vibration
  - ✓ Ultrathin Flexible circuit boards
  - ✓ HV-CMOS large prototype
  - ✓ Readout board prototypes
- ✓ Ongoing re-design of pixel detector services
  - ✓ He distribution
  - ✓ Power and cabling
  - ➢ Effects all surrounding systems

To be done:

- **1st operational detector module**
- Qualification of optimized module design



Pixel Tracker
Rendering of CAD study
Re-optimized pixel tracker

See talk:
Pixel Detector
Frank Meier Aeschbacher

Fibre Detector

Accomplished:

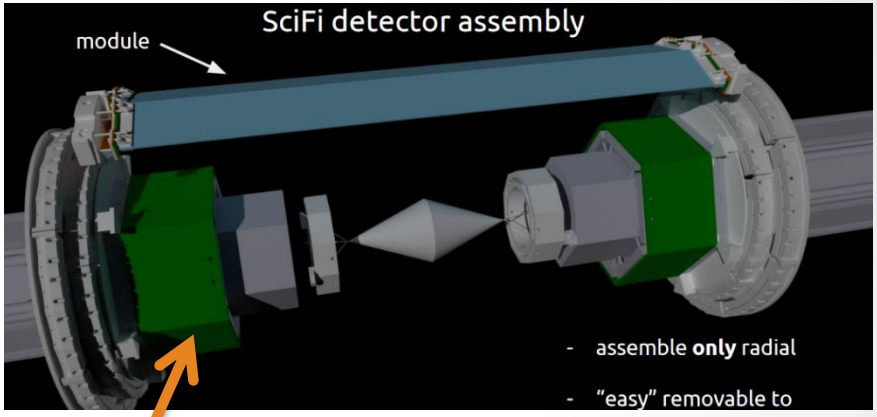
✓ Characterization of fibres

✓ **Proof of concept** including

- ✓ Simulation of fibre response
- ✓ Identification of working point

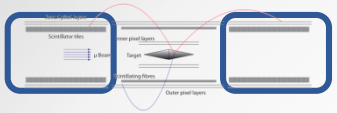
To be done:

- Choice of fibre type
- 1st operational detector module
- **Ultra compact front end electronics**
  - critical
    - **Integrate** new MuTRiG TDC chip

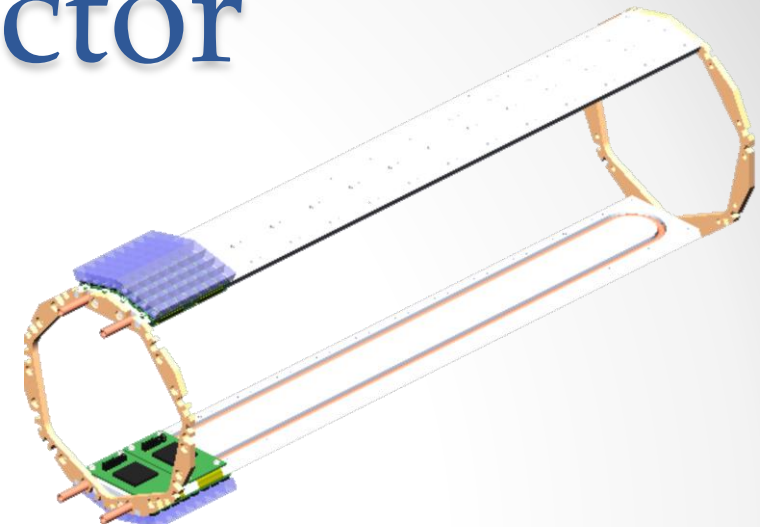


Fibre Detector
Rendering of CAD study

See talk:
SciFi
Antoaneta Damyanova



Tile Detector

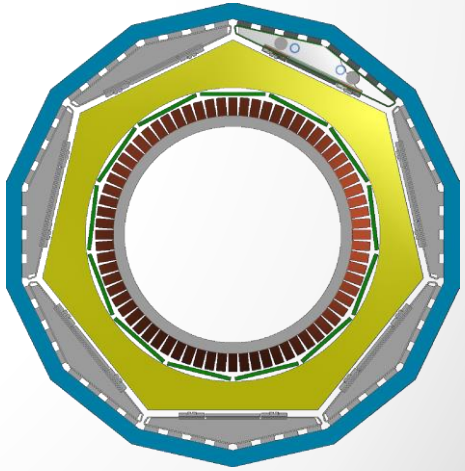


Accomplished:

- ✓ Characterization of submodule
- ✓ **Proof of concept** including
  - ✓ Production of similar system
- ✓ Development of TDC ASIC MuTRiG

To be done:

- 1st operational detector module
  - Prototypes in production
- Share space with He lines and cables

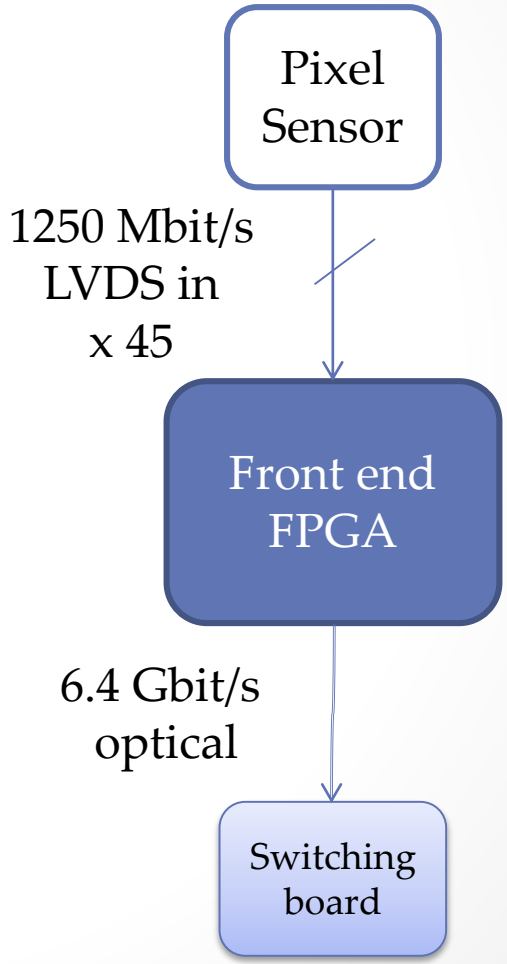


See talk:
Timing Detectors
Yonathan Munwes

DAQ Backup

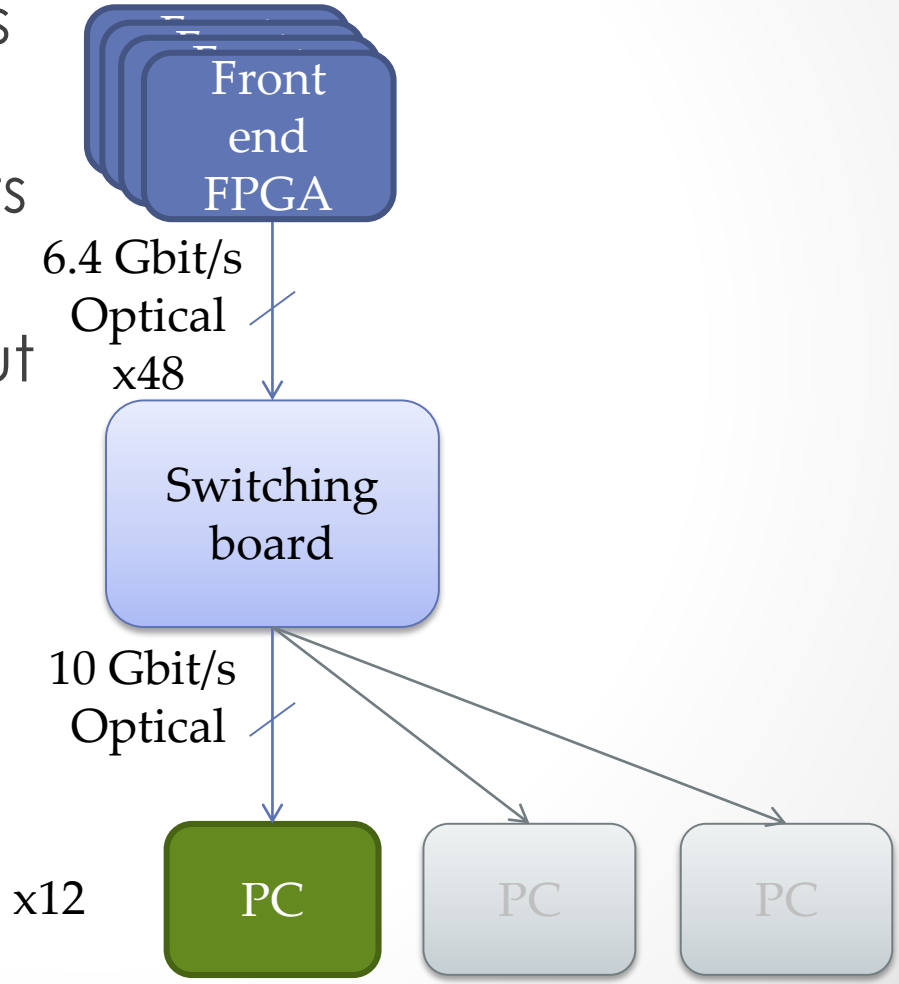
Front End FPGAs

- FPGAs in magnet volume
  - 112 pieces
- Receive sensor data
  - 36-45 LVDS inputs
- 6.4 Gbit/s outputs
  - 8 optical links
  - … to counting house



Switching Board

- FPGA switching boards
  - per sub-detector
- 6.4 Gbit/s optical inputs
  - 16-48 inputs
- 10 Gbit/s optical output
  - 12 outputs to PCs
- Switching network
  - One output per PC



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- FPGA switching boards
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- 6.4 Gbit/s optical inputs
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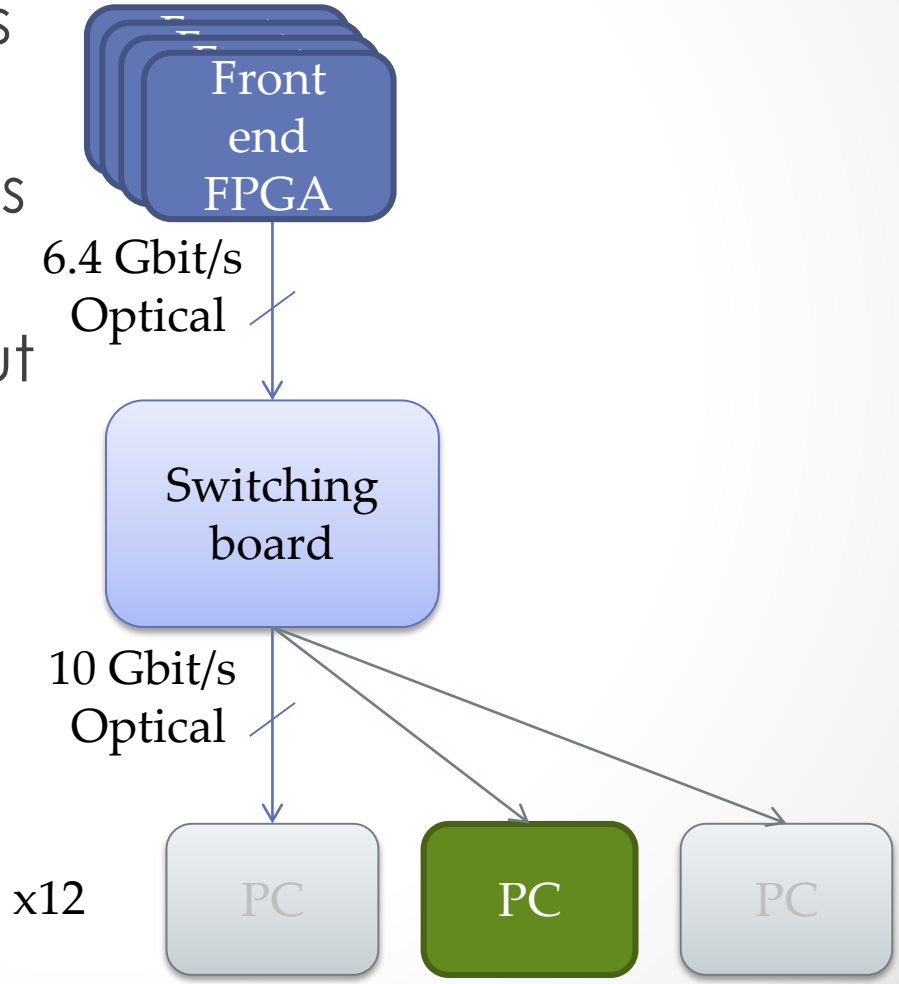
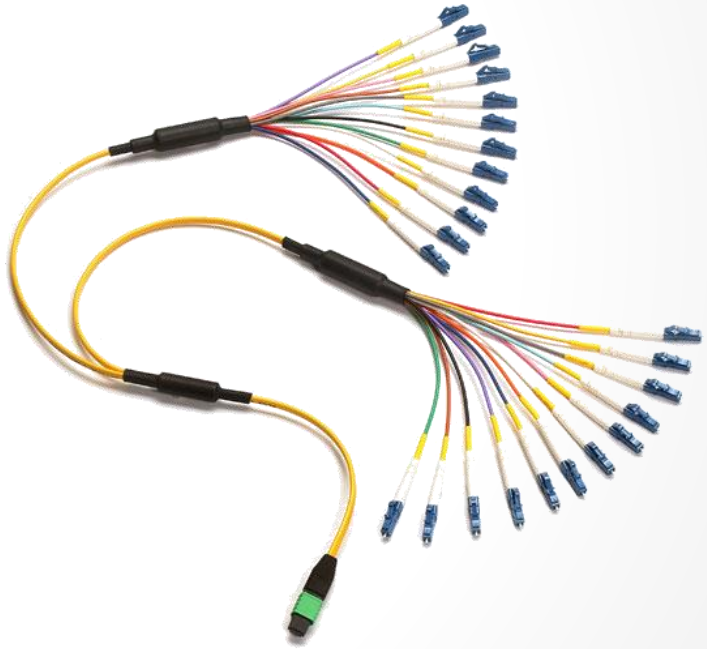


Trigger-less DAQ

- Front end links
  - Pixel sensor to on-detector FPGA
    - 1250 Mbit/s
    - LVDS
  - Timing detector readout
- Optical links from detector
  - Front end FPGAs
  - … to switching boards
  - 6.4 Gbit/s
- Optical links in counting room
  - Off-detector read out boards
  - …to PC Farm



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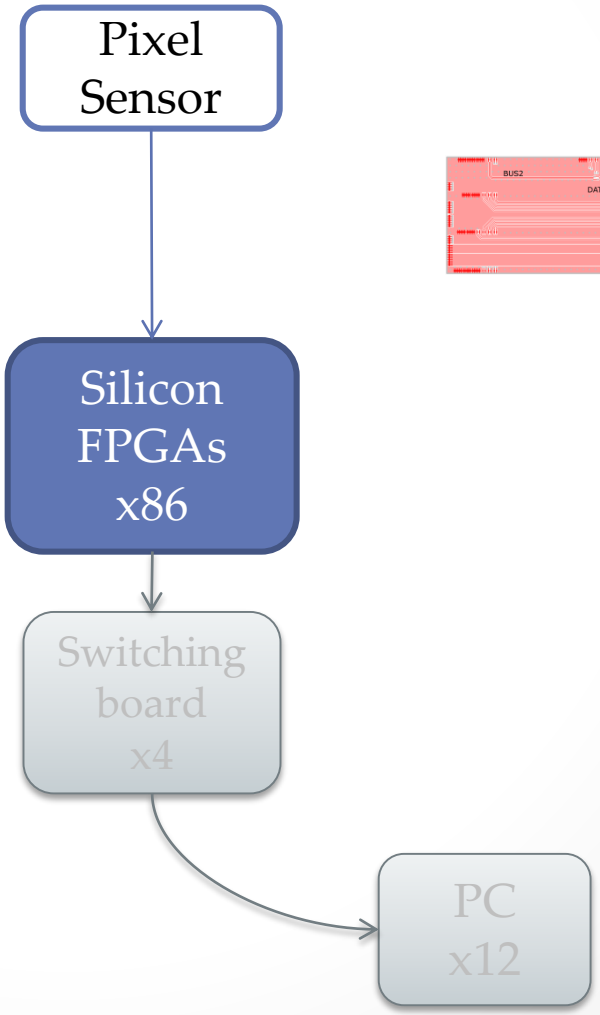

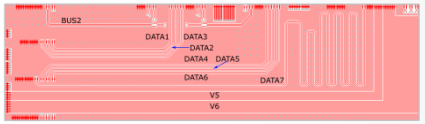

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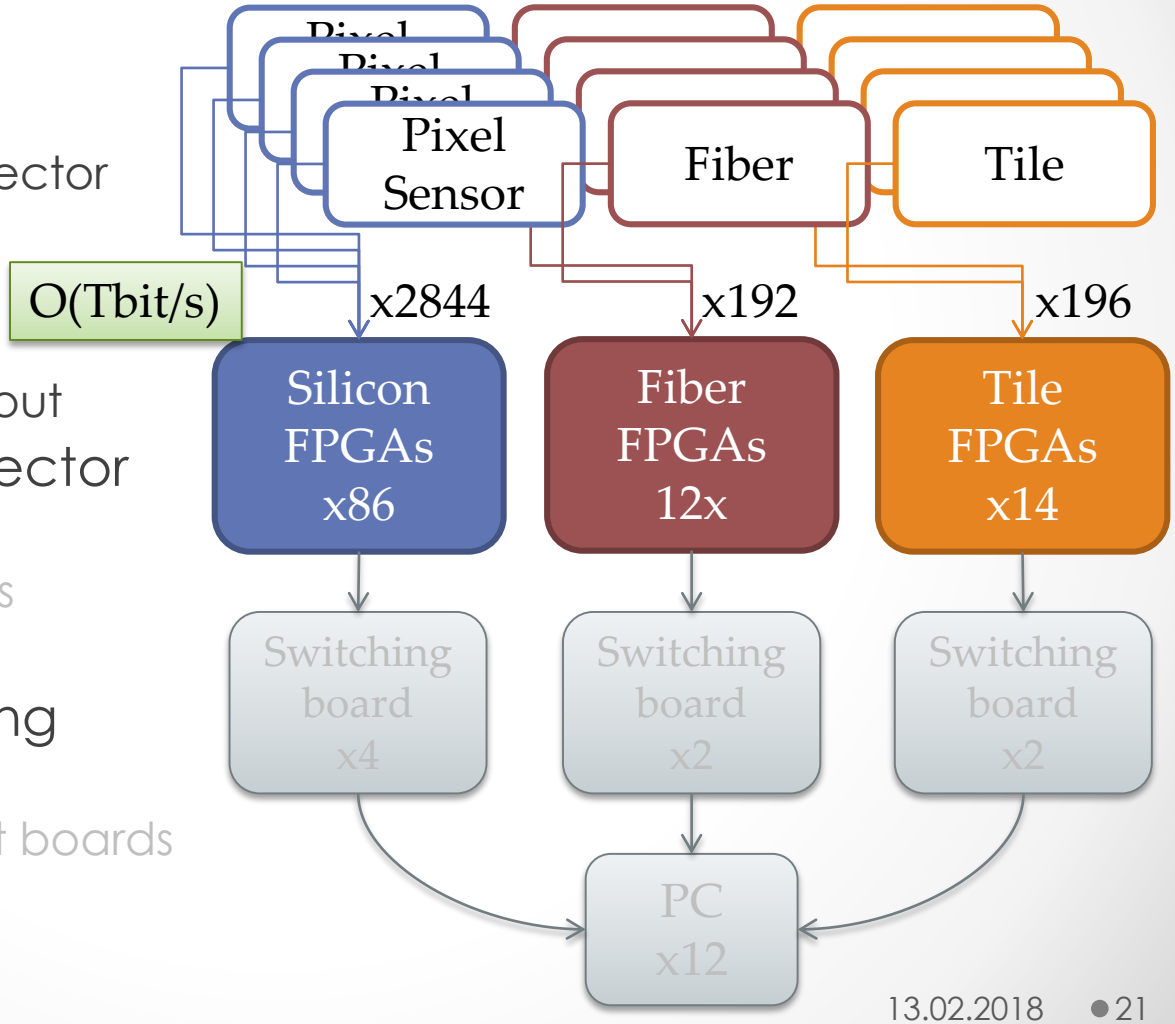

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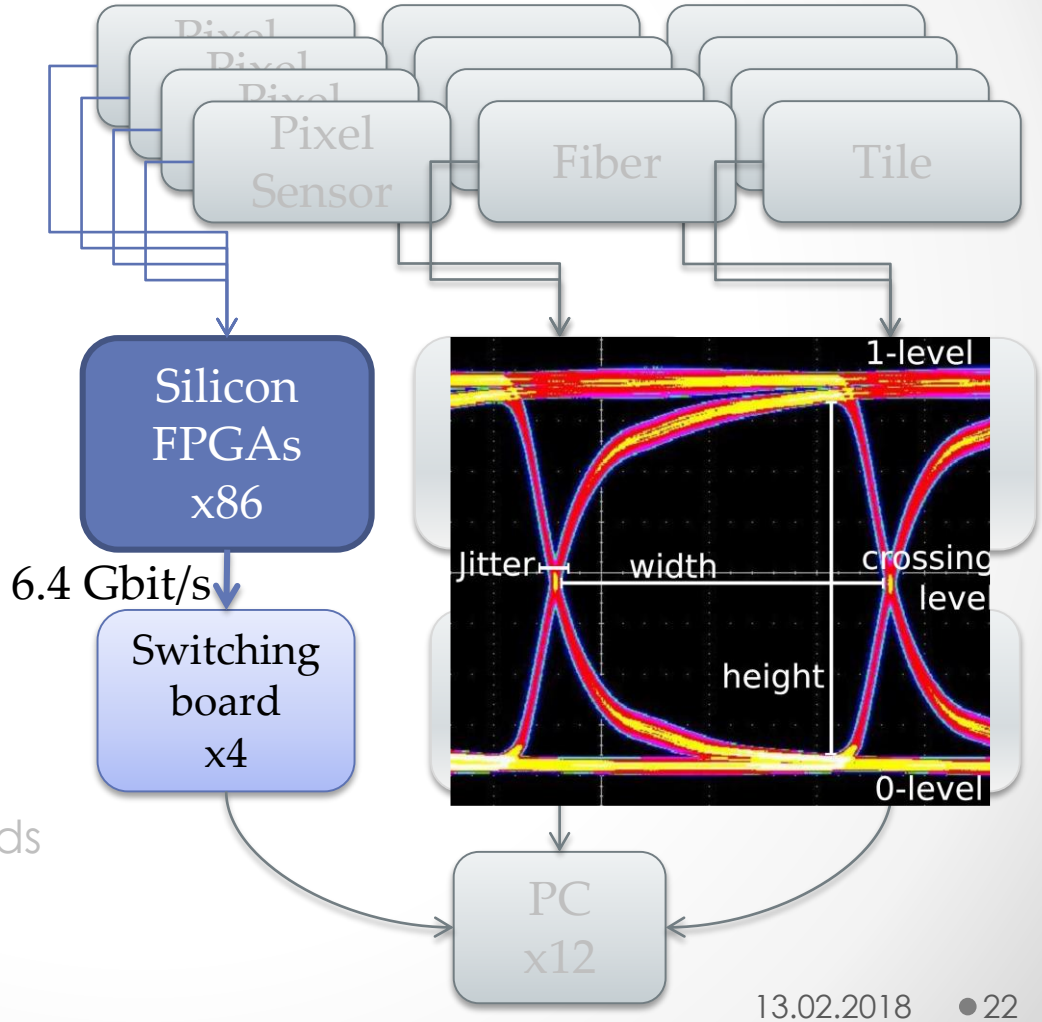
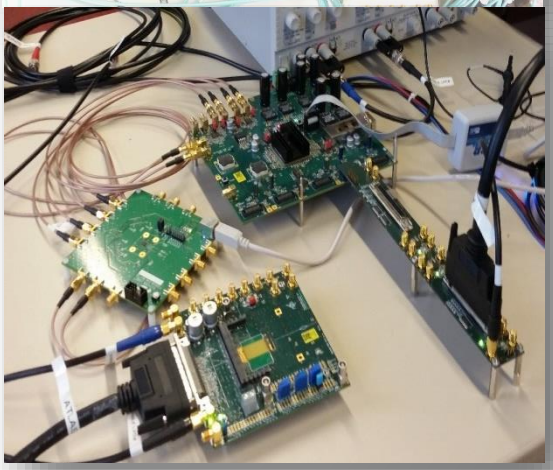
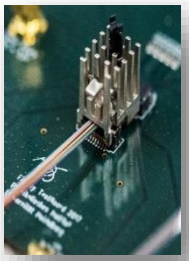
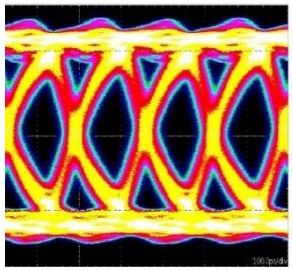


Readout Vertical Slice Test

- ✓ Control and readout firmware of MuPix sensors
- ✓ Optical links tested intensively: MiniPods, QSFP and Samtec Firefly
- ✓ Front end board to PC communication
- ✓ **Front end board MuPix8 readout NEW!**
- ✓ Optical clock distribution

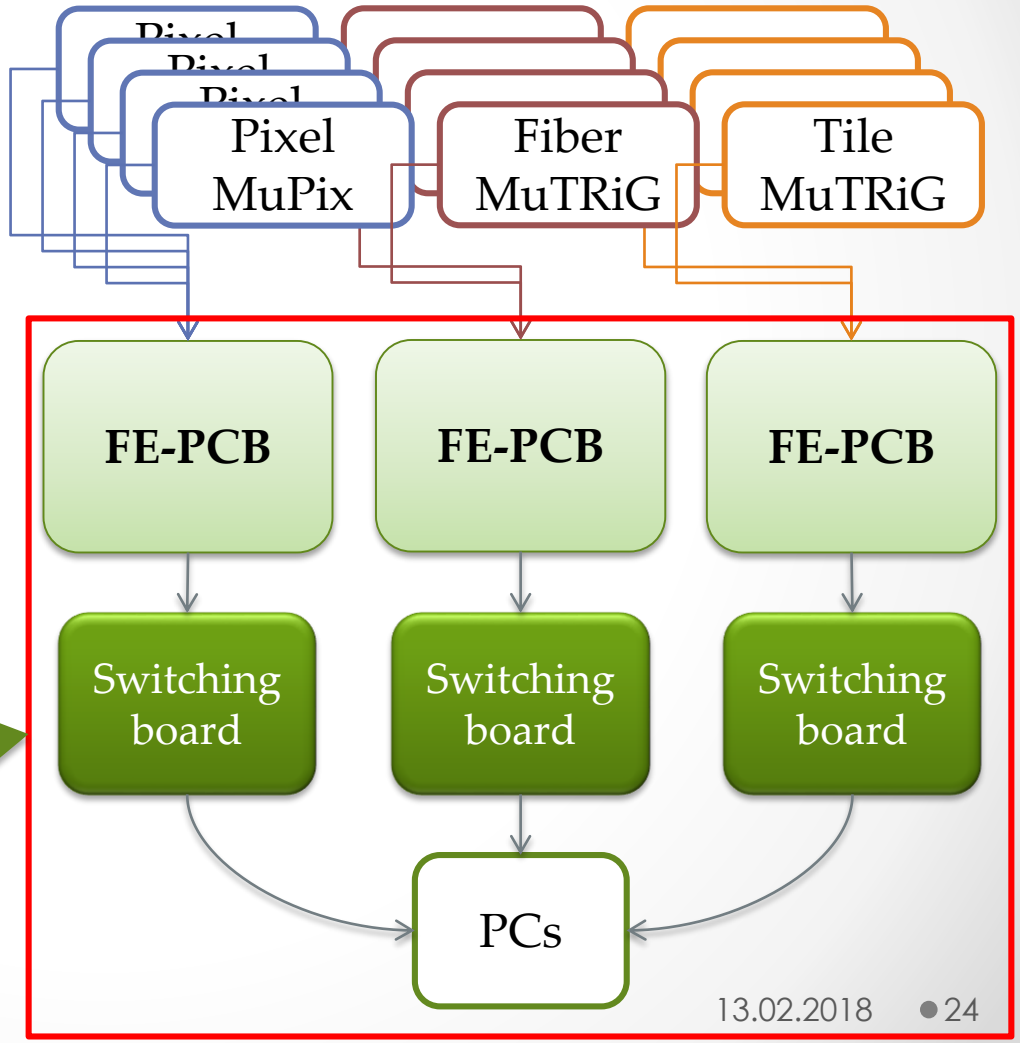






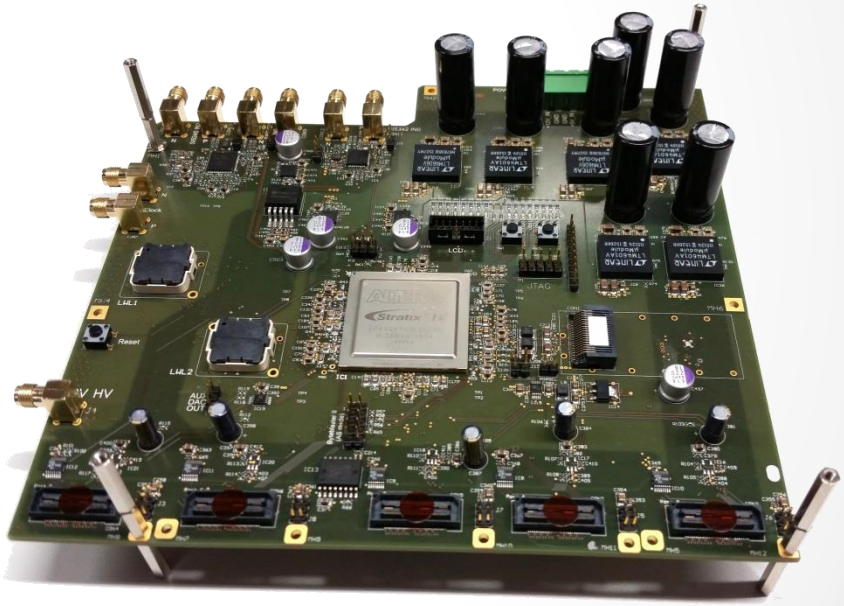
Readout System

- Pixel detector
  - HV-MAPS (MuPix)
    - ✓ Pixel detector system on one chip
    - ✓ Zero-suppressed serialized data
- Timing detectors
  - SiPMs plus MuTRiG
    - ✓ TDC system
    - ✓ Zero-suppressed serialized data
- **Common read-out system**



Common Read-out PCB

- ✓ **Front-end PCB**
  - Common for pixel, fibre and tile detector
  - ✓ Data acquisition
  - ✓ Clock distribution
  - ✓ Slow control distribution
- ✓ Prototype **functional**



Trigger-less DAQ

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    - 1250 Mbit/s
    - LVDS
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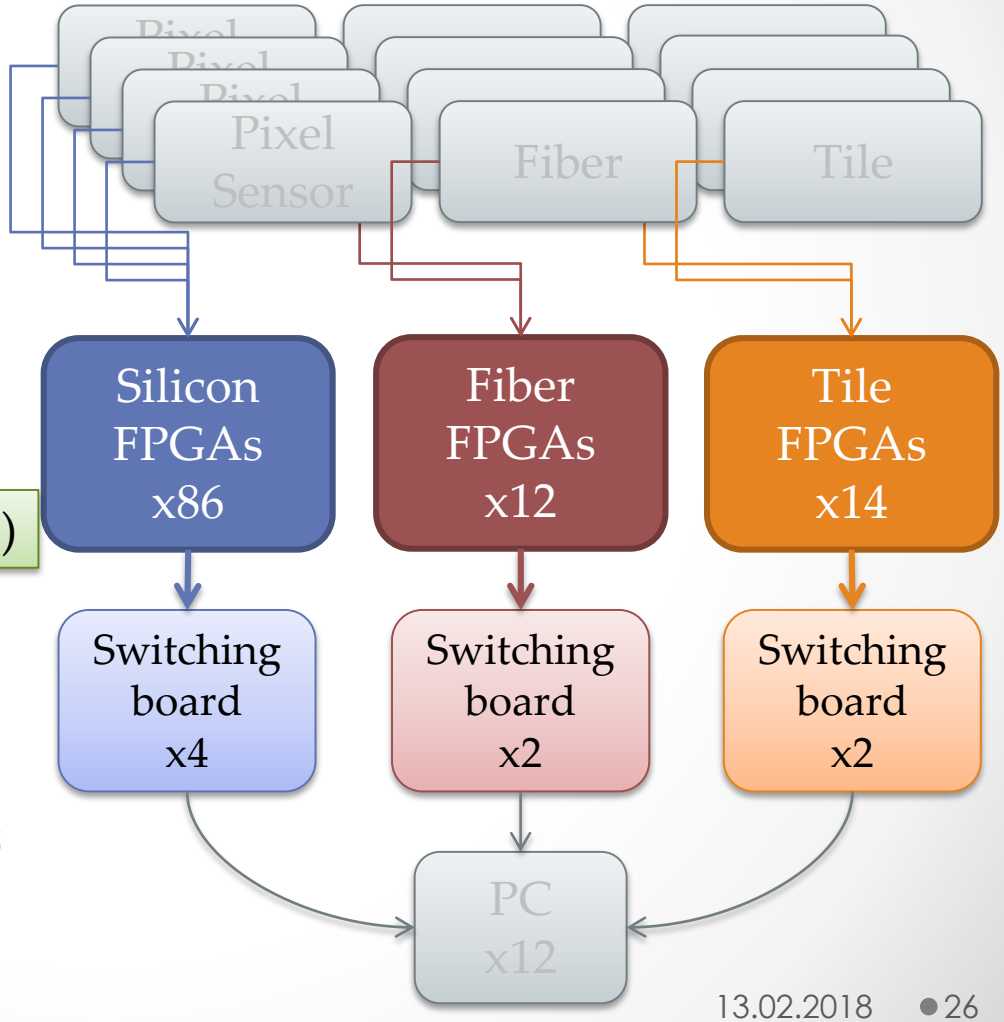
- Optical links from detector
  - Front end FPGAs
  - … to readout boards
  - 6.4 Gbit/s
- Optical links in counting room
  - Off-detector read out boards
  - …to PC Farm

O(Tbit/s)



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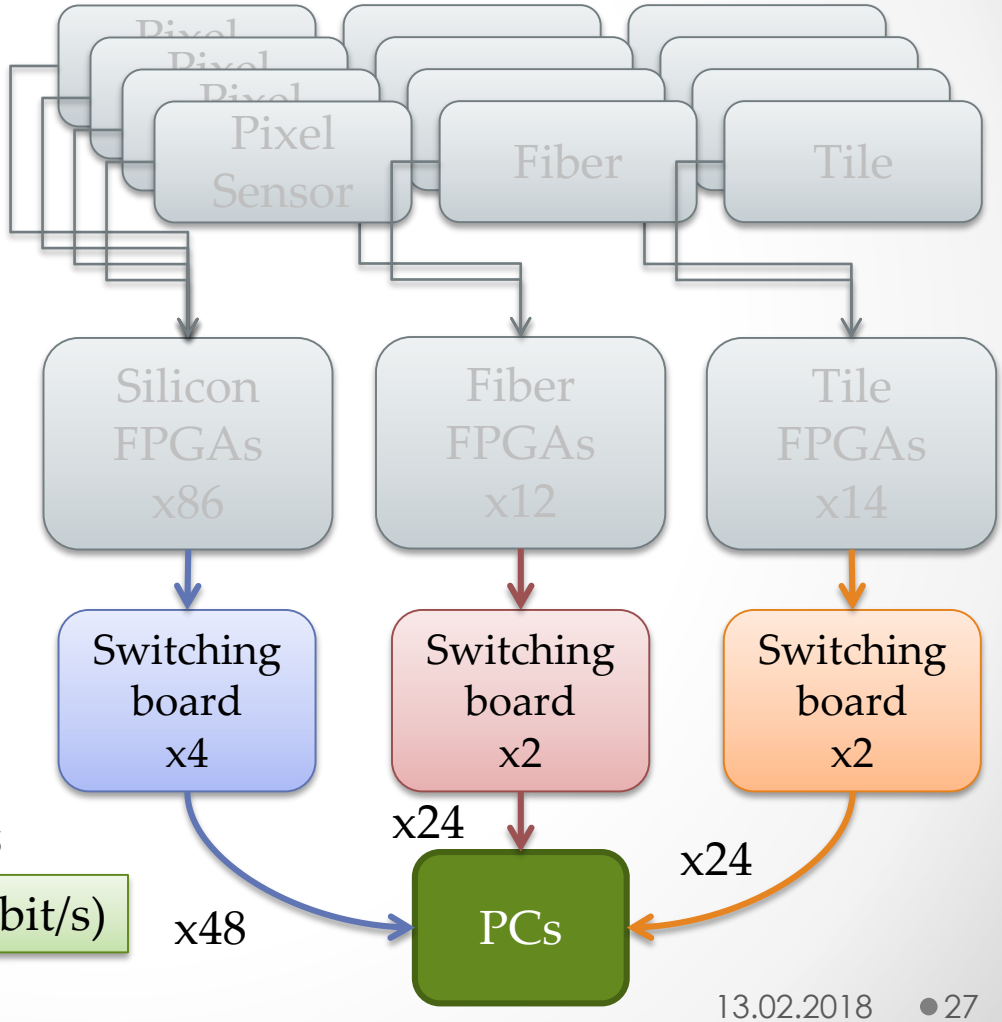

GPU-PC

- PC with GPU
- 10 Gbit/s Fiber input
  - 8 inputs from sub-detectors
- Data filtering
  - Timing Filter on FPGA
  - Track filter on GPU
  - Data to tape < 100 MB/s

GPU computer

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Optical mezzanine connectors

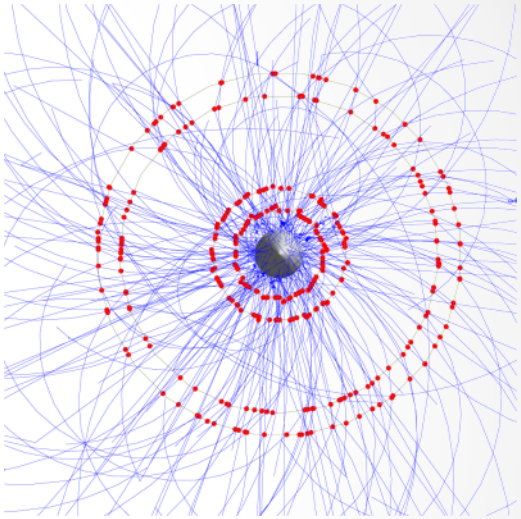
FPGA PCIe board

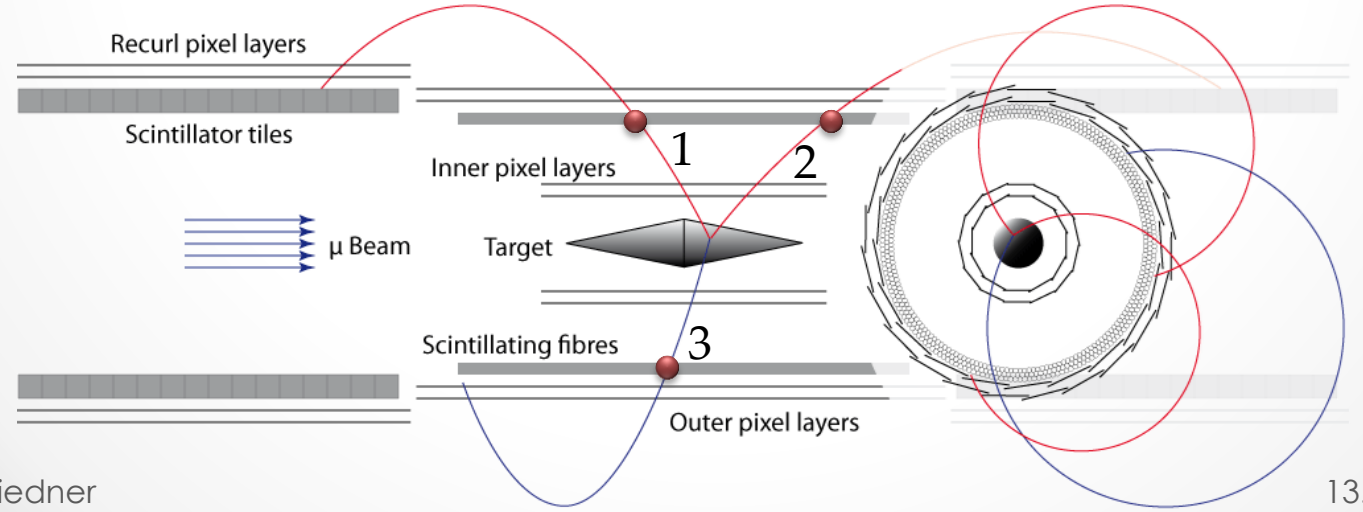
GPU computer

Timing Filter

Under discussion

- Entire event on PCIe FPGA
- Tile and Fiber data
  - Easy to match
  - Look for three tracks
- Reject data without three hits
  - … inside time interval





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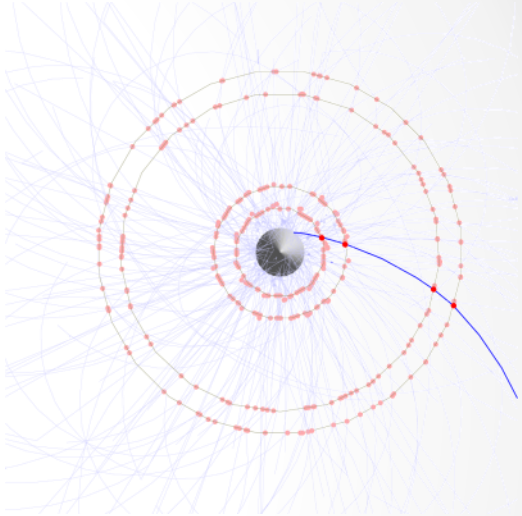
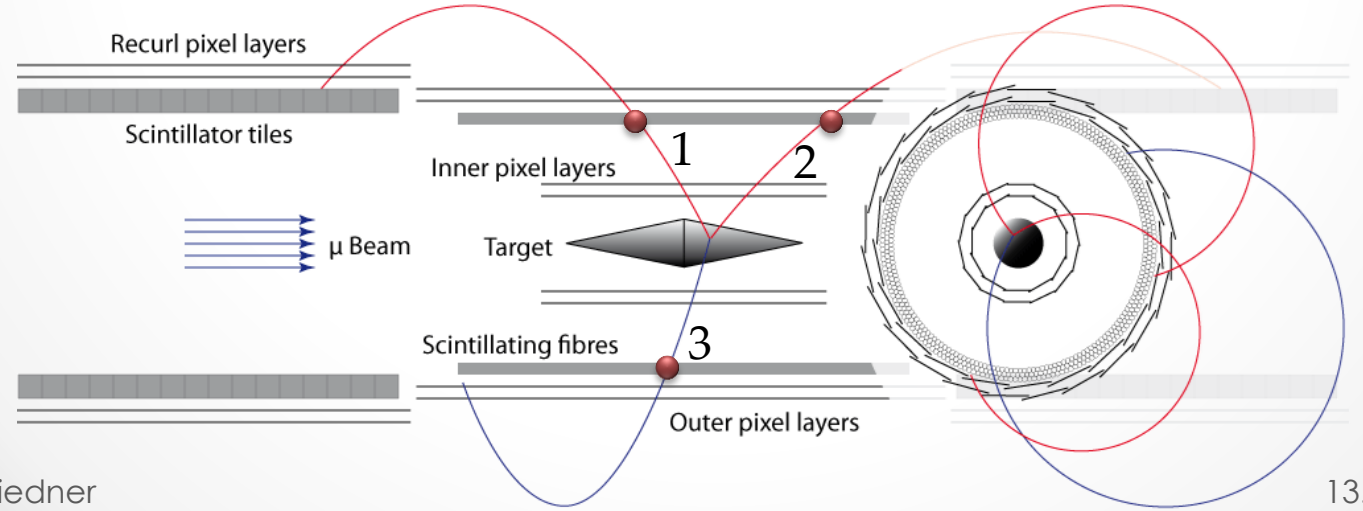
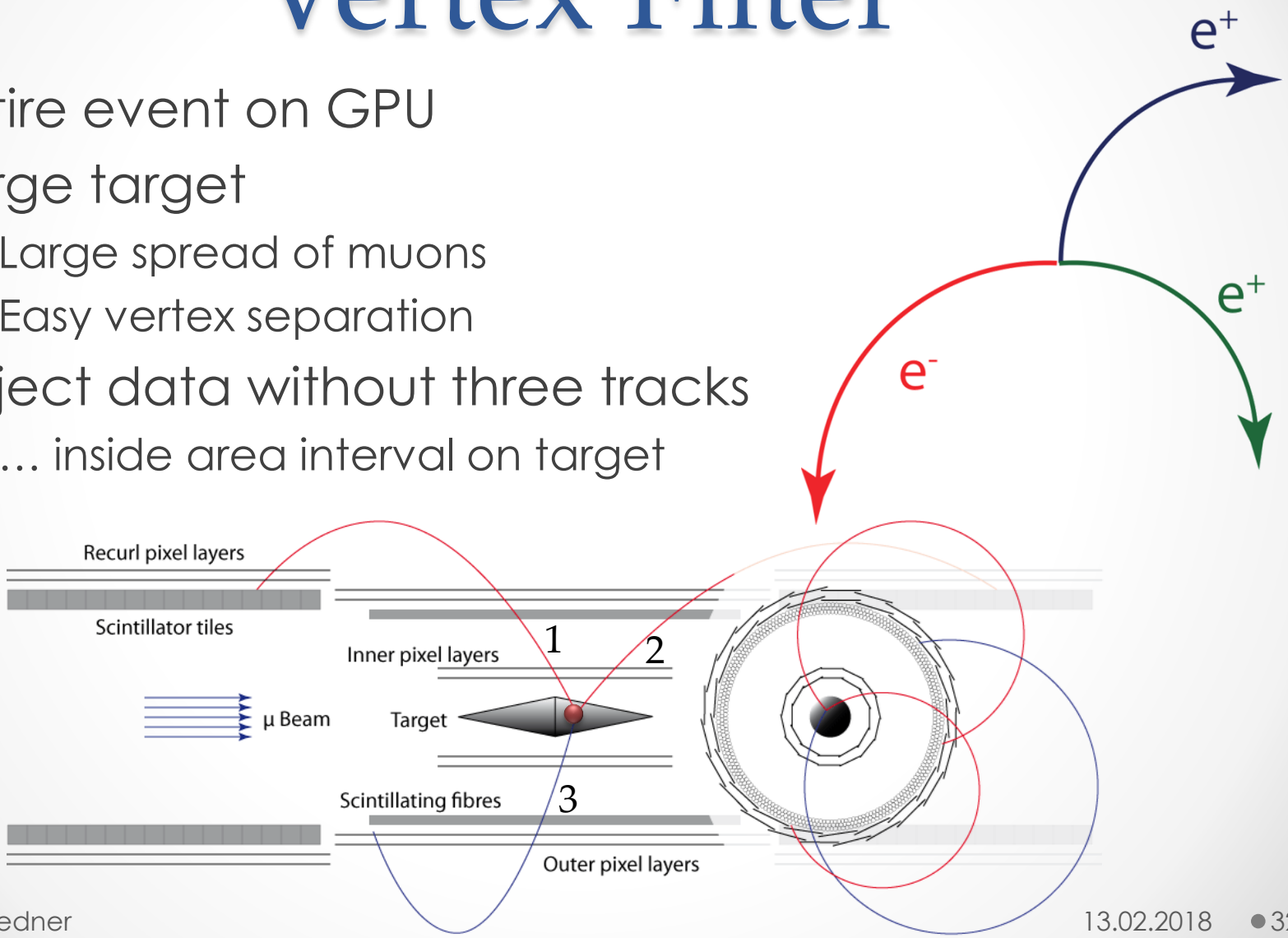




Vertex Filter

- Entire event on GPU
- Large target
  - Large spread of muons
  - Easy vertex separation
- Reject data without three tracks
  - … inside area interval on target



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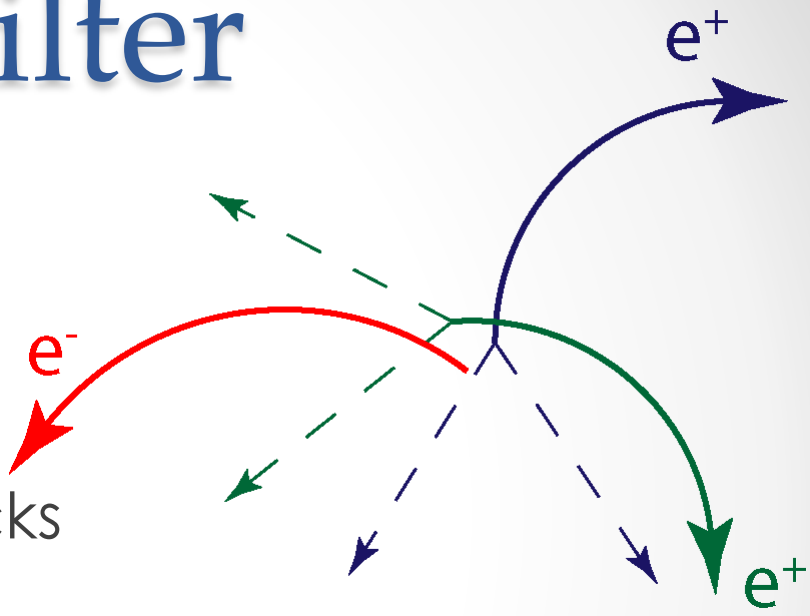
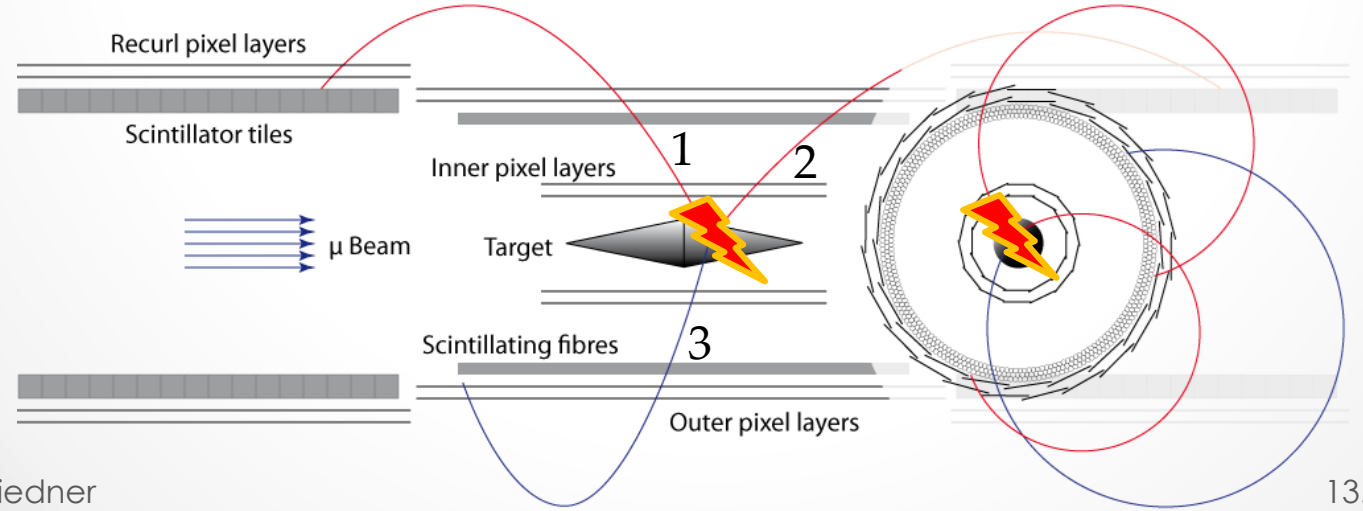
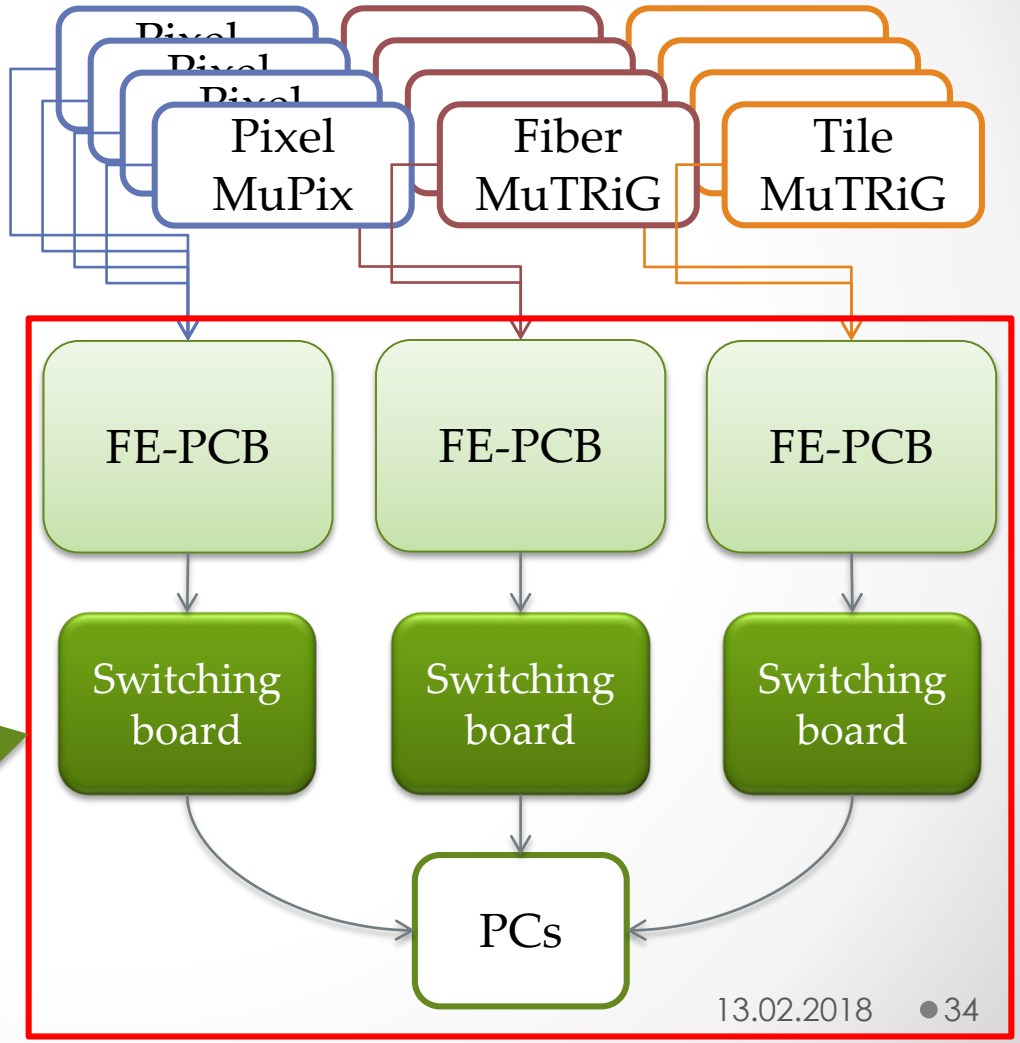




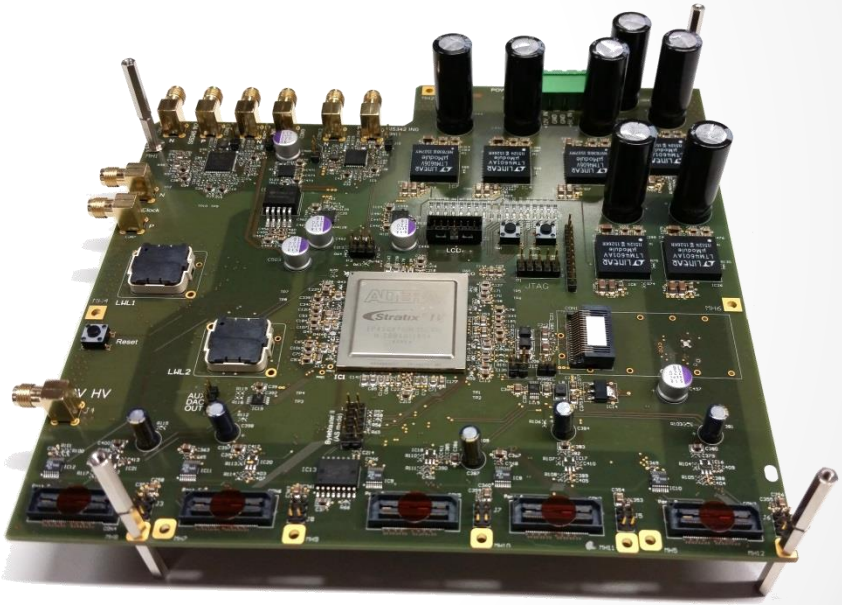
Readout system

- Pixel detector
  - HV-MAPS (MuPix)
    - ✓ Sensor and read-out chip in one
    - ✓ Deliver zero-suppressed serialized data
- Timing detectors
  - SiPMs plus MuTRiG TDC
    - Deliver zero-suppressed serialized data
- **Common read-out system**



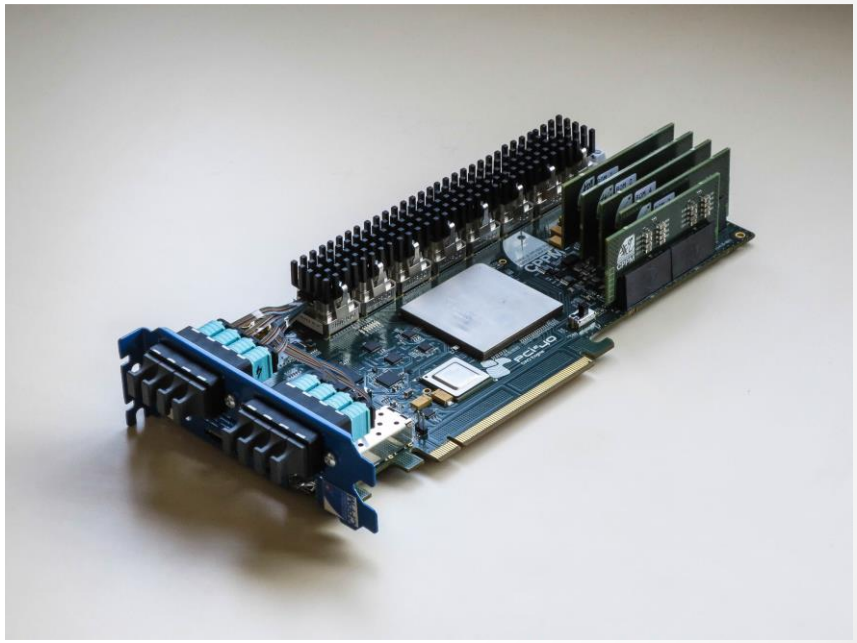
Common read-out PCB

- ✓ **Front-end PCB**
  - Common for pixel, fibre and tile detector
  - ✓ Data acquisition
  - ✓ Clock distribution
  - ✓ Slow control distribution
- ✓ Prototype **functional**
  - Improved version for Q3/2017
- Next: Vertical slice test:
  - All electronics from (pixel) module to PC



Switching Board

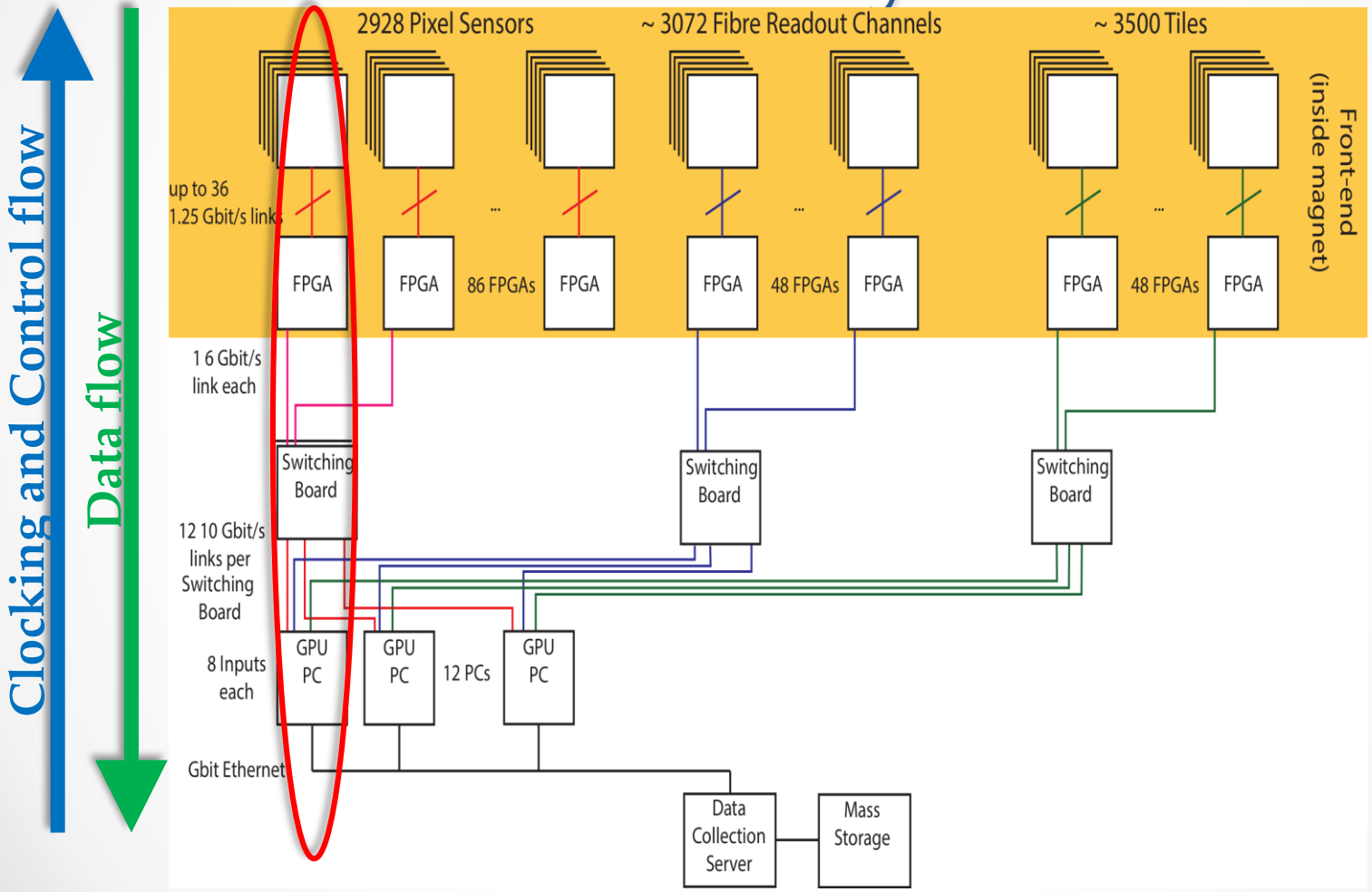
- PCIe40
- Developed for LHCb and ALICE upgrade by CPPM (Marseille)
- 48 optical I/Os
- Optcial network switch fro Mu3e filter farm
- Mu3e will receive samples from the current production



Receiving FPGA board PC side

- De5a-NET boards from Terasic
- Successfully tested at Mainz
- 8 out of 12 boards already acquired

Vertical slice of the Mu3e readout system



Tasks, problems, challenges

```
write_process : process(clkin, reset_n)
begin
   if(reset_n = '0')then
```

```
void MudaqDevice::zero_wrmem()
{
    uint32_t temp;
```

- Hard-, firm- and software developments
- Testing custom designed front-end boards and bringing them to operation
- Data transmission studies
  - Electrical links
  - Optical links
- Data reduction at front-end:
  Up to 45 × 1.25 Gbps → 1 × 6 Gbps
  with as little logic utilization as possible