Powering status

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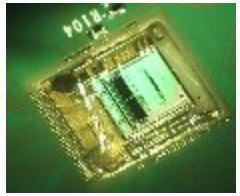
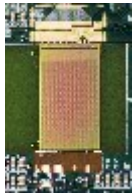
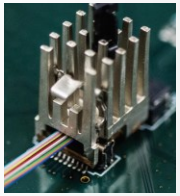
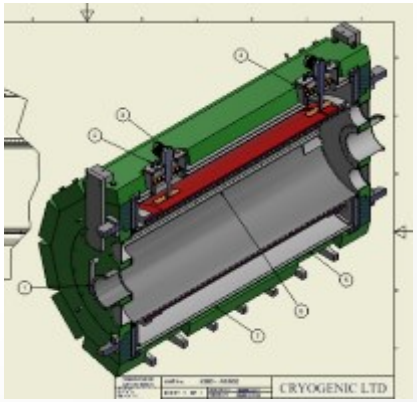
Introduction

- Low voltage requirements:
  - 10kW of power
  - Clean analog 1.8V for ASICs MuPix and MuTRiG
  - Clean digital 1V-3.3V for FPGAs and optoelectronics
- Dense environment
- He enclosure
- 1T magnetic field



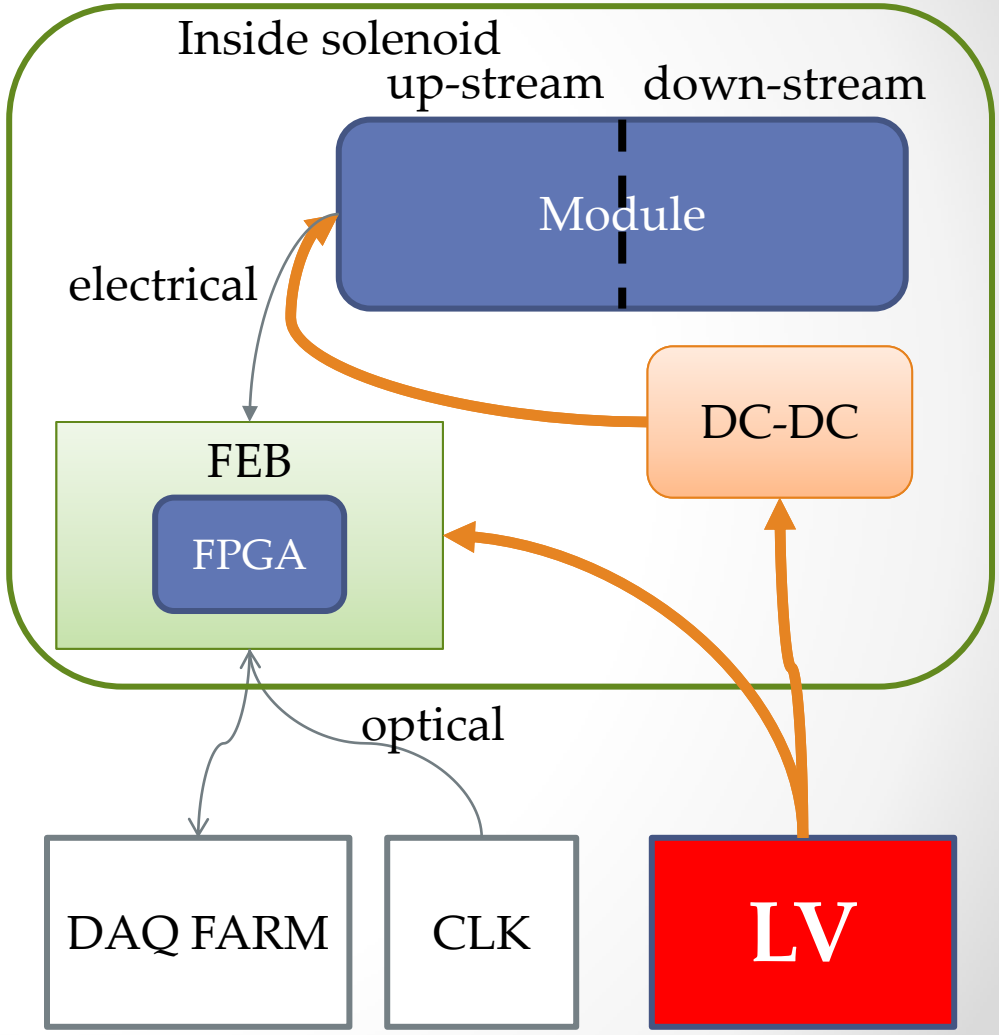






Detector Partitions

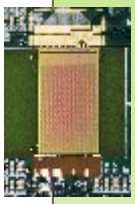
- Half module corresponds to partition
- Modules read-out on both ends
- One front end board (FEB) per partition
- One low voltage per partition
- One high voltage per partition
- 112 partitions in total
  - +8 spares



Pixel Partitions

- MuPix requires 1.8V
  - 400 mW/cm^2
  - 1.6W/chip x 2844
- Extra components
  - FE-FPGA
  - LVDS repeater
  - Optical transceiver
  - Clock chips
- Loss in DC-DC

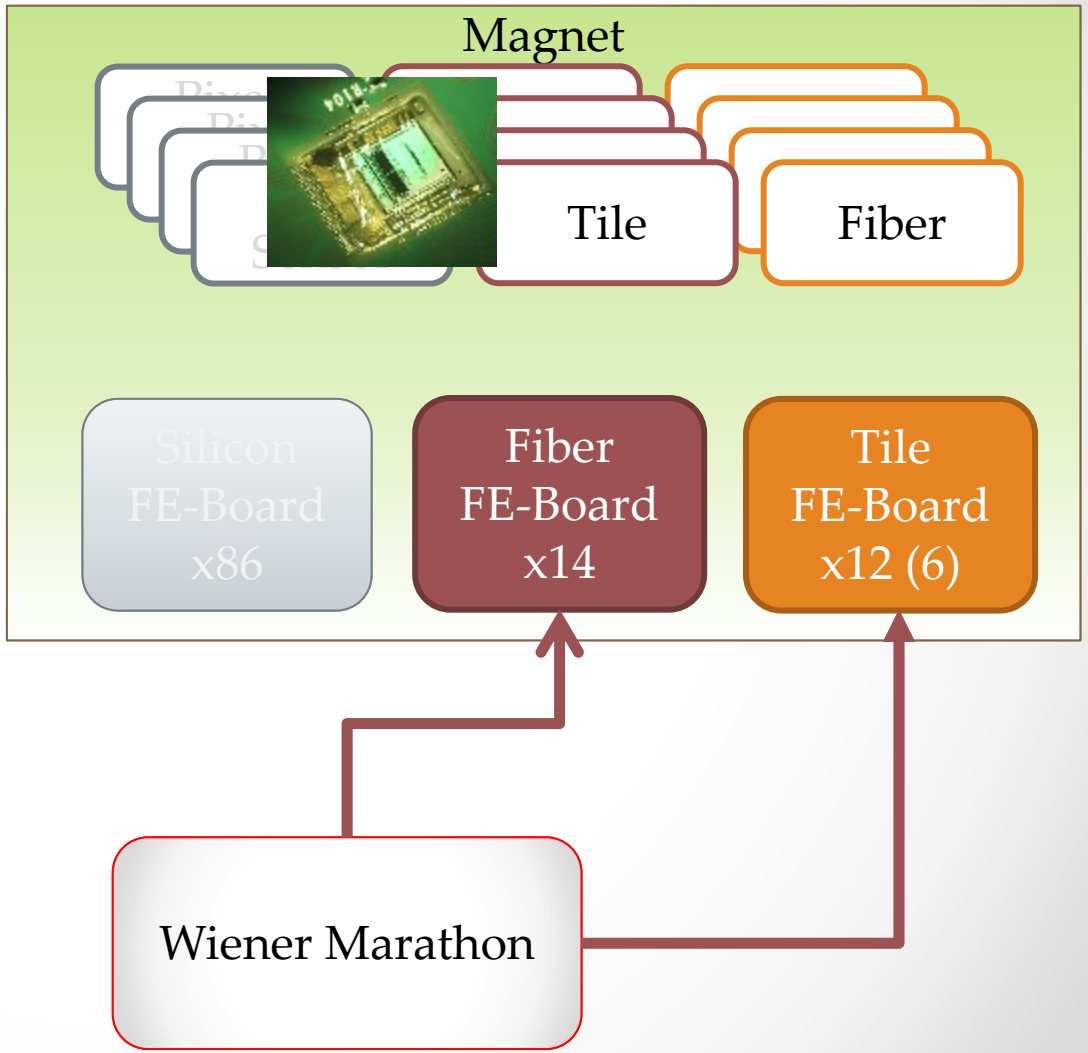
➢ Ca. 9kW total



Tile and SciFi Partitions

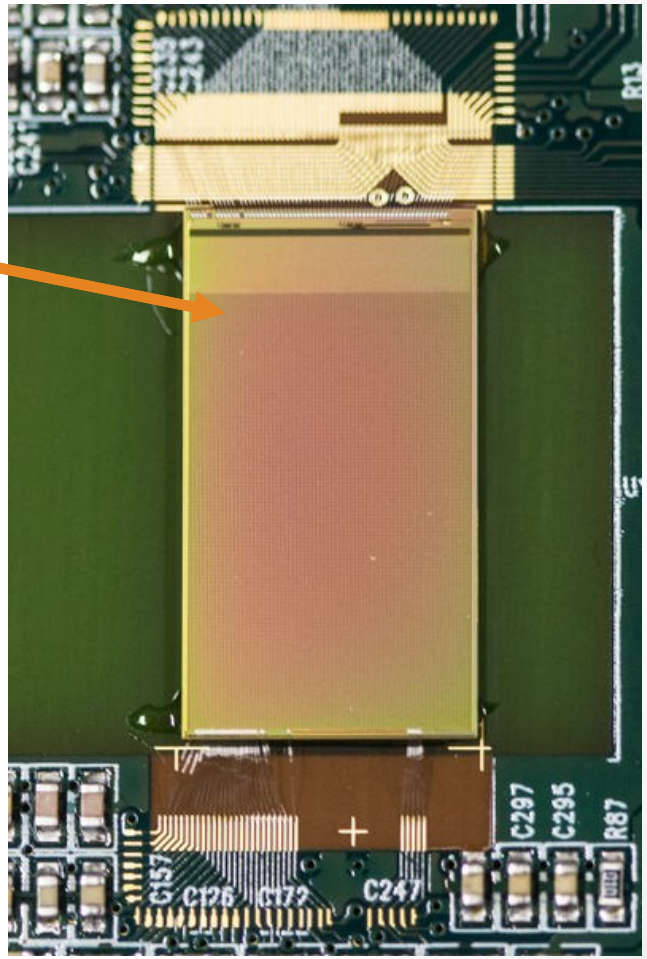
- MuTRiG requires 1.8V
  - 1.2W/chip x 292
- Extra components
  - FE-FPGA
  - LVDS repeater
  - Optical transceiver
  - Clock chips
- Loss in DC-DC

➢ Ca. 1kW total



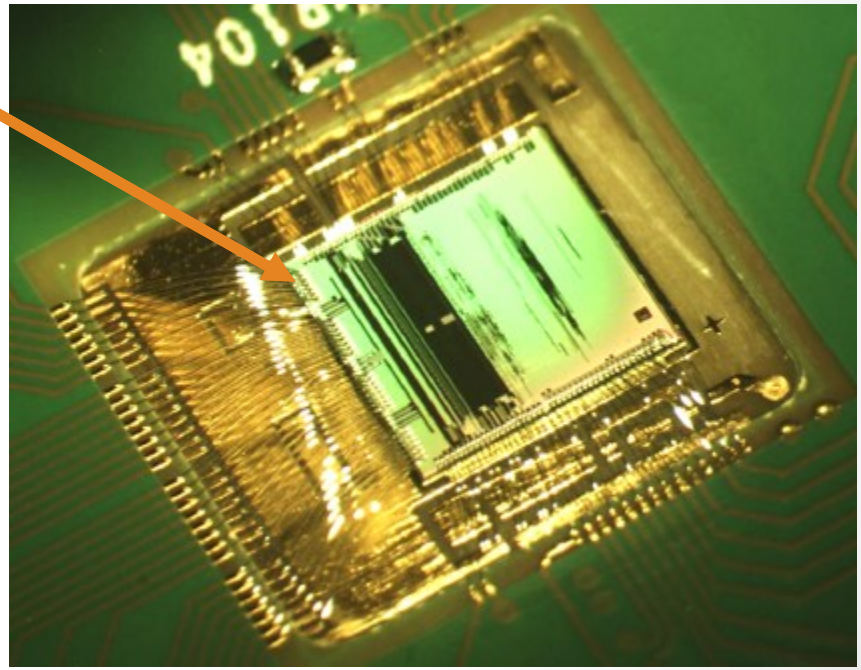
1.8V for MuPix

- MuPix8 (<0.25W)
  - VDD, VDDA1.8V++
  - VSSA 1V++
  - Performs well in test environment
- Production MuPix ≤1.6W
  - VDD=VDDA 1.8V
  - I_{in} ≤ 1A
  - Located on ultra light HDi
  - No extra capacitors at MuPix
- ≤57.6W/ partition
  - 32A @ 1.8V



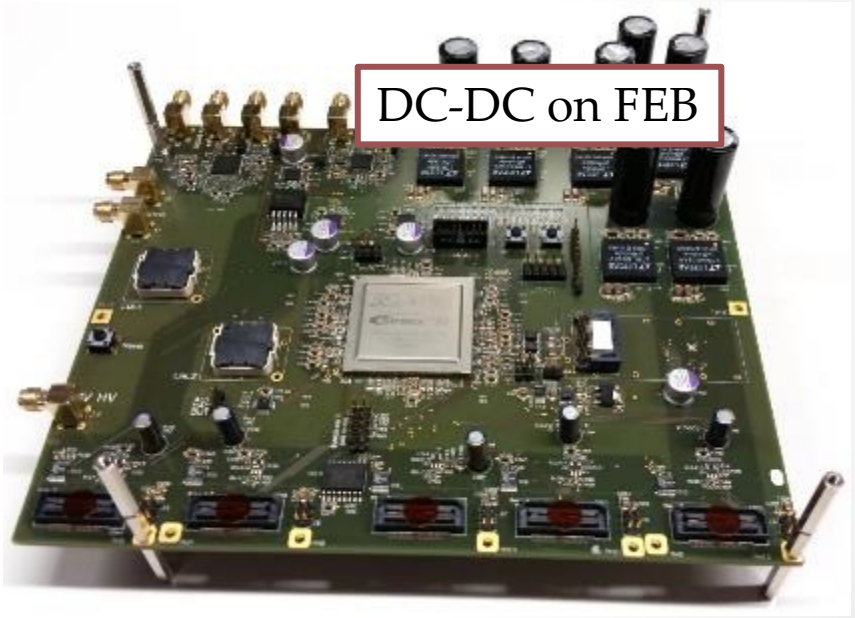
1.8V for MuTRiG

- MuTRig prototype (<2.1W)
  - VDD, VDDA1.8V
  - Performs well in test environment
- Production MuTRiG ≤1.2W
  - VDD=VDDA 1.8V
  - I_{in} ≤ 0.67A
  - Located on Cu-Flex with extra capacitors
- ≤16.8W per partition
  - ≤9.3A



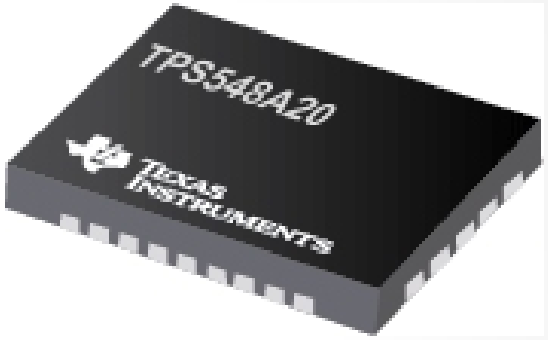
Front End Board V1.02

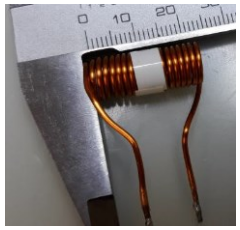
- Bug-fix of Front End Board V1.0
  - Extra resistors
  - Extra voltage regulator
- DC-DC for entire partition
- Eight PCBs produced
  - Tested and ok

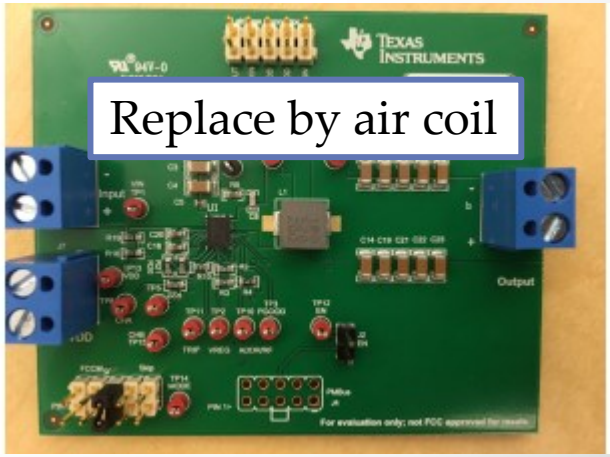


DC/DC Mainz

- DC-DC Board
  - MAINZ DC-DC
  - ✓ Based on TI chip set **TPS548A20**
    - ✓ 4.50 mm x 3.50
    - ✓ VQFN-CLIP (28)
    - ✓ Plus air coil
  - ✓ $V_{IN} \leq 20V$
  - ✓ $I_{OUT} \leq 15A$
- Extra capacitors
- ✓ Eval. PCB running



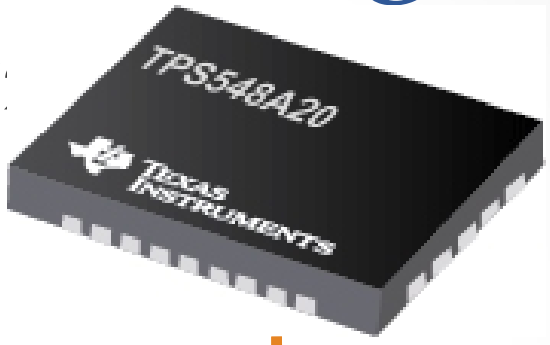


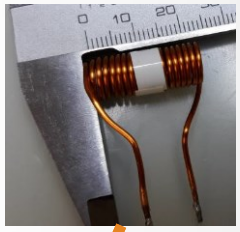


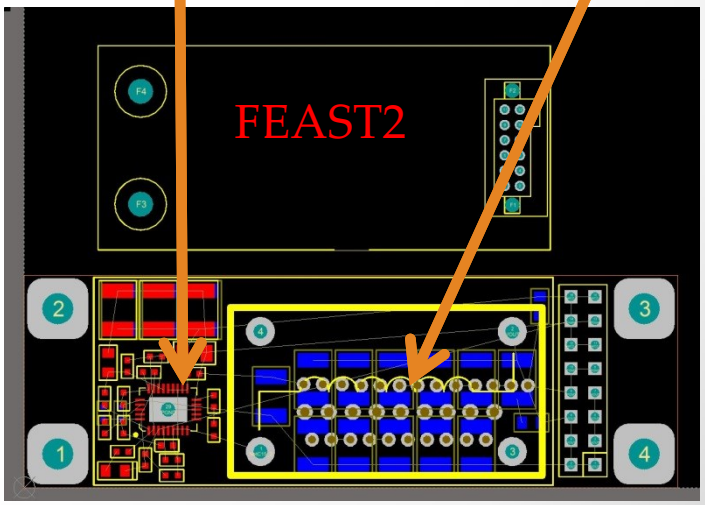
See Frederiks talk at the Mu3e May meeting

DC/DC Heidelberg

- DC-DC for Front End Board V
  - MAINZ DC-DC design
  - ✓ Based on TI chip set **TPS548A20**
    - ✓ 4.50 mm x 3.50
    - ✓ VQFN-CLIP (28)
    - ✓ Plus air coil
- Extra capacitors
- ✓ Layout make good progress
- Build separate DCDC board
  - Test with FEB V1.02
  - Use same layout with FEB 2.o

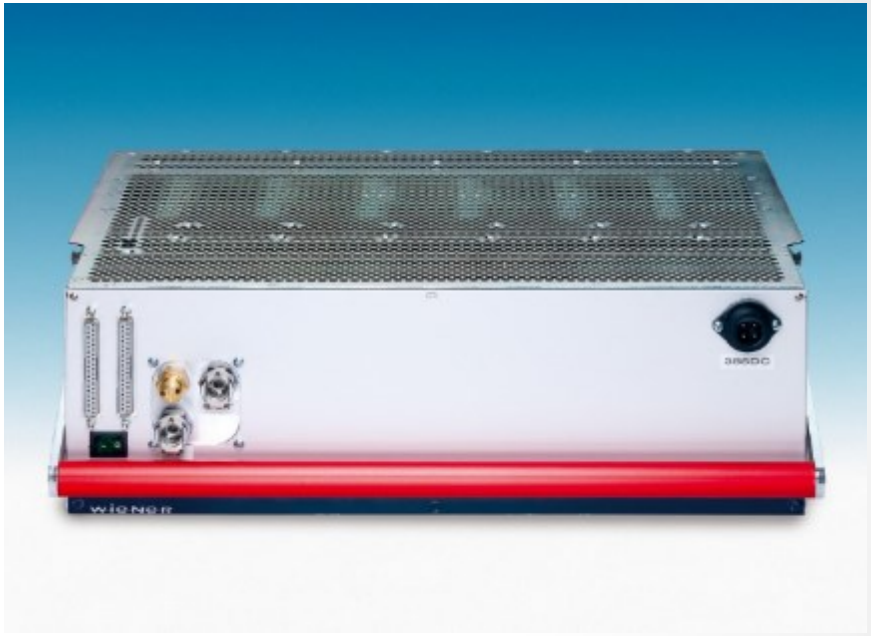


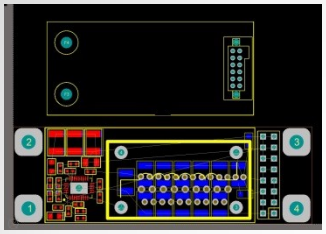




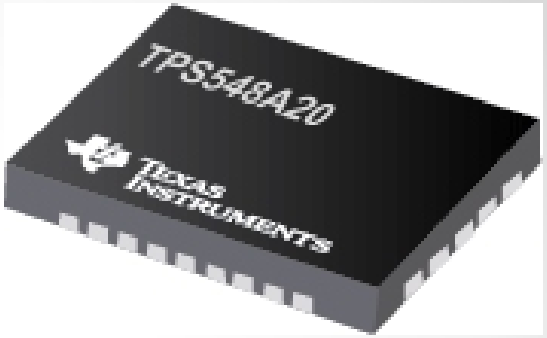
Power Supplies

- Wiener Maraton
- 10 crates
- 12 channels each
- Each channel:
  - 230W (330W)
  - 20V (12V)
  - 11.5A (22A)
  - Other versions available
- Water cooled
- Tolerate 30mT to 120mT magnetic field

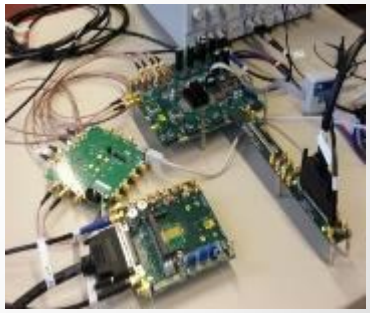




Summary



- >10kW Low voltage required
- 1.1V to 3.3V, mostly 1.8V (++)
- Mainz has tested alternative (TPS548A20 + air coil)
- Heidelberg DC-DC test board in layout
- Wiener MARATON as baseline



Outlook

- Test DC-DC with FEB V1.02
- Build FEB 2.0 with DC-DC
- Buy first Wiener MARATON Q1 2019

Backup Slides

Power Estimate

Detector	ASIC	#partitions	#ASICs/ partition	Sum ASICs [W]	Sum other [W]	Sum [W]	DC-DC [W]	Total [W]
Pixel				per partition				
Layer1	MuPix	4	12	19.2	21.2	40.4	69	231
Layer2	MuPix	4	15	24	21.2	45.2	77.5	258
Layer3	MuPix	3 x 12	32, 36	51.2, 57.6	21.2	72.4, 78.8	1166.4	3888
Layer4	MuPix	3 x 14	36	57.6	21.2	78.8	1418.4	4728
Fibre	MuTRiG	12	8	9.6	21.2	30.8	158.4	528
Tile	MuTRiG	14	14	16.8	21.2	38	228	760
Total		112						**10393**

Estimate update 27.02.2018

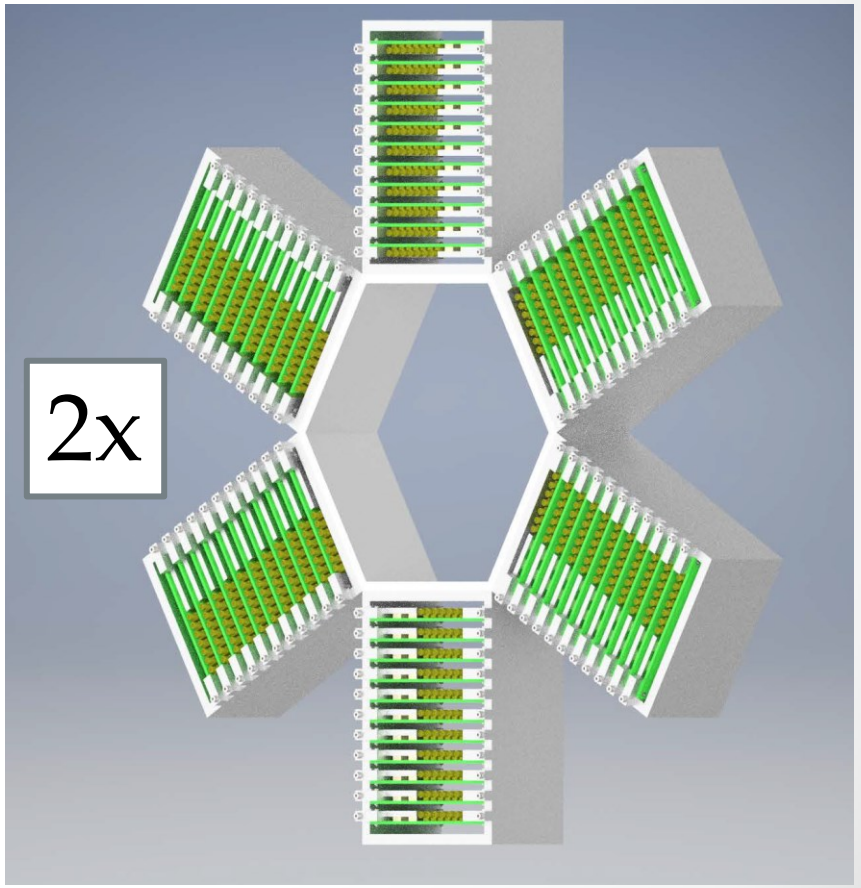
Power Estimate Components

Component	Quantity	Power [W]	Total [W]
MuPix	2844	1.6	4550
MuTRiG	292	1.2	350
ArriaV FPGA	112	10	1120
LVDS repeater	1344	0.6	806
Clock chip	224	1	224
FireFly	224	1	224

Estimate update 27.02.2018

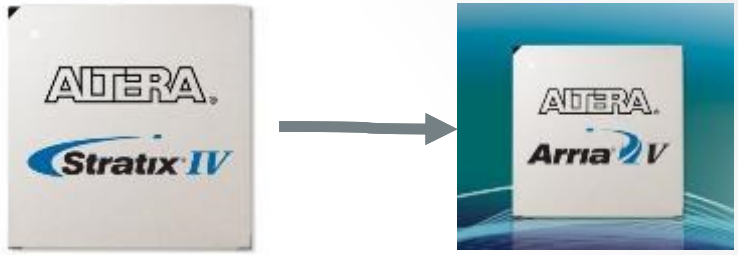
DC-DC-Crates

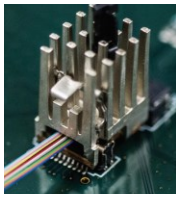
- DC-DC boards inside magnet
- 120 DC-DC boards in total
- Mounted in mini crates
- Star of crates
  - Upstream +
  - Downstream
- Water cooling

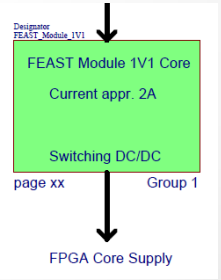


Front End Board V2.0

- Better FPGA
  - ArriaV instead of StratixIV
  - Lower power consumption
    - 6.6W → 3.3W (<10W)
- FireFly optical transceivers
  - 2 x 1W
- Clock distribution chips
  - SI5345 2 x 1W
- DC-DC only for FEB
  - FEAST2MD compatible

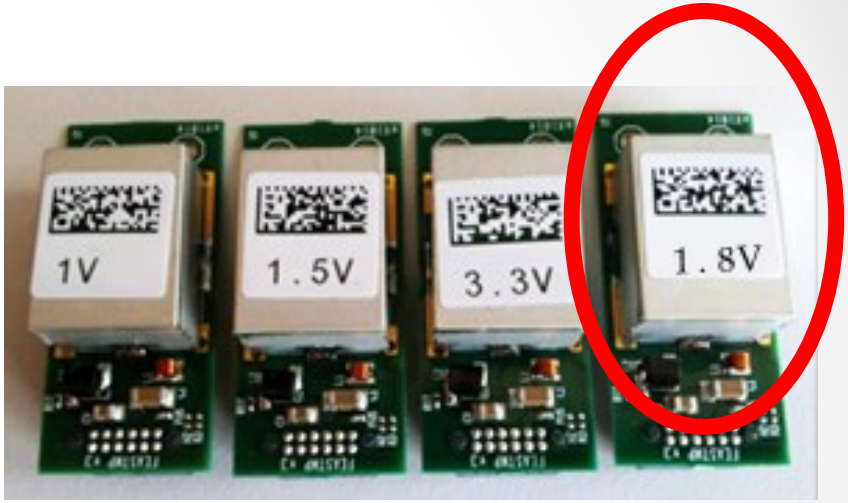


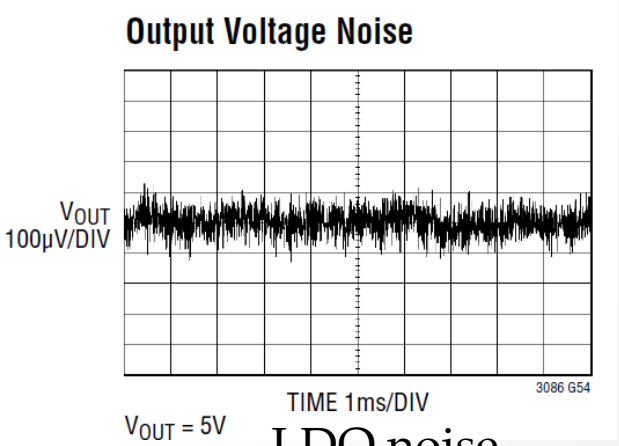




1.8V DC/DC FEAST2

- DC-DC Board
  - ✓ FEAST2 DC-DC
  - ✓ 1.8V version
  - ○ V_{IN}≤12V
  - ○ I_{OUT} 4A (2A rec.)
  - ✓ 2.5mV_{pk-pk} ripple
- Extra capacitors
- Linear Regulators
- LT3086 LDO
  - ○ >330mV drop
  - ○ I_{out} ≤ 2.1A
  - ✓ 40µV_{pk-pk} ripple
- ✓ We have it already
- ❑ BUT: up to 16 regulators per pixel partition

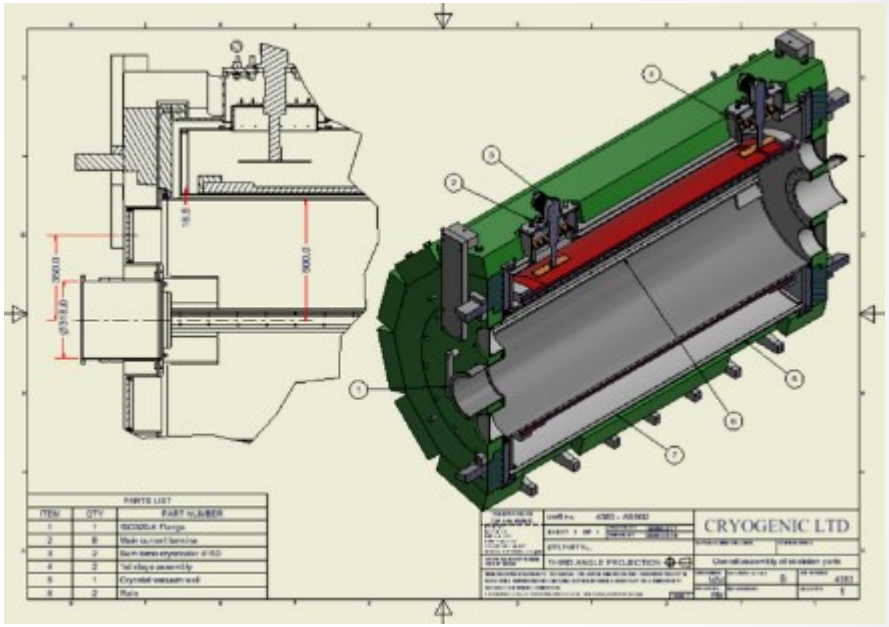




LDO noise

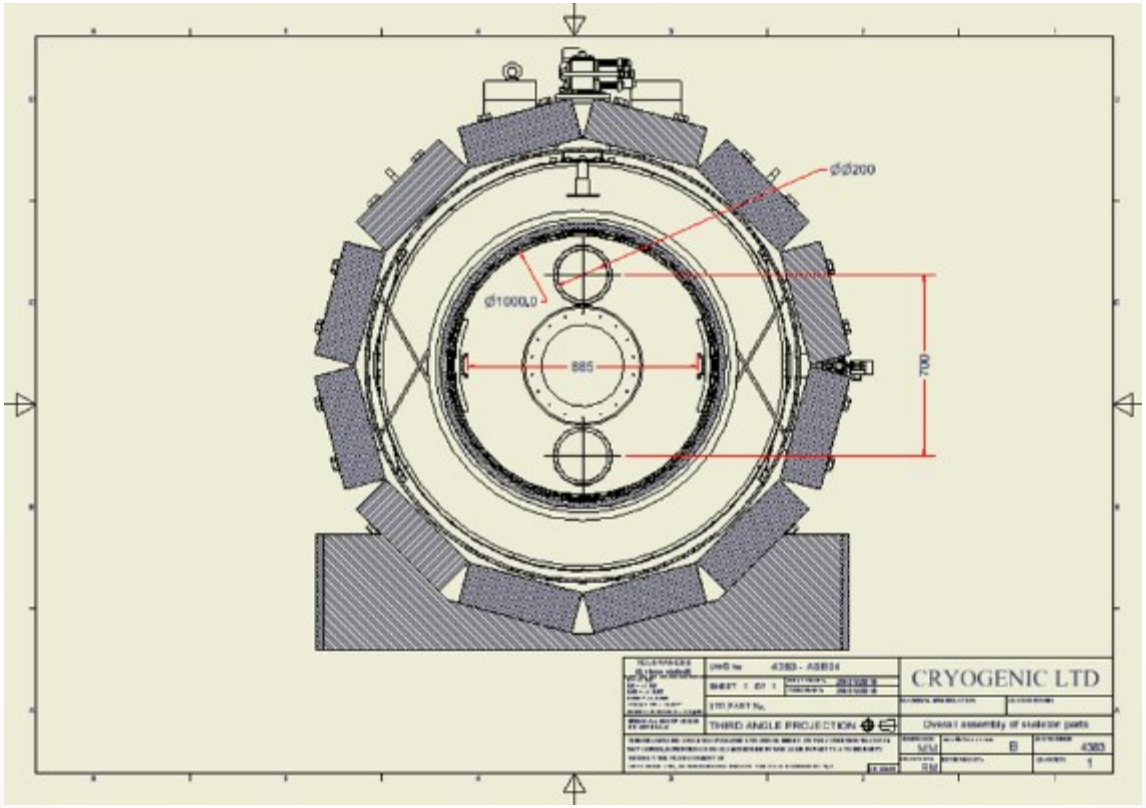
Mu3e Solenoid

- LV DC-DC inside magnet
- 1T field
  - No ferrite cores for coils
- He environment
- LV must be supplied through He tight endplates



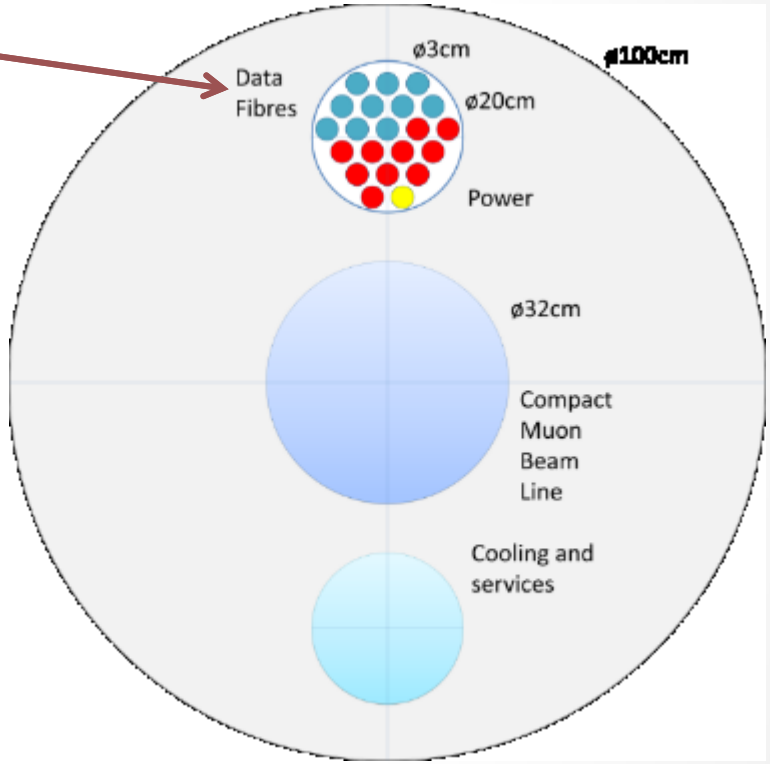
Mu3e magnet

Magnet End Plate Feed-through



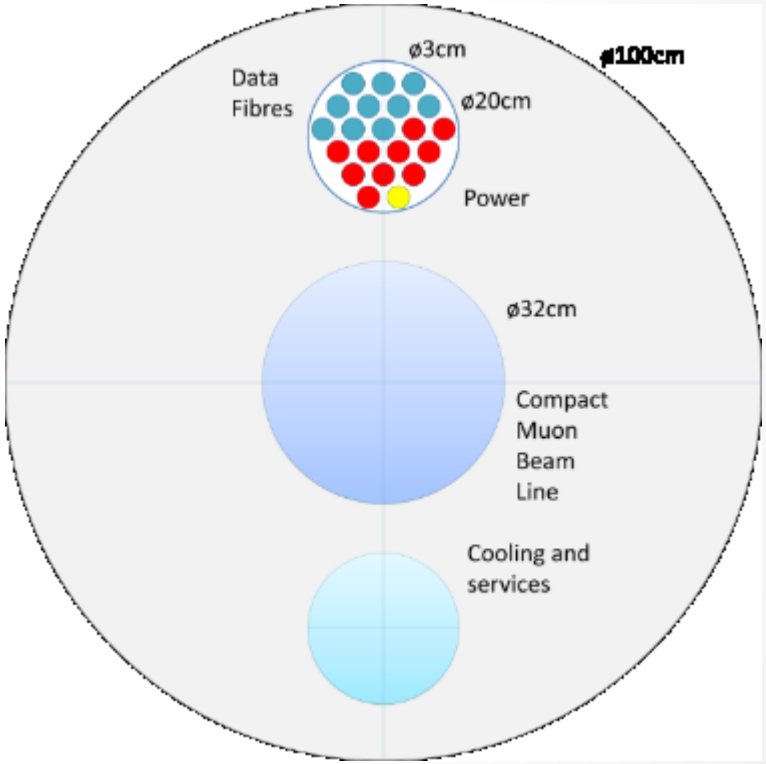
End plate design

- Data and power connectors
  - Gas tight
  - 120 detector partitions
  - One connector per 6 partitions
  - Each connector 3 cm diameter



End plate design

- Data and power connectors
  - Gas tight
  - 120 detector partitions
  - 20 connectors of each type
  - Each connector 3 cm diameter
  - Requires 2 x 20 cm ø
  - On plates



Racks

- piE5
  - ***Low Voltage rack***
  - Commissioning rack
- Skywalk platforms
  - Magnet power rack
  - Magnet compressor rack
  - Magnet control rack
  - Helium cooling rack
- Counting house
  - Filter farm racks
  - Clock and pixel slow control rack
  - Midas slow control rack

Sufficient rack space on skywalk platforms and in counting house

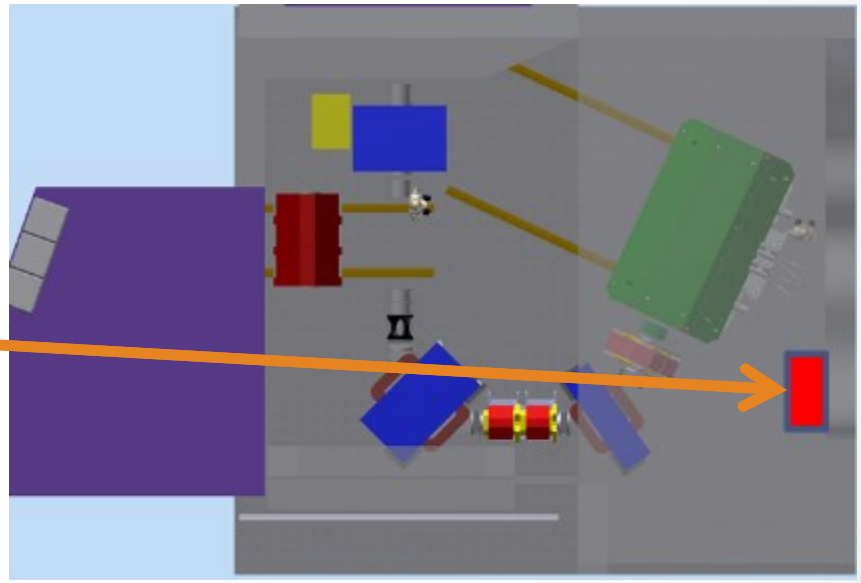
Area Planning

Good progress in terms of CAD, civil engineering for:

- ✓ Platforms
- ✓ Access ways
- ✓ Counting containers
- ✓ Power
- ➢ Cooling

Remark:

- Space in area **extremely** limited



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