Frontend board status

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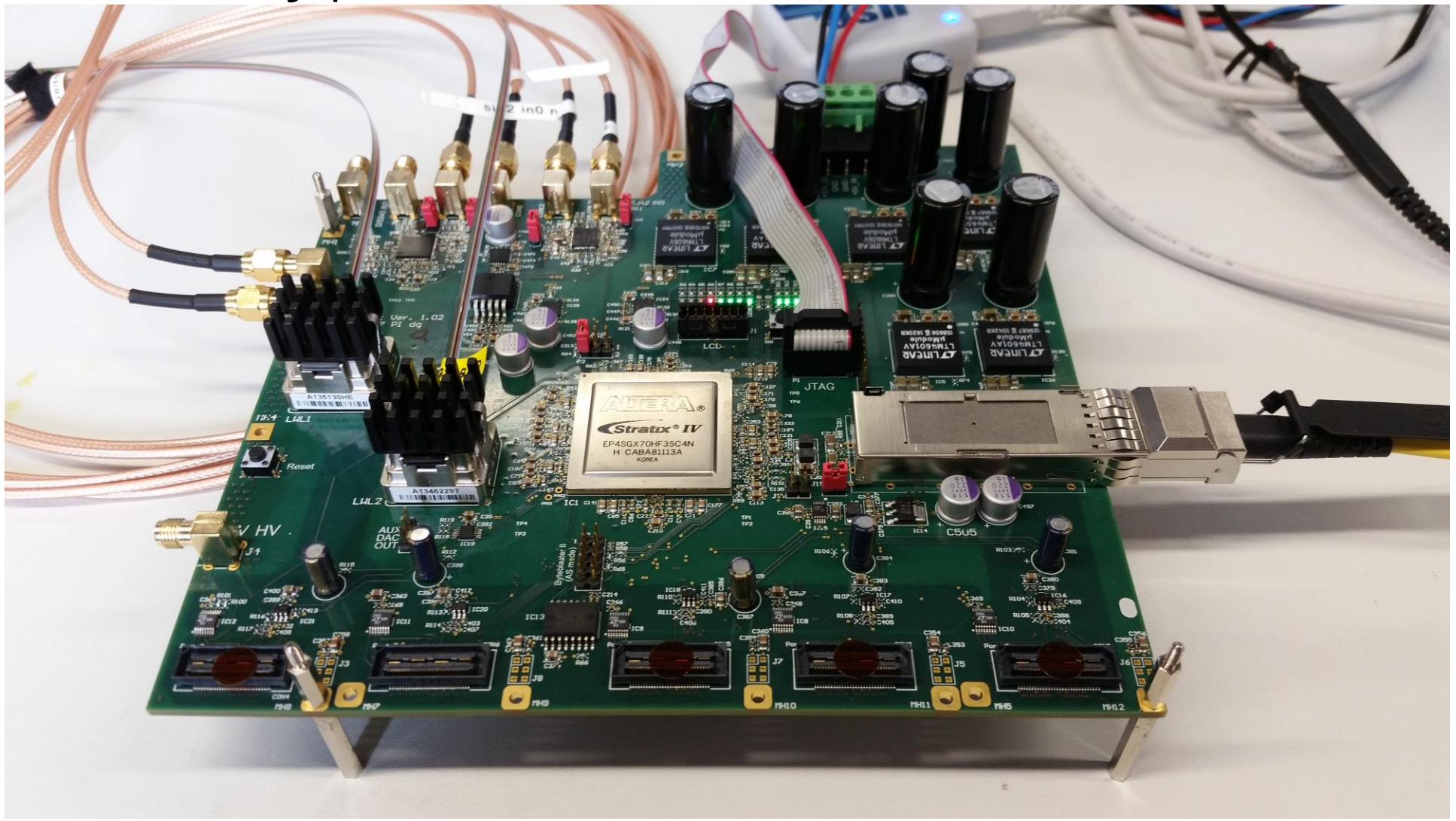
Mu3e integration meeting Geneva 2018

INTERNATIONAL MAX PLANCK RESEARCH SCHOOL PT FS FOR PRECISION TESTS OF FUNDAMENTAL SYMMETRIES

Prototype: Stratix IV Version 1.02



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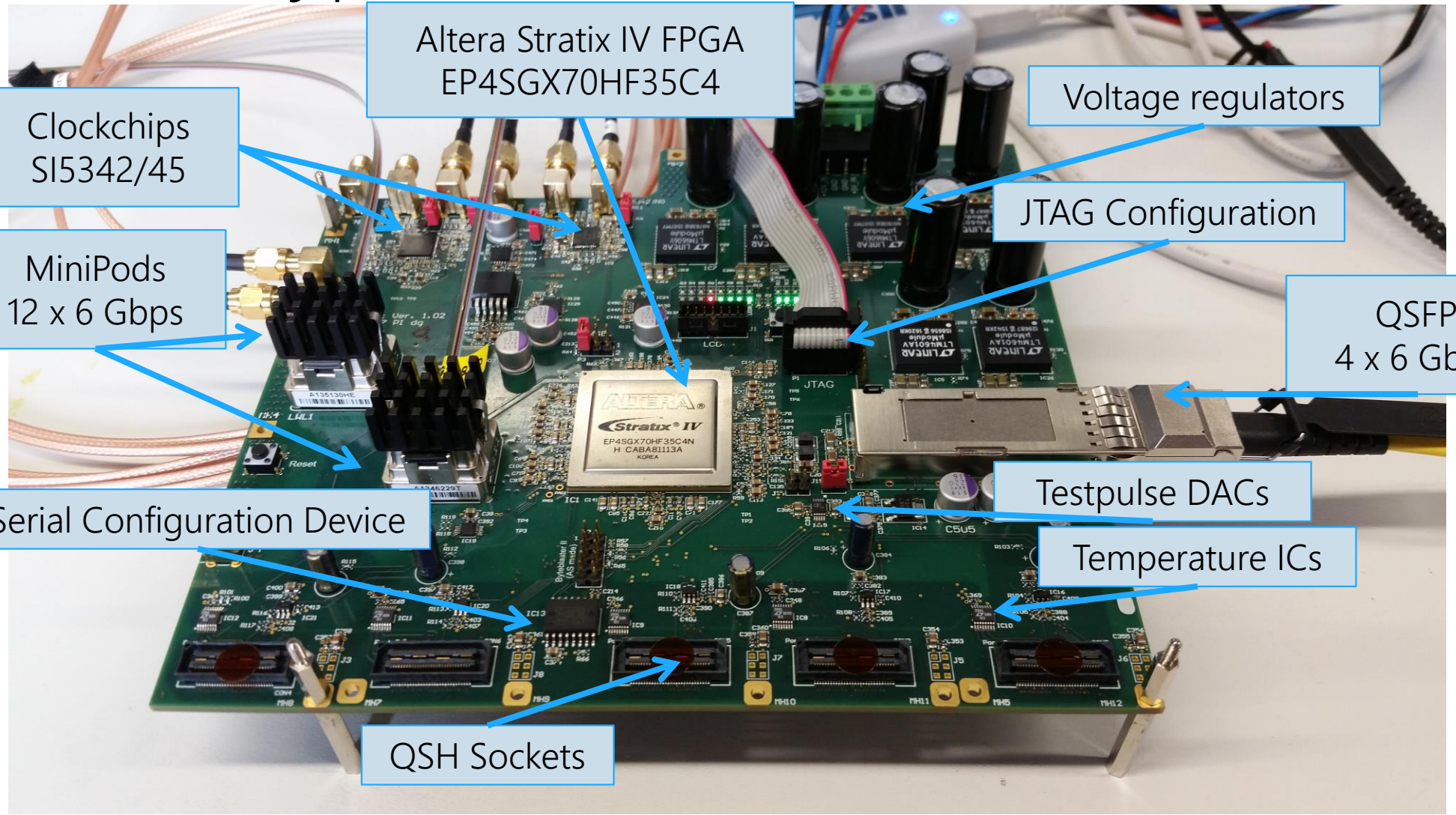


Summary on Stratix IV prototypes

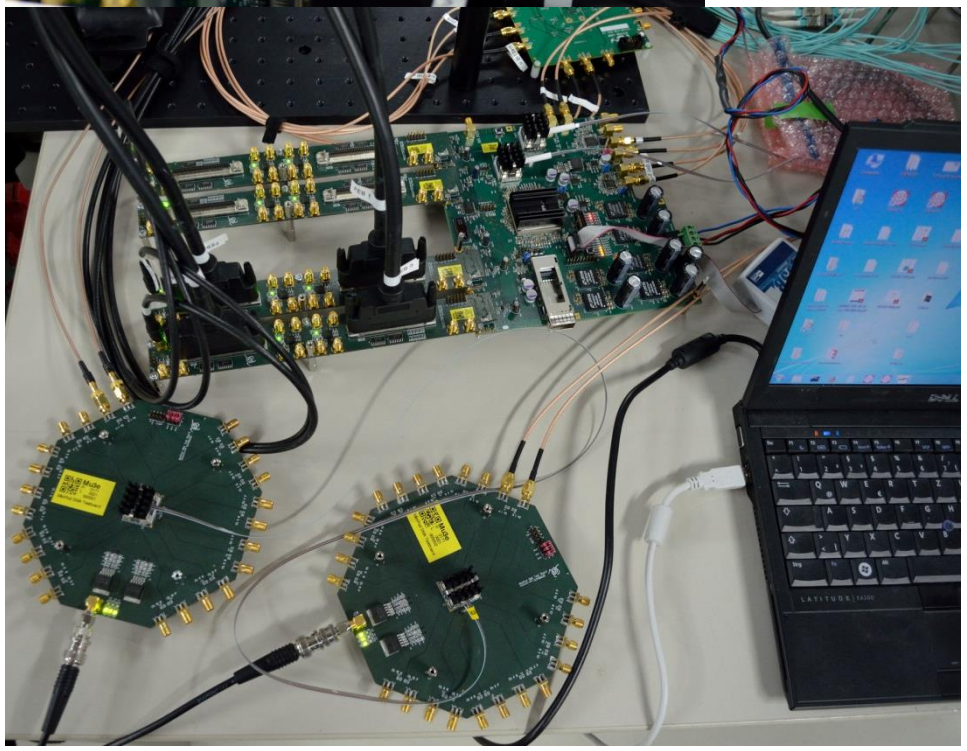
- 1 board of version 1.00 extensively characterized (internal note 0032)

- 6 boards of version 1.02 are fully operational
- 1 board of version 1.02 has issue with flash programming device, but is operational otherwise

- Can be used for vertical slice tests

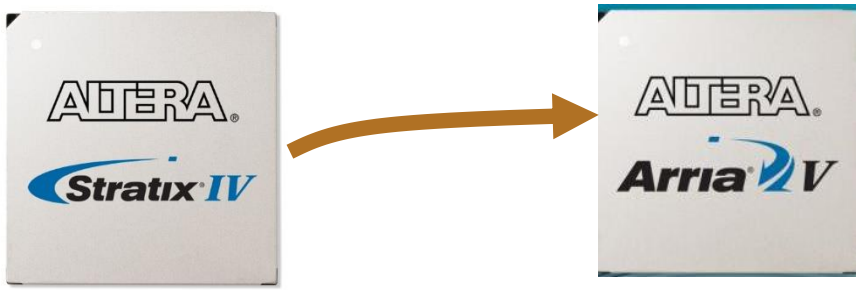
Front end board telescope

- MuPix8 telescope
  - 8 MuPix8 planes
- Read out via Front end board V1.02
- Testbeams:
  - DESY March 2018
  - MAMI March 2018
  - DESY June – July 2018
- Improved data for MuPix8@1.9V VDD
  - ➢ See:"*Update from the vertical slice commissioning*", Sebastian Dittmeier at the April Mu3e collaboration meeting



The next prototype: Arria V

- FPGA: 5AGXBA7D4F31C5N
- Development partially summarized (internal note 0035)



	EP4SGX70HF35C4N-ND	5AGXBA7D4F31C5N-ND
ALMs	29,040	91,680
Memory [kb]	8244	15,108
Tx/Rx (used)	16 (16)	9 (8/4)
LVDS Rx	56	80

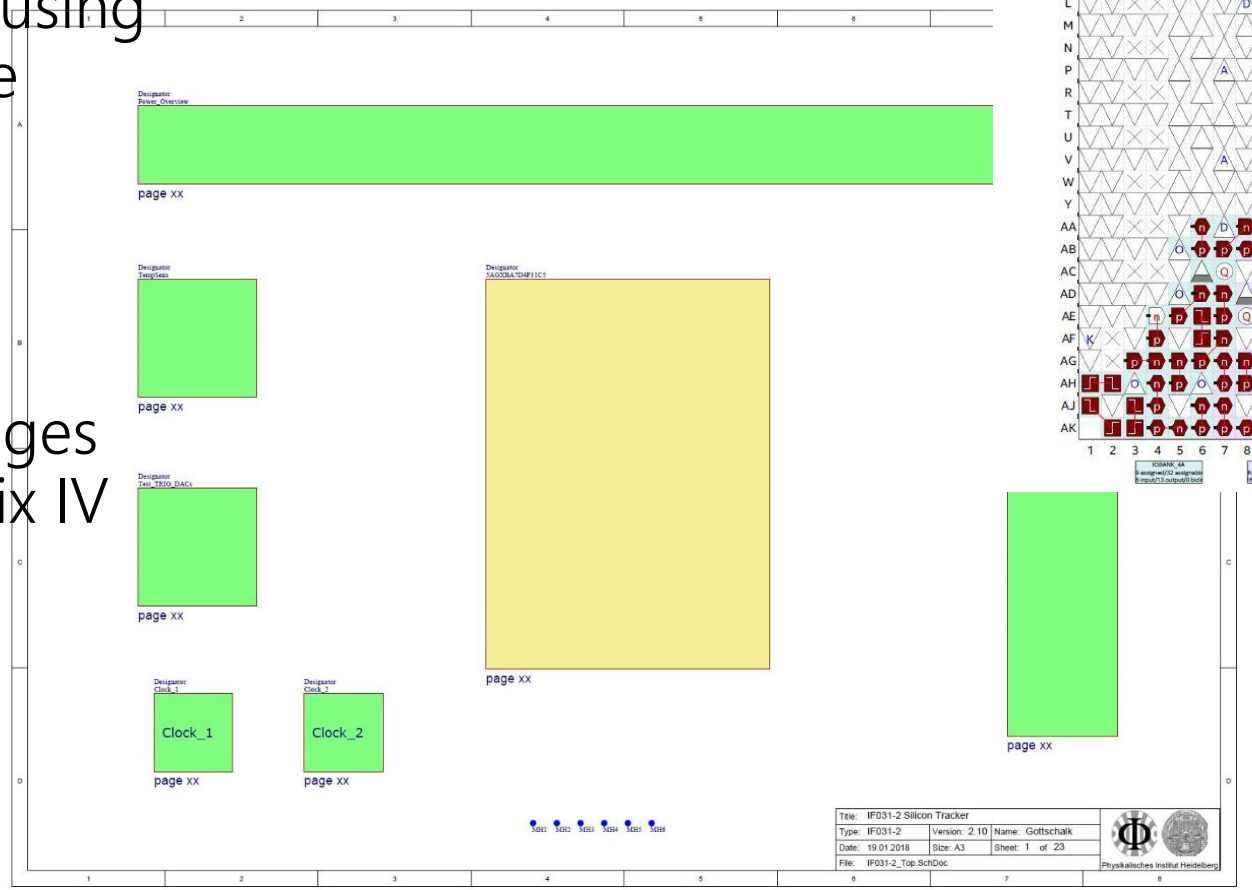
- Smaller feature size (28 nm compared to 40 nm)

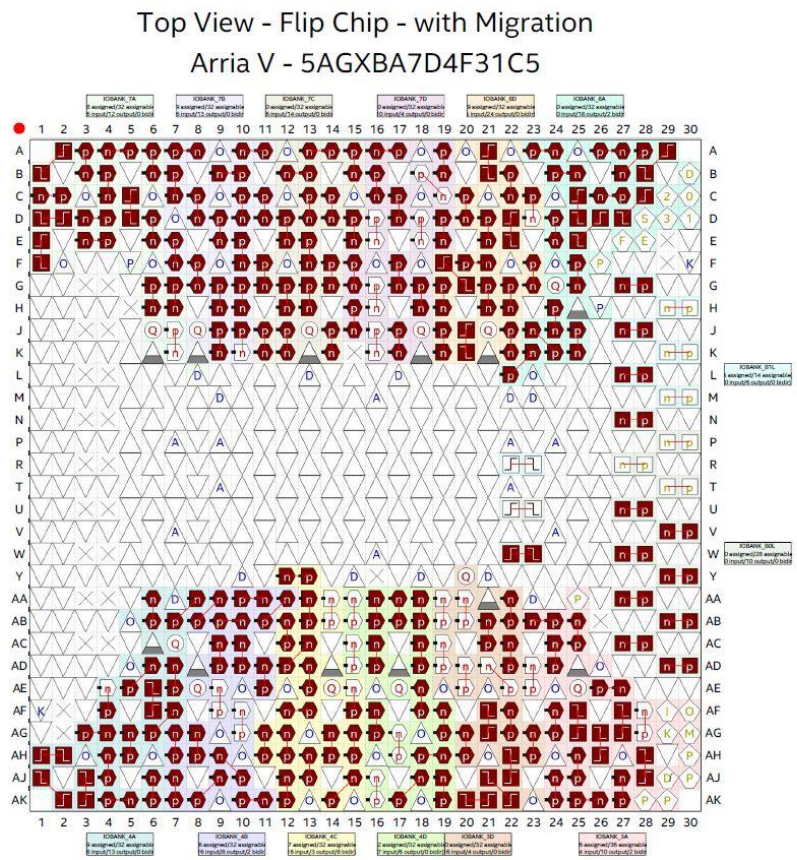
  → Reduced power consumption (3.3 W compared to 5.0 W, preliminary)

- Smaller package (31 mm compared to 35 mm)

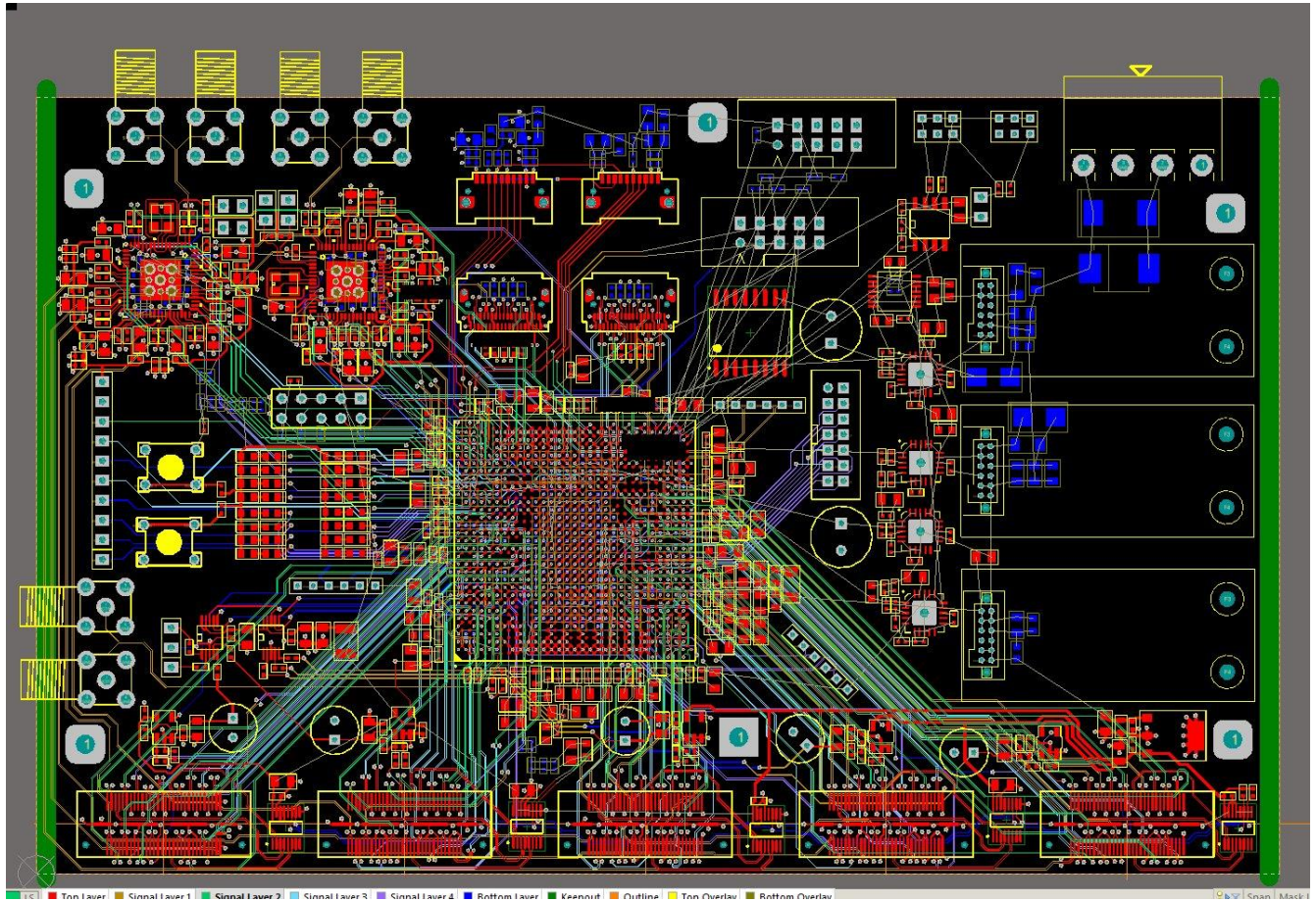
Preliminary schematic

- Pin-out was done using Quartus II software
- Schematic can be found here
- Layout started
- Will focus on changes compared to Stratix IV version



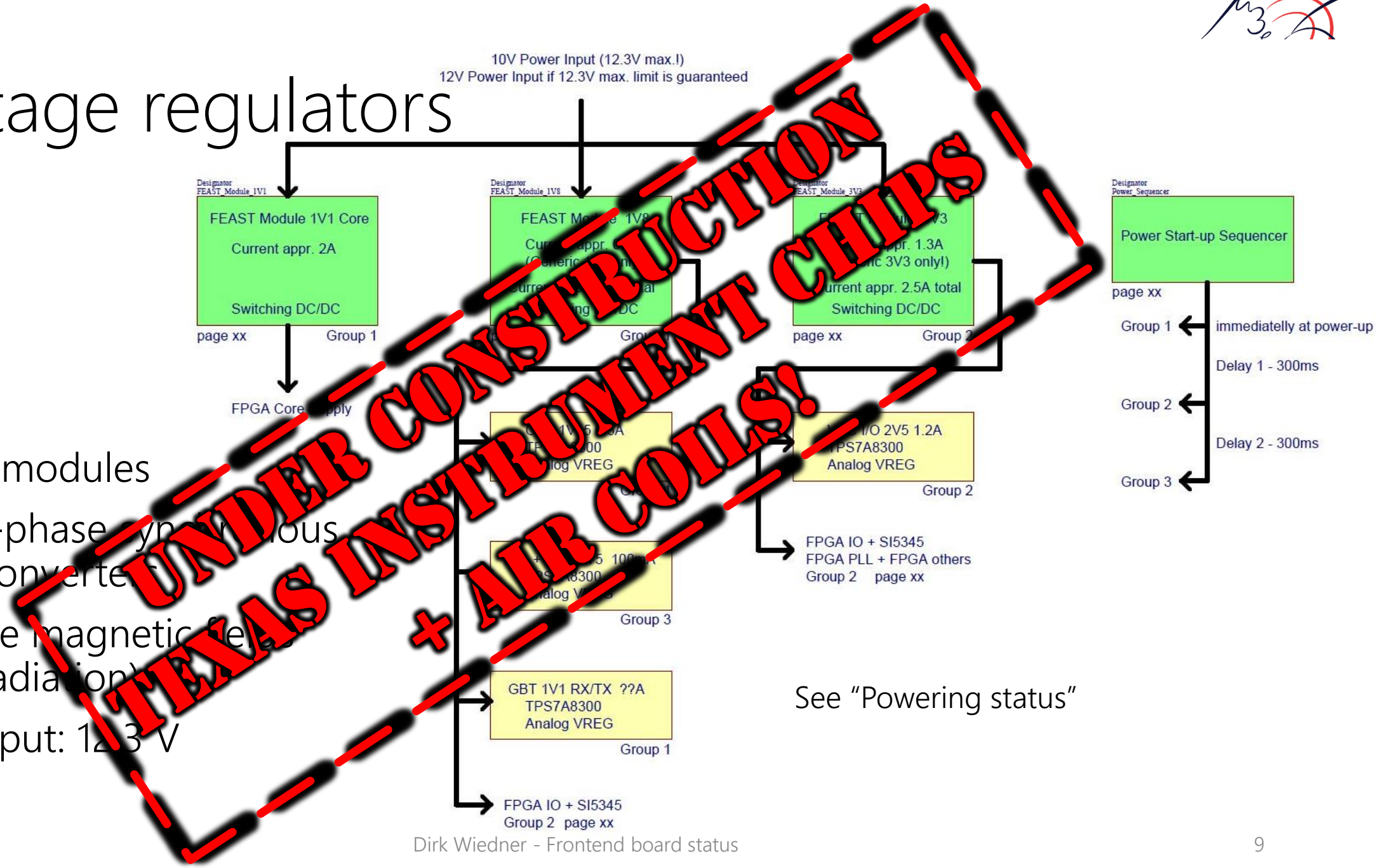


Layout FEB ARRIA version



Voltage regulators

- FEAST modules
- Single-phase synchronous buck converters
- Tolerate magnetic fields (also radiation)
- Max input: 12.3 V

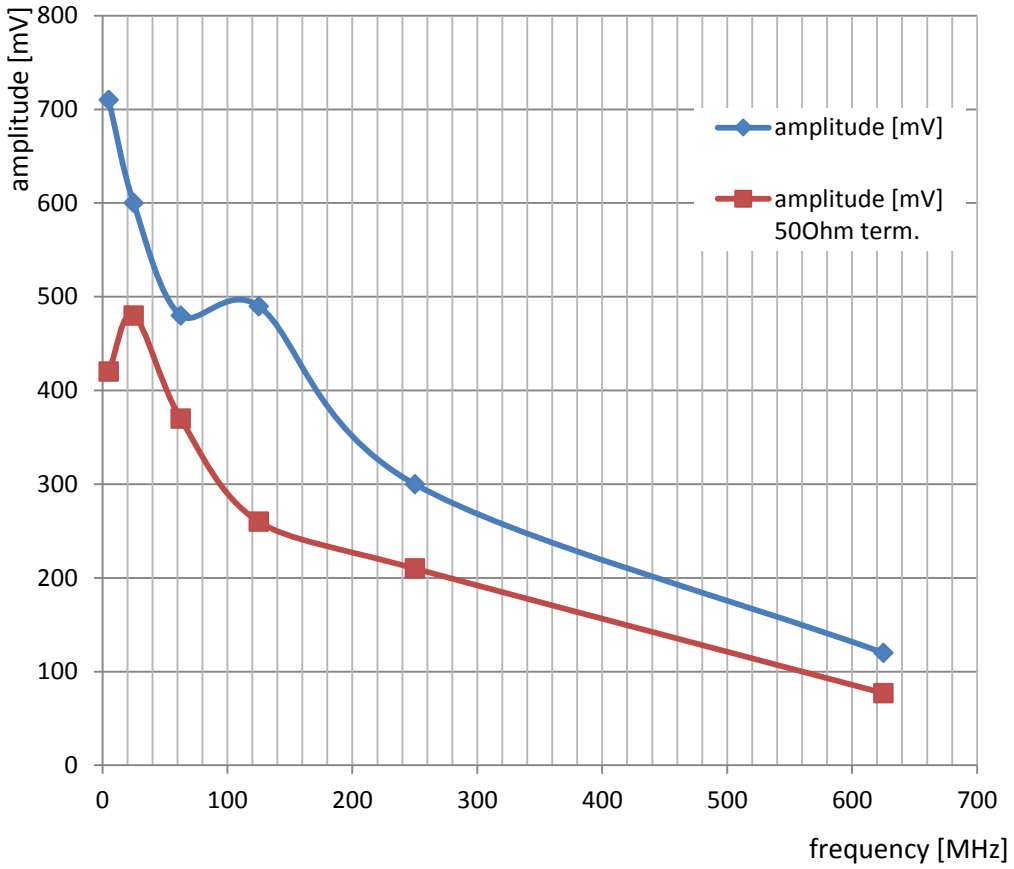


See “Powering status”

High speed electrical data links

- Received samples from PSI
- Small form factor twisted pair
- 68-82 Ohm differential measured with reflectometer
- 3m tested with
  - Si5338-EVB
  - 5 to 700MHz
  - LVDS
  - 50 Ohm high speed coax cables
  - 37.5 Ohm termination

➢Ok up to 200 MHz



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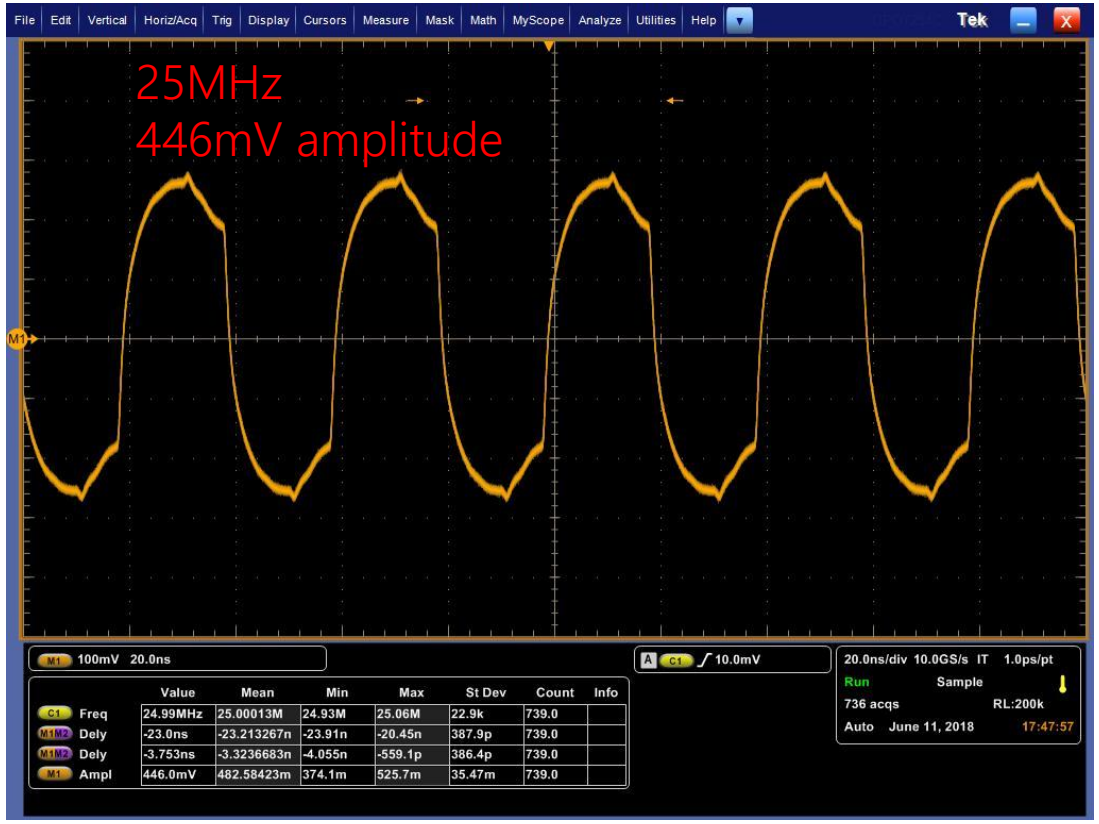

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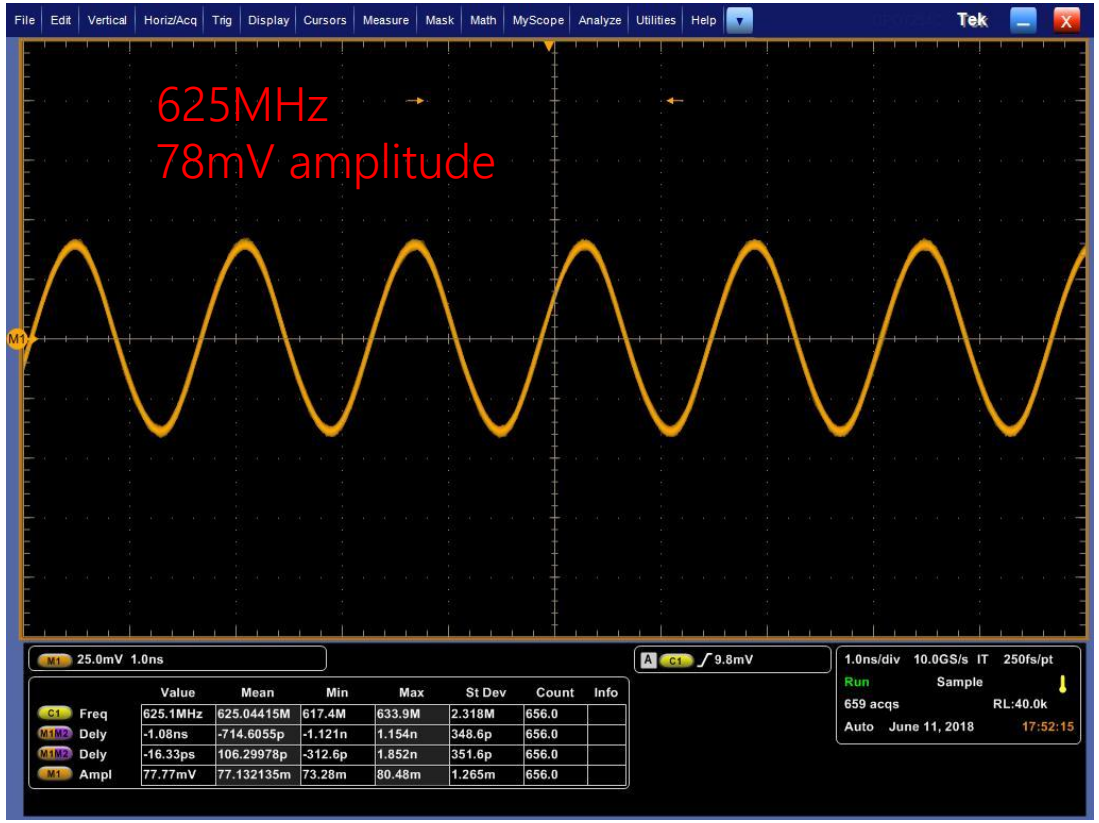


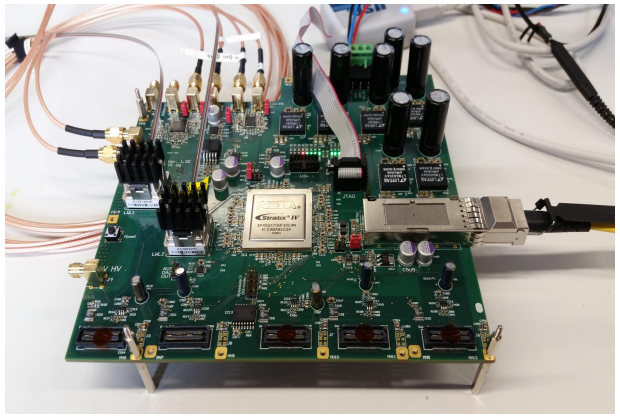
Crate controller interface

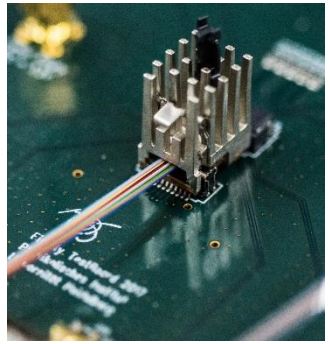
- Crate controller for FEB
- Monitoring of power and temperatures
- Crate controller powers off single FEBs
- JTAG
- MIDAS
- Power
- Connector type
  - Standard 1/20" 40 pin 3M connector
  - … as used for early MuPix PCBs etc.
- Layout progressing

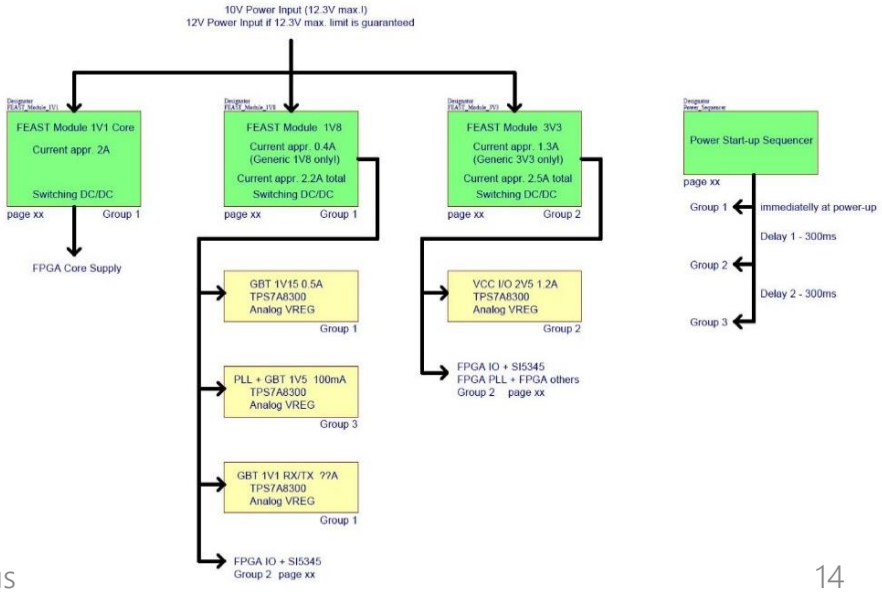
Summary and outlook

- 8 Stratix IV Front-end boards produced and operational

- Arria V board development on track
- Changes compared to V.1.02
  - Optical transceivers
  - Configuration device
  - Clocking
  - MSCB interface
  - Crate controller interface
  - Voltage regulators with aircoil
- Prototype estimated to be ready by the end of this year

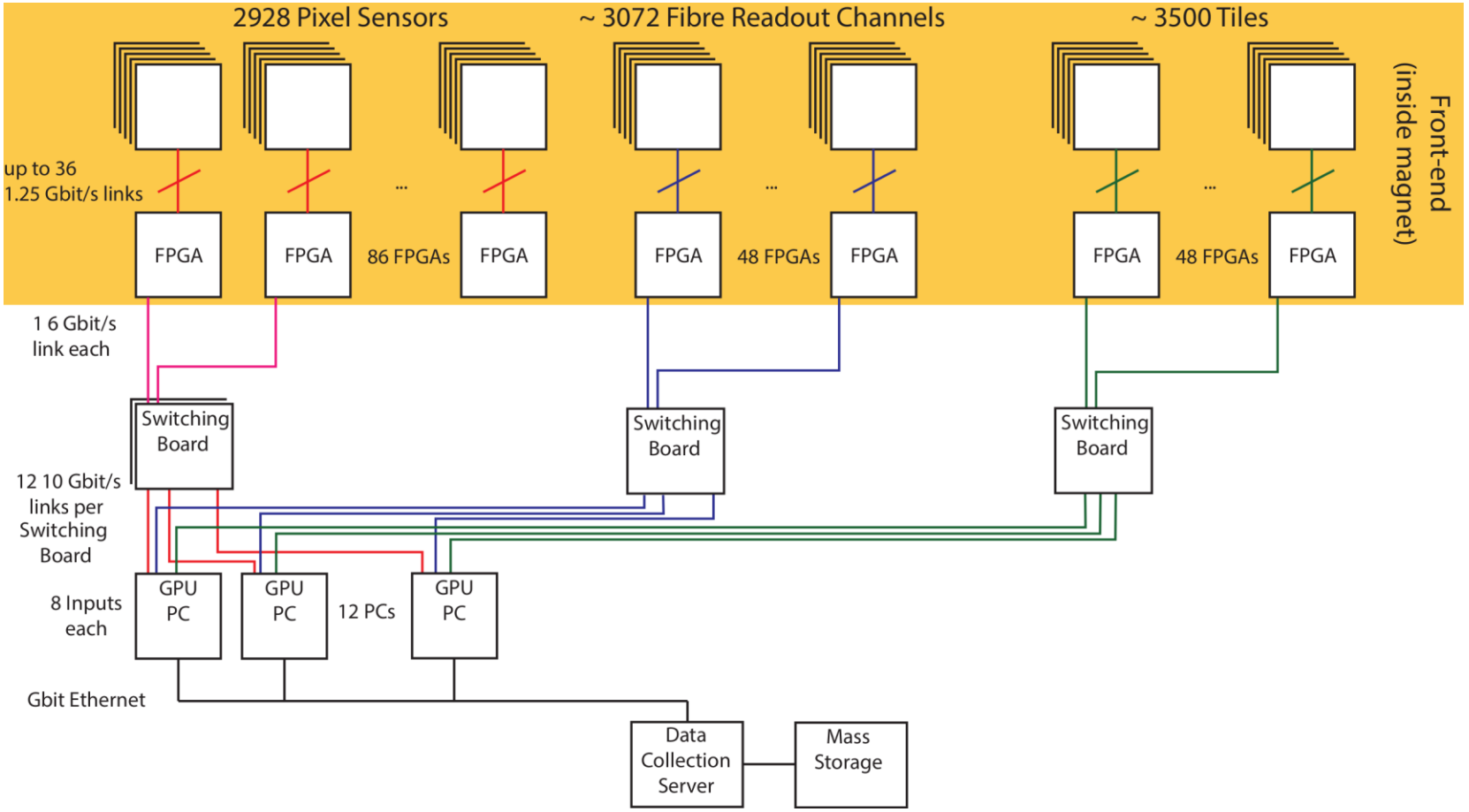






Backup slides

Mu3e Data Acquisition Concept

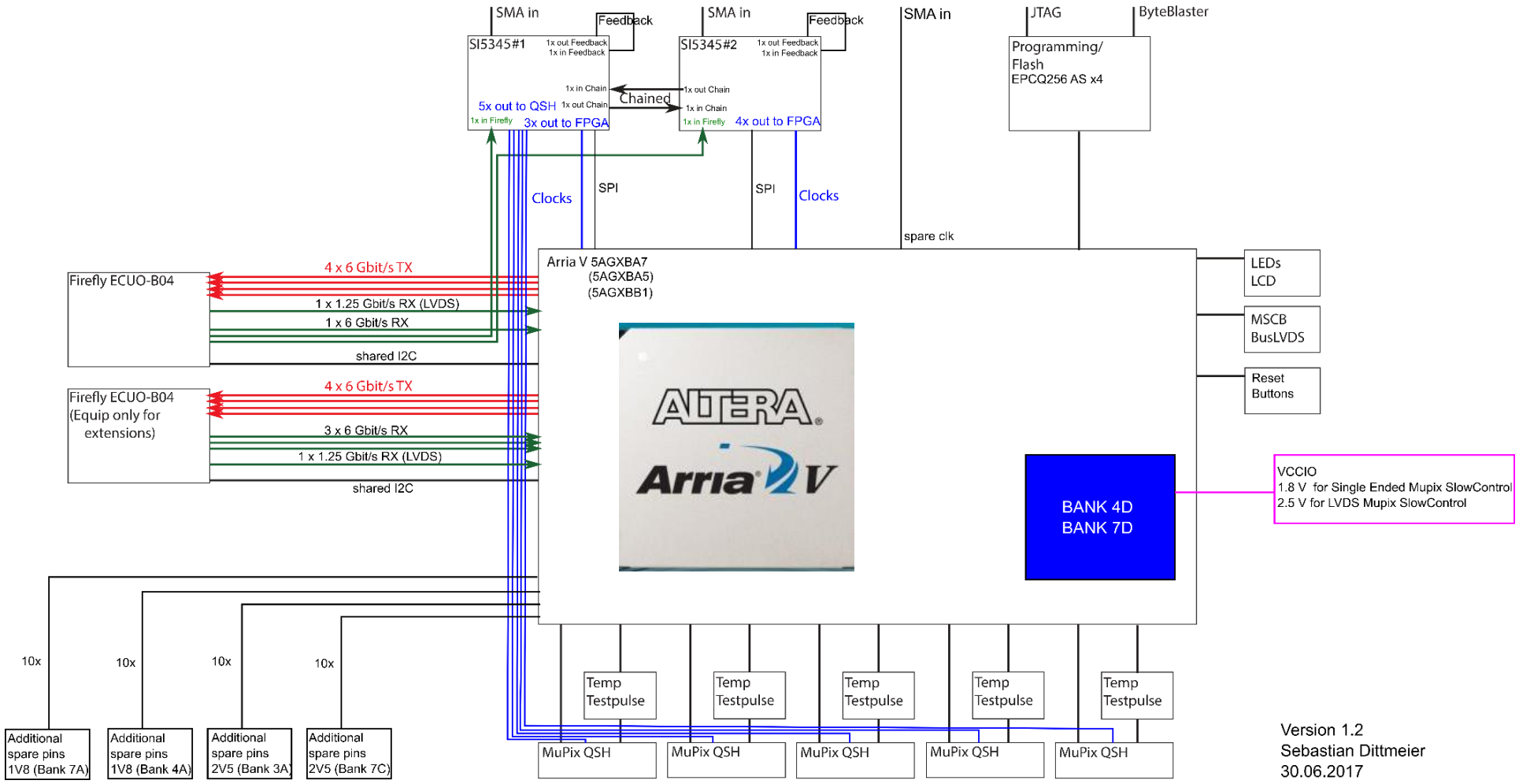


General issues with Stratix IV prototype

- The chosen Stratix IV FPGA has a quite low logic density
- One QSH-connector bank is missing deserializing inputs @ FPGA
- The chosen voltage converters do not tolerate magnetic fields

➢ Major redesign required
➢ Choice of different FPGA (Arria V) that fits our needs better and is cheaper
➢ Choice of different optical transceivers: Samtec Firefly

The next prototype: Arria V



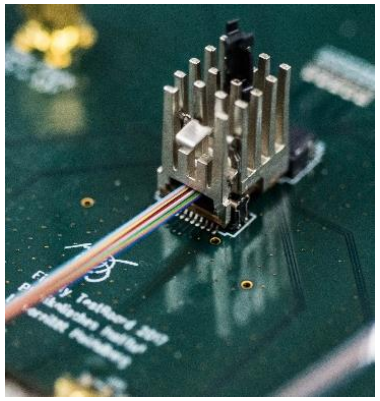
Configuration device and clock chips

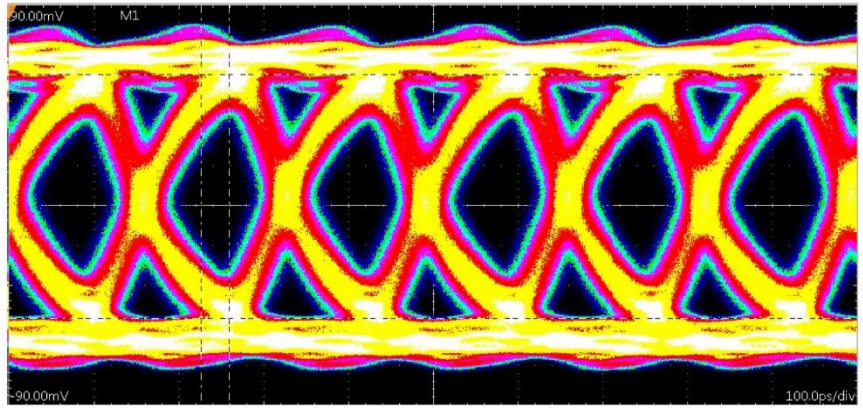
- Stratix IV version: EPCS128
- Arria V: Larger configuration device EPCQ256
- Allows to store at least two hardware images

- Stratix IV version: 1 × SI5342, 1 × SI5345
- Arria V version: 2× SI5345
- Allows to add individual clocks for QSH connectors

Optical transceivers

- 8 × optical links using 2 Samtec Firefly Duplex ×4 transceivers
- Transmitters: 8 × Multi-Gigabit transmitters of FPGA (6.25 Gbps)
- Receivers: 2 × Clock signals to SI5345 clock chips
  2 × LVDS receivers @ 1.25 Gbps as reset line
  4 x Multi-Gigabit receivers of FPGA (6.25 Gbps)

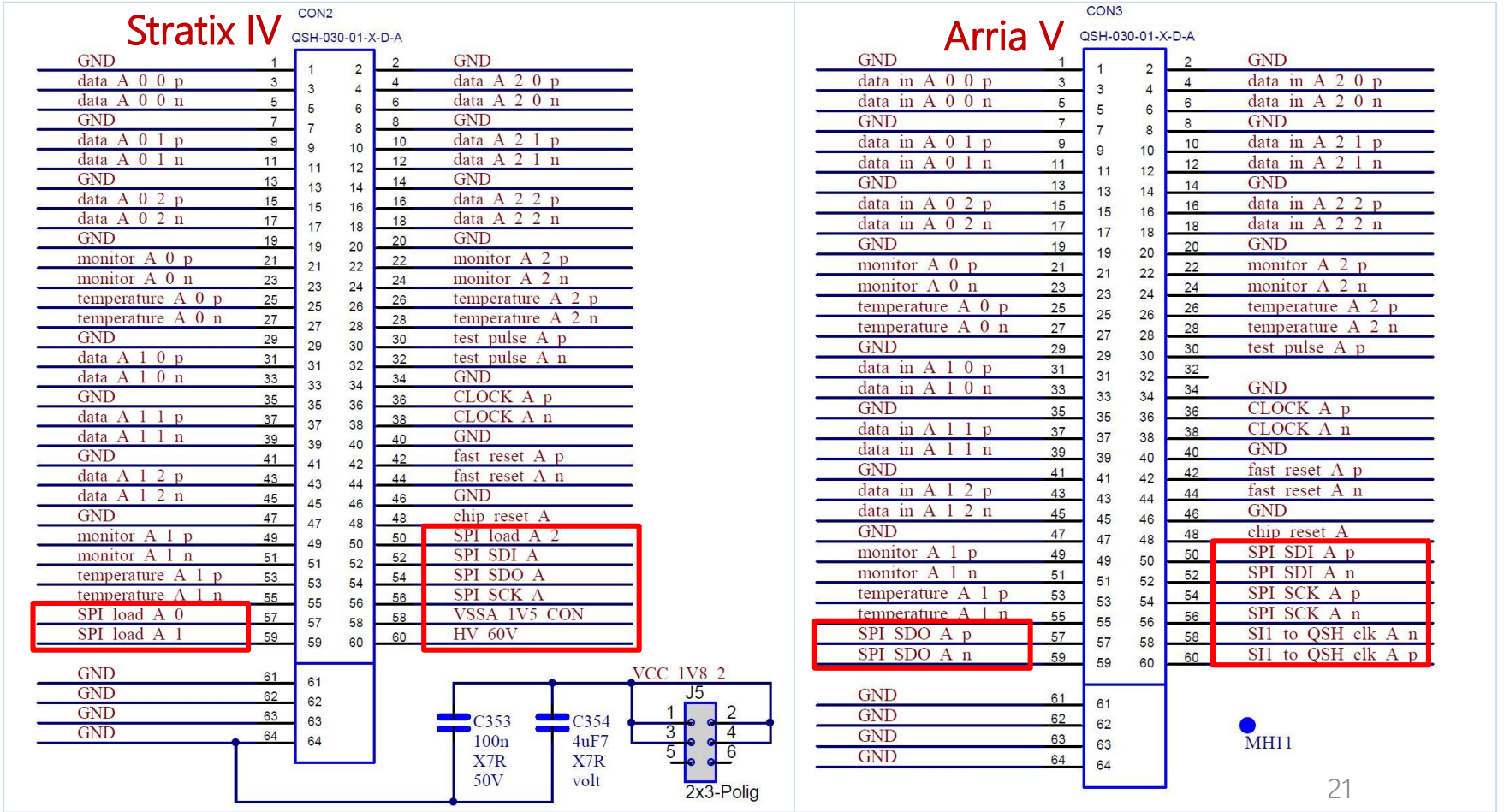




6 Gbps PRBS7 data after optical transmission using Samtec Firefly

QSH connector

- QSH-connector is to large extent compatible with board v.1.02
- Removed Power
- Removed HV
- Added clock from SI5345
- Slow control lines are routed differentially



MSCB interface

- On the Stratix IV board:
  2 pins connected to FPGA differential buffer
- Arria V board:
  External differential buffer ADN4691
- Connects to 2 × RJ10 connectors
- Allows MSCB daisy-chain for FEBs
- Jumper to connect power supply