

PAUL SCHERRER INSTITUT



WIR SCHAFFEN WISSEN – HEUTE FÜR MORGEN

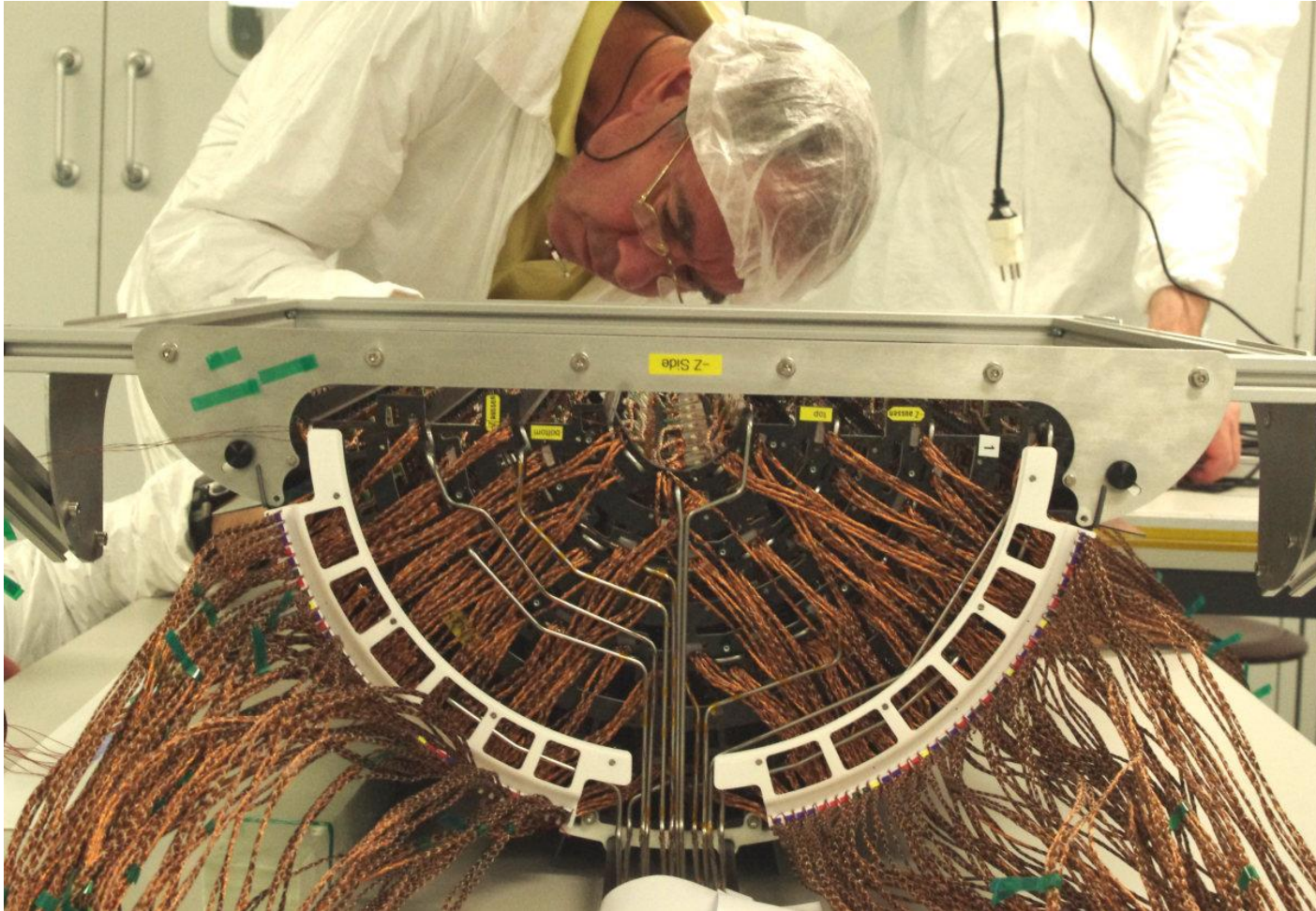
Beat Meier :: Chip Design Team :: Paul Scherrer Institut

# Readout Cables Inside Detector Mu3e Integration Meeting

19/20. May 2018



Can we use the same type of cable for the Mu3e pixel detector?



CMS BPIX assembly with cables and cooling tubes ( $\frac{1}{4}$  detector)



# BPIX vs. Mu3e Pixel Cabling



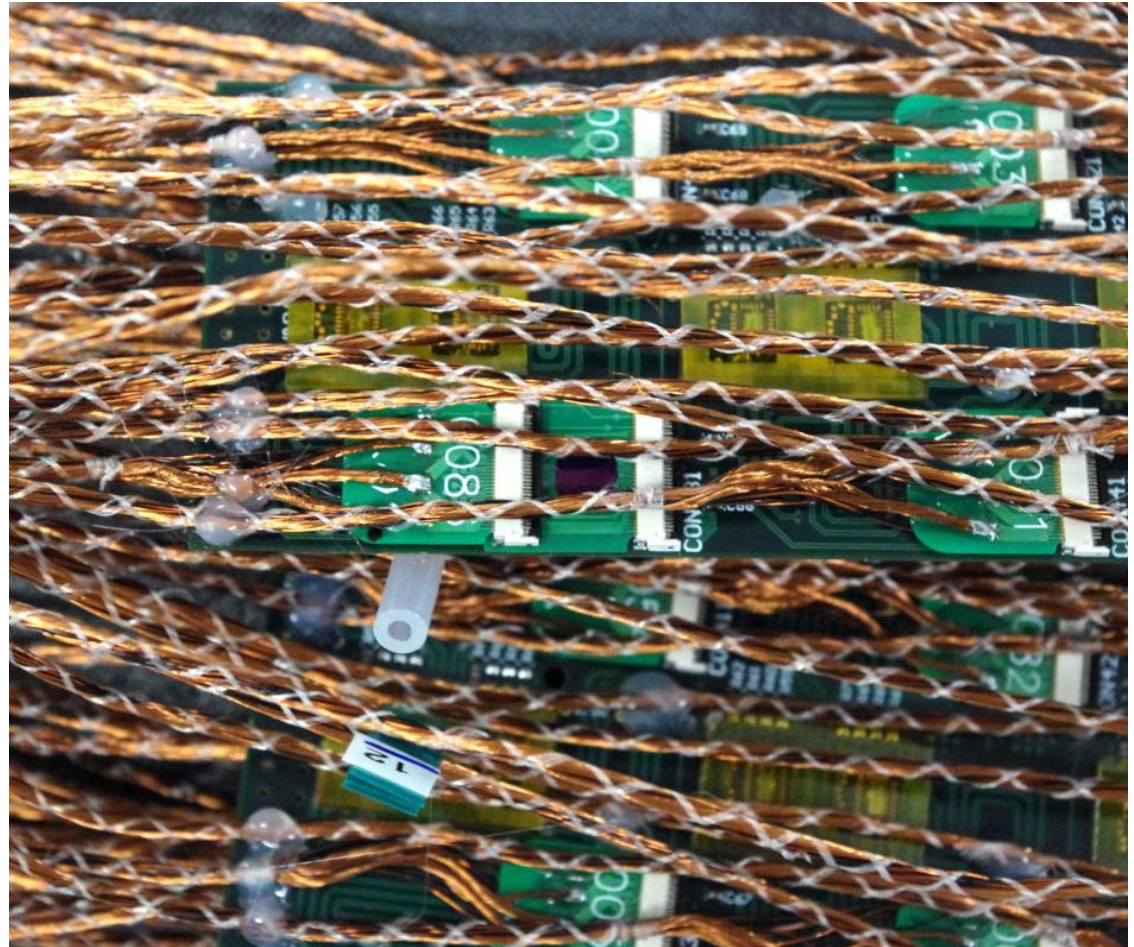
Similar requirements

- low mass
- limited space
- cable length 1m
- high speed data transfer

BPIX: **400 Mbit/s**  
without pre-emphasis

Mu3e: **1.25 Gbit/s**  
with pre-emphasis

Speed is the critical point

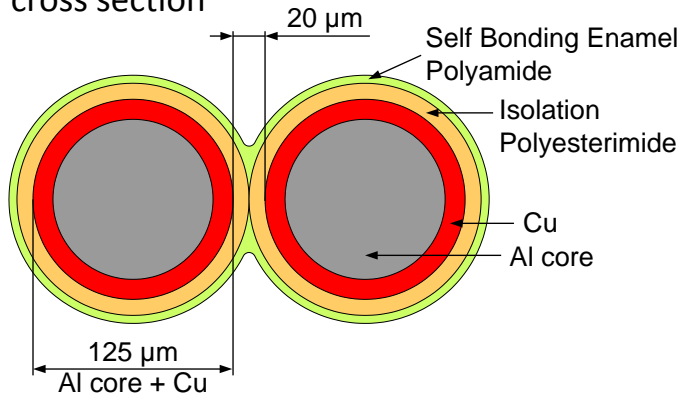


Module cabling on the BPIX connector board



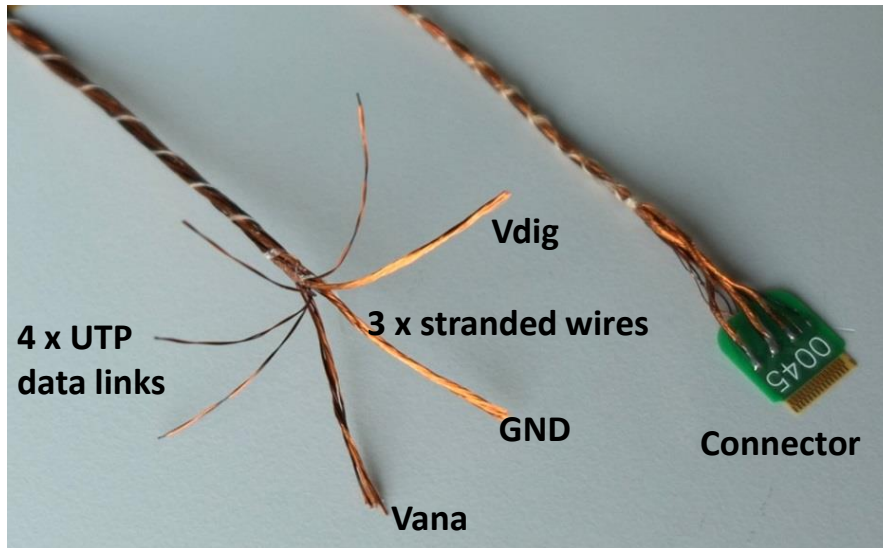
## Unshielded Twisted Pair UTP

cross section



- Self bonding wire (Elektrisola)
- 125  $\mu\text{m}$  wire diameter Cu tests with Cu layer on Al core  $\rightarrow$  difficult to handle
- twisted: 10 mm per turn
- unshielded
- diff. impedance: 60 Ohms

## Module Cable

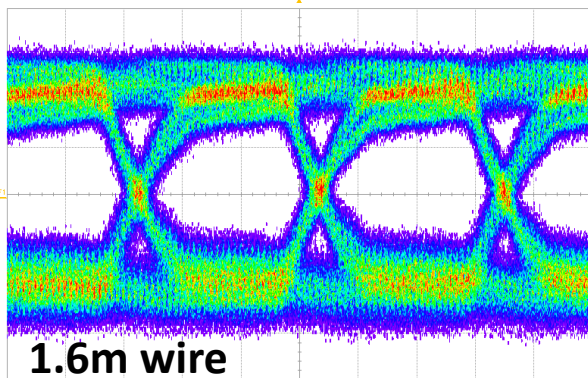
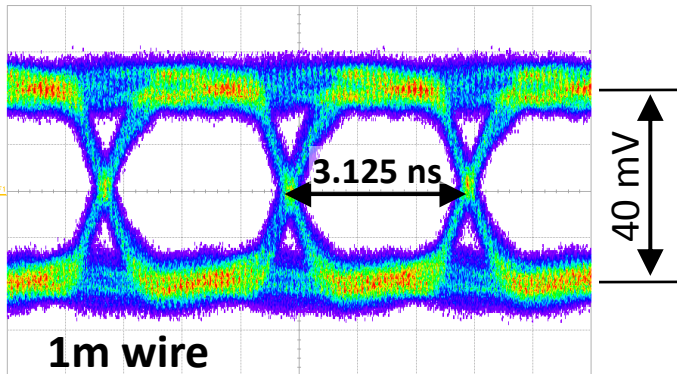
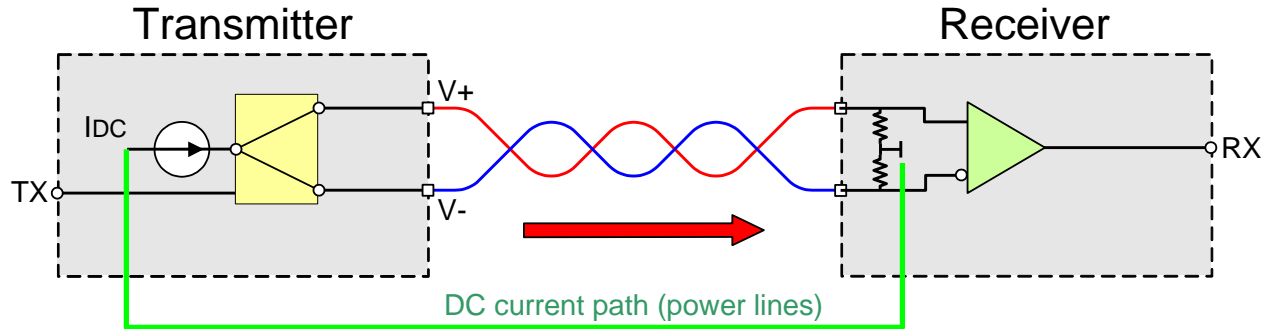


### pros

- very flexible in all directions
- minimal material / diameter

### cons

- high loss;  $R_{DC} = 2.3 \text{ Ohm/m}$   
Skin depth = 8.5  $\mu\text{m}$  @ 100 MHz
- difficult assembly (connectors)



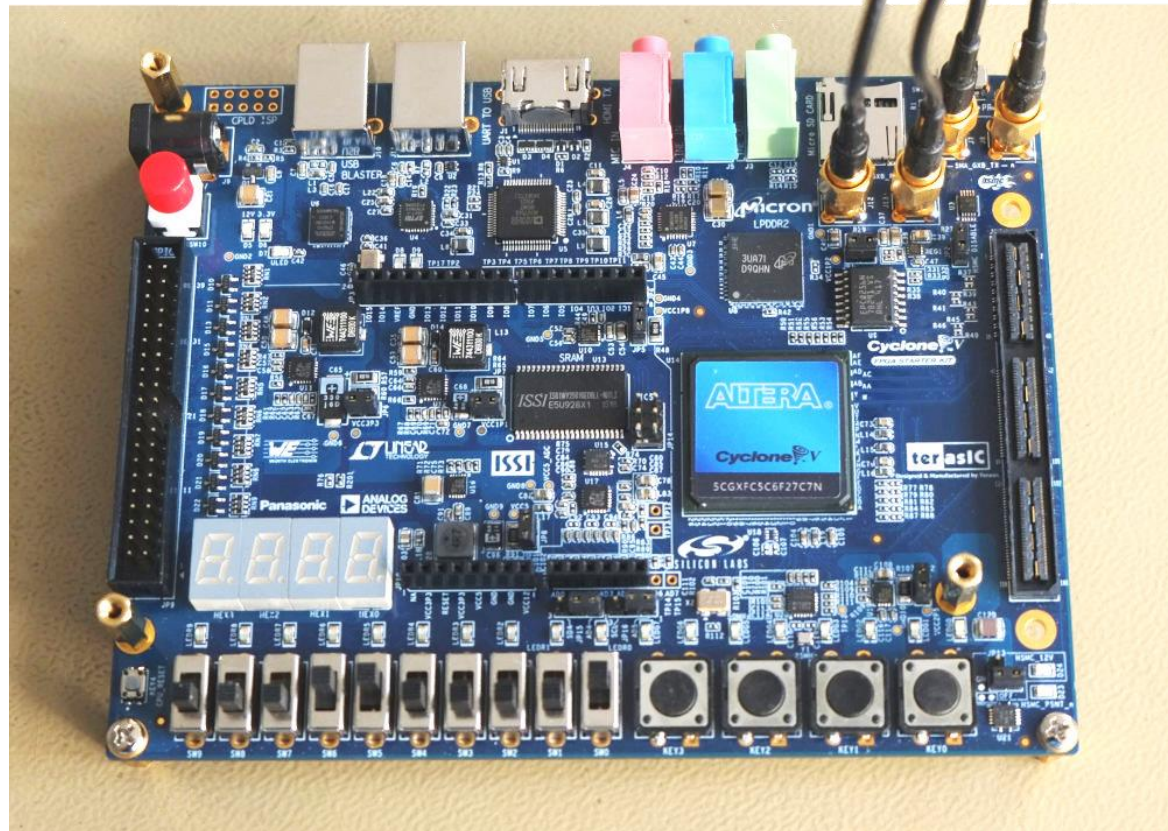
- Custom driver and receiver LCDS (500 Mrad)
- 320 Mbit/s
- Minimal amplitude: 20 mVpp
- +/- 500 mV DC offset between driver and receiver
- Bit error rate <  $10e-12$  (different condition)
- Crosstalk: -27 dB
- Power consumption / link: 4mW (12 pJ/bit)



# First Test Setup for 1.25 Gbit/s



- Cyclone V GX starter kit
- FPGA TX → UTP → FPGA RX
- speed up to 1.25 Gbit/s





- MuPix8 Chip, boards and cables from Heidelberg
- Arria V FPGA development Kit (PCIe Card)
- MuPix8 → UTP → FPGA RX

