Mu3e SciTiles

Konrad Briggl, with Yonathan and Hannah (KIP)

Mu3e Integration workshop

19&20th of June 2018

Geneve

Tile detector parts and nomenclature

Assembly

PCBs and requirements

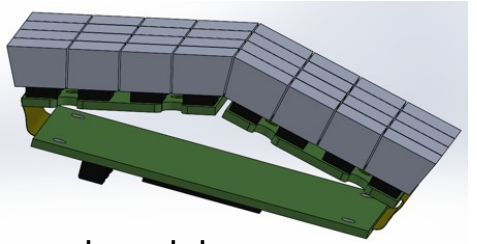
Space, etc.

Tile detector overview

Submodule

- Tiles (Ej-228, 6.5x6.5x5mm³), wrapped in ESR foil, glued to SiPMs (3x3mm²),
- 32 channels
- Front-end board: Flex-rigid PCB (6 Layer / 2 Flex)

  Hosts readout ASIC (MuTRiG, currently StiC3.1), tiles & SiPMs

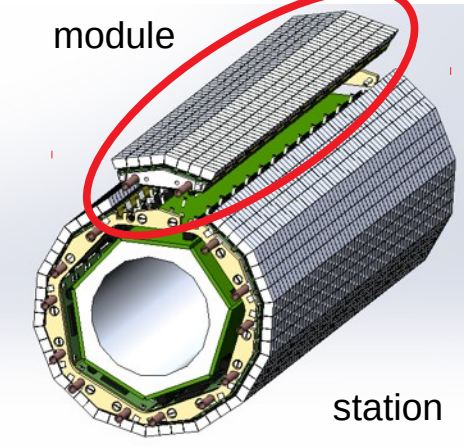


submodule

Module

- 14 submodules mounted on cooling structure (water cooling)
- Connection to FE-FPGAs: MALIBU board

  (clock distribution, power, system monitoring)



station

Station

- 7 modules mounted on end rings
- Total length 368mm
- 2 Stations in phase I

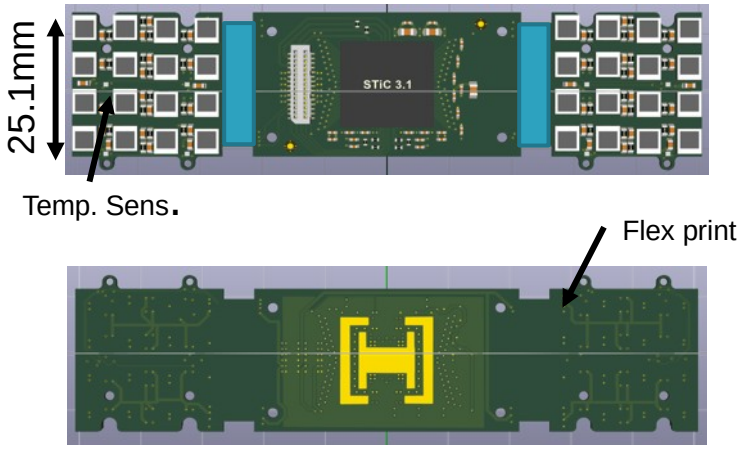
Tile detector – Front-end board

Currently designed for STiC readout ASIC, MuTRiG in next iteration

32 SiPMs,

8 digital temperature sensors,

1 readout ASIC in BGA



Test procedure during/after assembly

Test ASIC in testsocket before assembly

Test board with populated ASIC (charge injection)

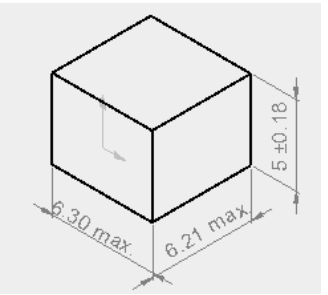
Test board after populating Sensors (DCR, noise, jitter with laser,…)

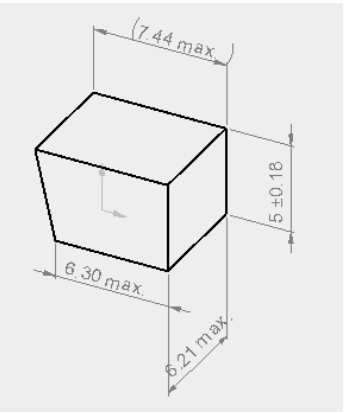
Final test with cosmics and in testbeam

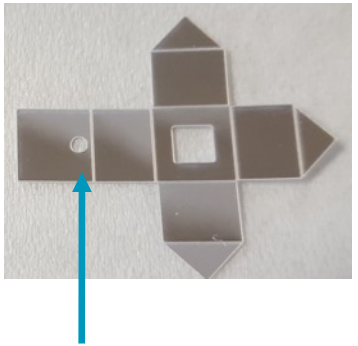
Tile production

- Scintillator material Ej-228 (equivalent to BC-418)
- KIP workshop produced 180 tiles
- Foil design to maximize reflection (Laser-cut ESR 3M foil)

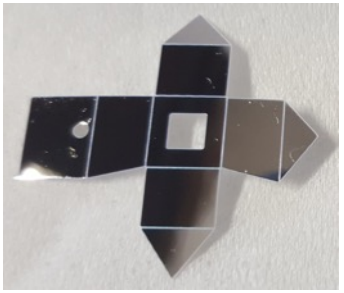
- Tile dimensions checked before wrapping

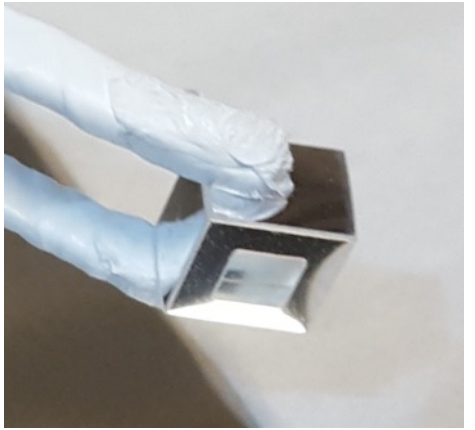




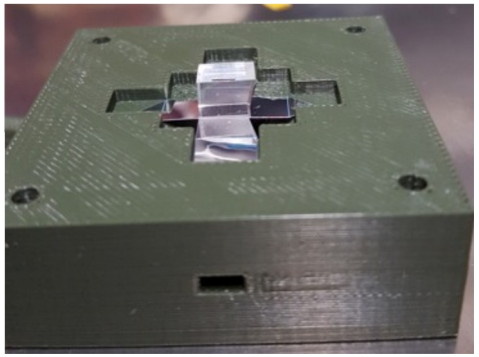
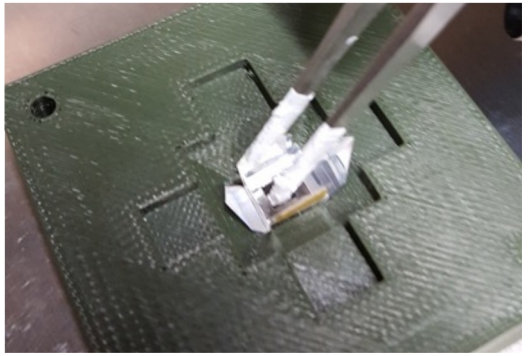


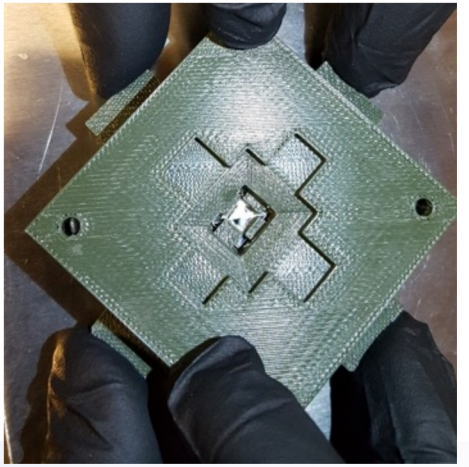
Hole for monitoring the glue quality

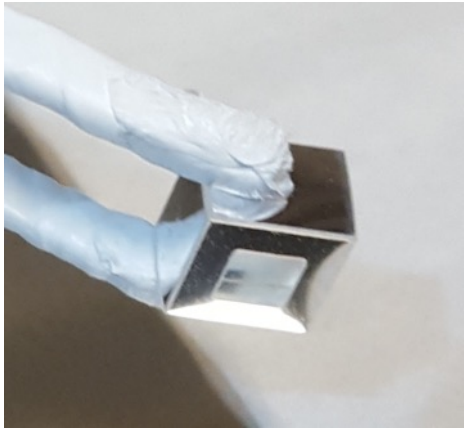




Tile wrapping

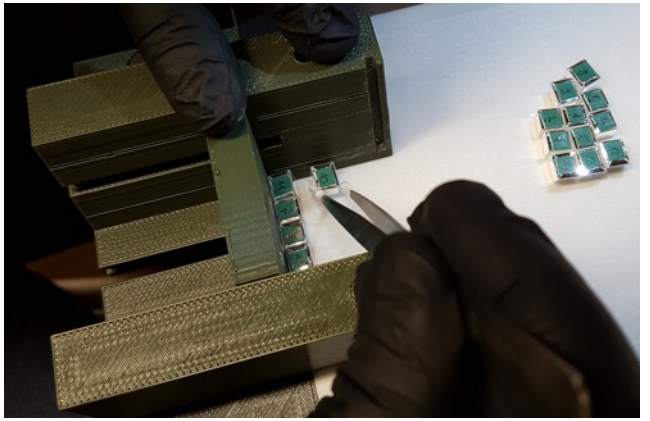



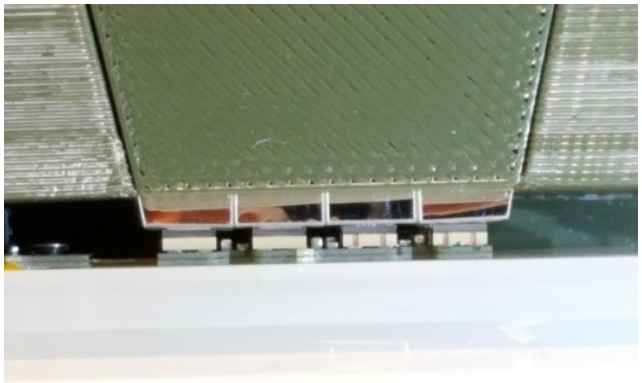




Submodule assembly

- Tile wrapping
- Glue 16 channels (half matrix) at the same time (reduce tolerance issues)
- Dispense glue
- Monitor for bubbles after 24h of curing
- Reached stable (good) glue quality results in this procedure & tools
- Some issues with placement tolerances & Tile dimensions identified
  → Expect better alignment with more rigid gluing tools
- Tile dimensions after wrapping close to the tolerance limit
  (foil thickness larger than specified in datasheet)
- Half matrix too large after gluing
  → Need to increase tolerances (decrease scintillator size) to compensate

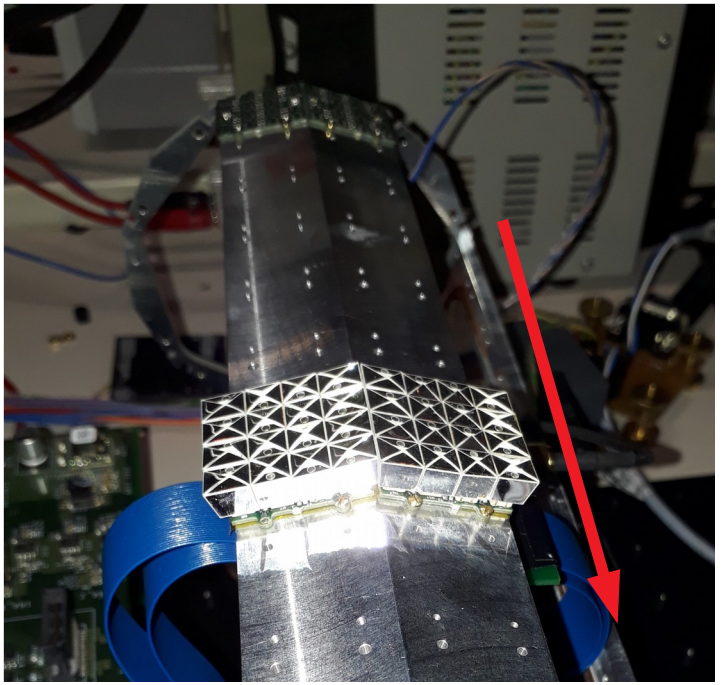




Module assembly

- Assemble submodules on cooling/support structure
- ASIC side: fixed by screws
- SiPM side: alignment pins + Screws only on one edge
  (accessibility with tiles placed…)

- Predefined assembly direction
- Not ideal for possible replacement of submodules,
  screws easily interfering with tiles, …
- Different solutions under consideration,
  basic point is to mount SiPM part from ASIC side
  - Requires split support plate or cutout for screws in FEB

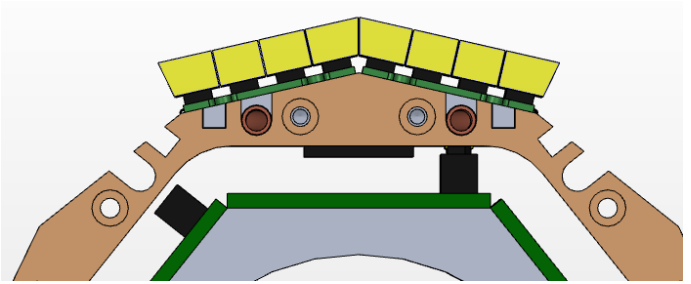


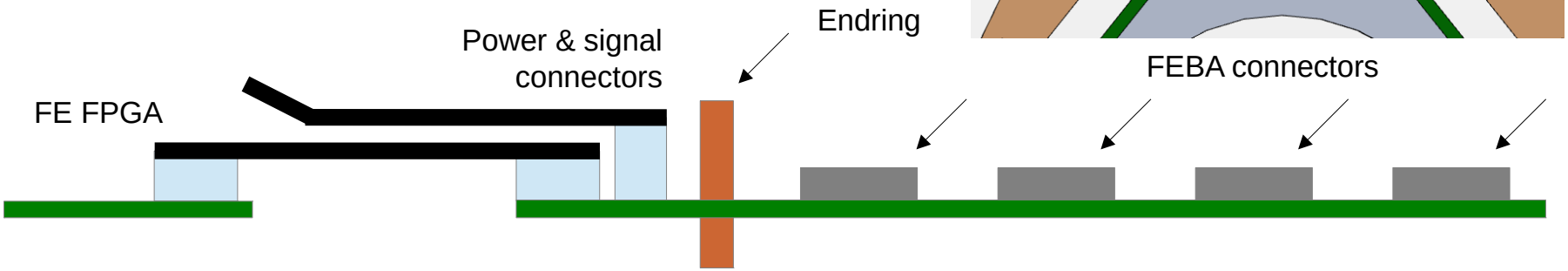
Assembly direction on module

Module interconnection board (MALIBU)

- Interconnection for one module (14 ASICs) to front-end FPGA
- Routing of data, slow control & clock
- Power distribution
  - 2 LDOs for each ASIC,2 for auxilliary chips
- Clock distribution
  - Separate clock trees for digital part & PLL (should be combined)
  - Buffer tree for PLL test injection signal

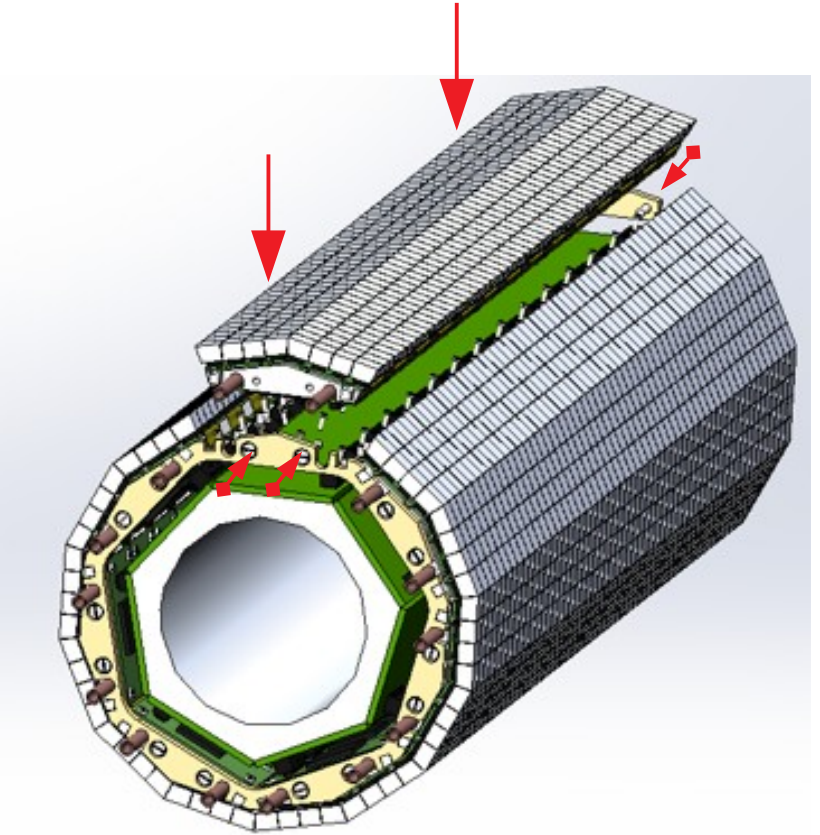
- Connectors for power (LV,HV) and to FPGA-board each behind end-ring sections
- 8 Layer board, approx 40x420x1.5mm size (+ components)





Station assembly

- Slide in submodules in r-direction
- Fix to endrings using screws along z
- No access to screws after mounting endring to beampipe
- Better to also have the screws in radial direction
- Minimum thickness of endring sections



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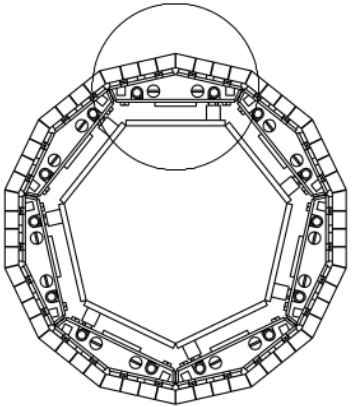

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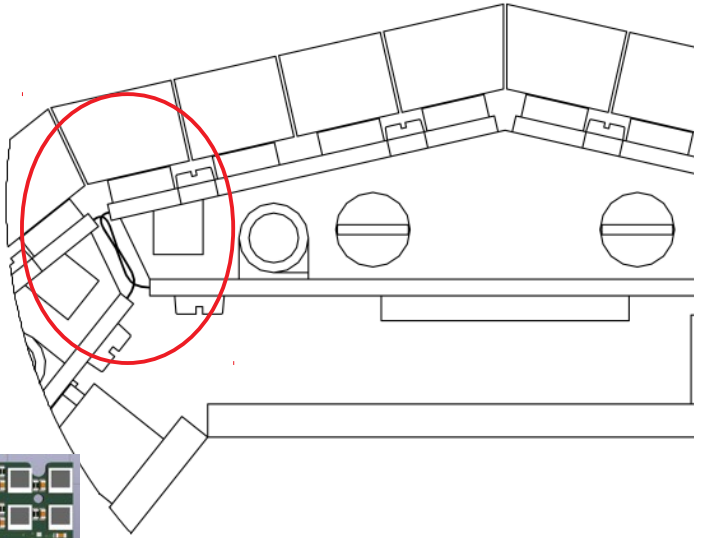
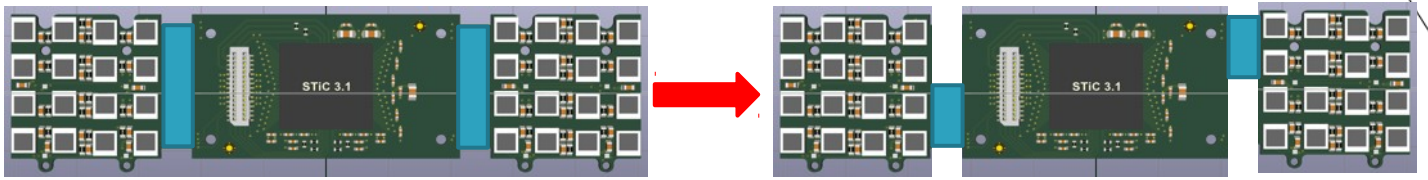


- Small gap between modules
  - Flexprints interfering
  - Next version of FEB will have staggered flex-part to avoid this



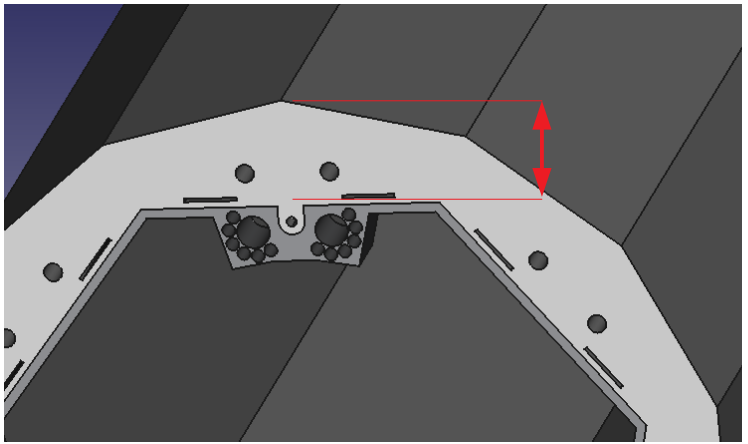
Electronics: Requirements

Connection single module (MALIBU) ↔ FE-FPGA , HV, LV

- Foreseen two data port connectors (Samtec QTH/QSH) on the FE-FPGA
  - Pin compatible with FE-FPGA, also requires space for 2 cables (More space on FPGA wheel?)
- Power using M3 cable mount connectors for current prototype
  - „5V“ supply – mainly clock driver chips
    - Locally regulated to 3.3V
    - 5A total per datasheet, seems to be overestimating
    - Heat generation of clock chips also needs to be considered!
    - Thermally connected to tile support or by helium flow?
  - „2.5V“ supply – ASICs
    - Locally regulated to 1.8V (digital+analog) – possibility to move LDOs to FEBs to be investigated
    - ~20A in STiC working configuration
    - ~9A for MuTRIG
- HV
  - Currently split in 4 domains
  - How many required depends on full thermal simulation including pixels, expected radiation damage (Local gradients)

Getting it together

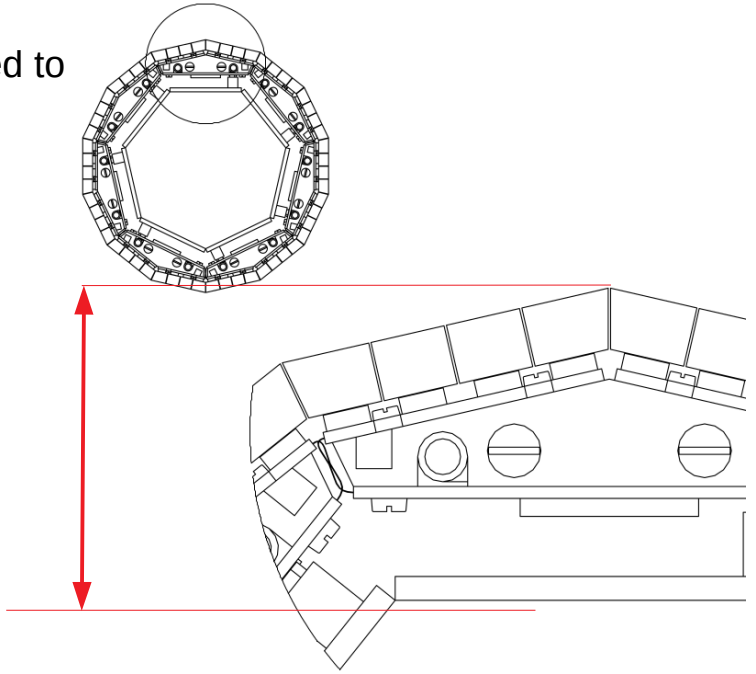
- Currently big discrepancy between TDR tile mechanics and design by Silvan
- Missing almost 10mm in radial direction
- Interferences in end-ring sections
  - Blocks interconnection board
  - Endring-mounts and surrounding cabling area should be rotated to corners, to make room for PCB in this area



~16.4mm

vs

~26.2mm



Getting it together

- Currently big discrepancy between tile group mechanics and design by Silvan
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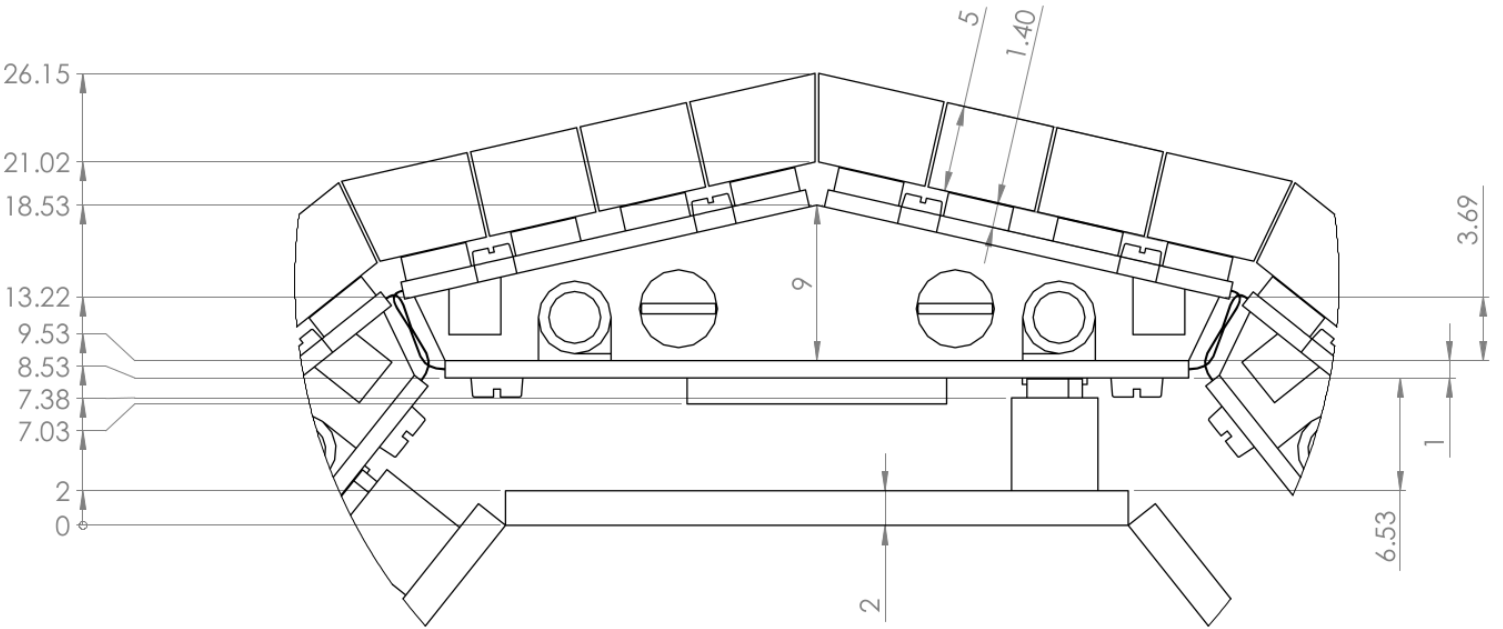
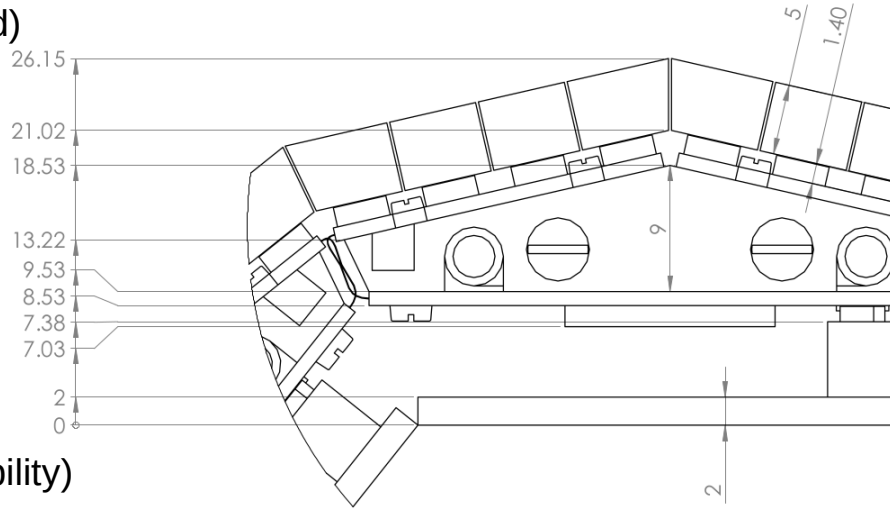
- Mechanics based on older detector design → Where to shrink ?



Getting it together

- Currently big discrepancy between tile group mechanics and design by Silvan
- Missing almost 10mm in radial direction
- Mechanics based on older detector design → Where to shrink ?
  - MALIBU PCB Currently 1.5mm thick,
    components top 1.7mm/bottom 1mm (connectors excluded)
    - May shrink up to 1mm using thin PCBs
  - MALIBU – FEB connector
    - Mating height 6mm, minimum 1.7mm
      (with ASIC on support side), reduce by 4.3mm
  - Support structure (9mm)
    - Mostly given by detector geometry,
      (also recurl electron stopping power, mechanical stability)
    - Minimum flex bending radius allow slimming by 1.7mm
  - FEB (1mm on each side)
    - Proper SiPM-Tile gluing requires flat surface on sensor side…



We are still missing 3mm...

Getting it together

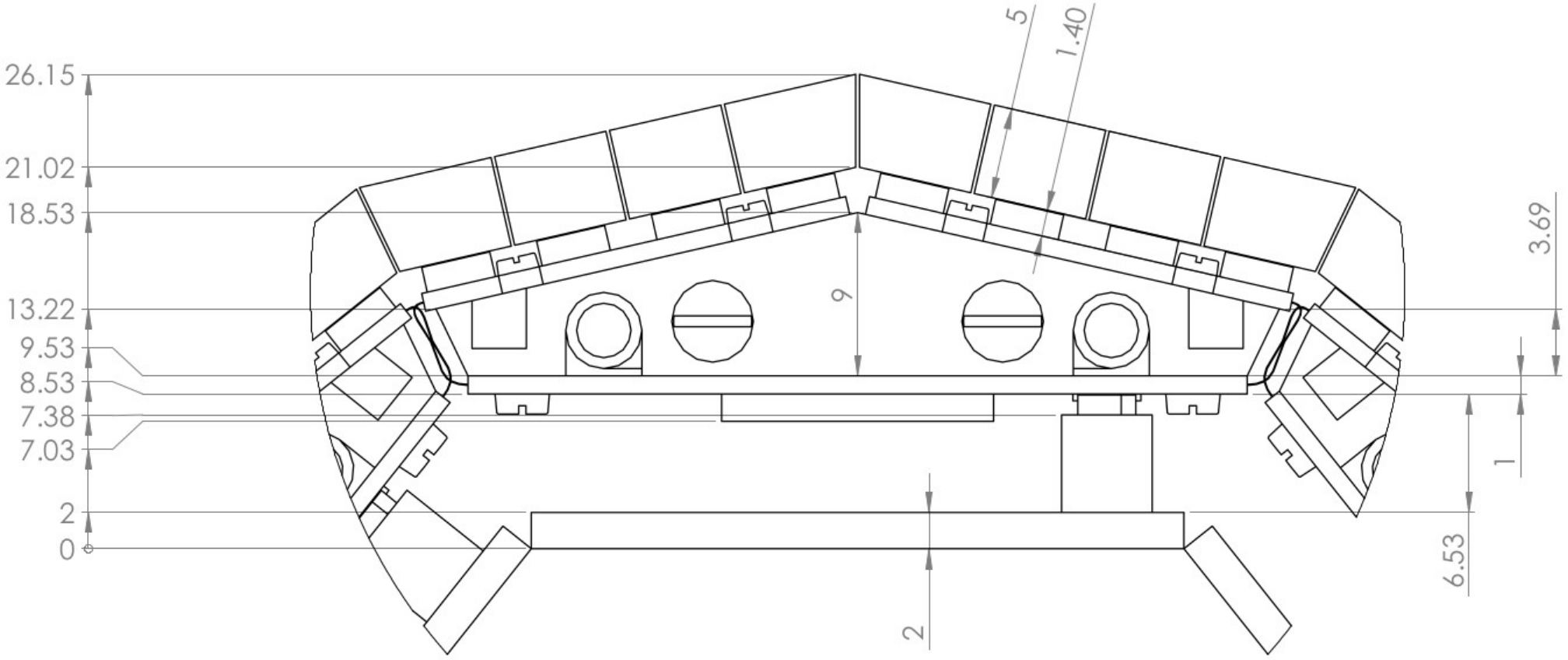
- Where to shrink further?
  - Flex also on FEB, (ASIC side only) would give another ~800um
  - Only small room for improvement on component heights (MALIBU)
  - Current testbeam results seem to allow to reduce the tile size, but...
  - Radiation damage and degradation SiPMs, actual temperature, noise environment, full system performance etc. not studied / can not be concluded yet
  - This should only be a last resort

Outlook 2018

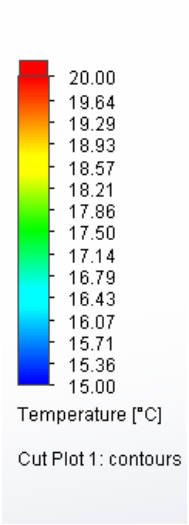
Milestone	BVR 48	BVR 49
Prototype of support structure & cooling	Q2/17	✔
prototype of TileFEB (with STiC3.1)	Q3/17	✔
32 channel technical prototype (support, cooling, FEB, STiC3.1)	Q4/17	✔ (96 ch)
MuTRiG test	Q4/17	✔
MuTrig Integration	Q4/17	Q3/18
Develop QA scheme	Q1/18	Q2/18
Mass production strategy	Q1/18	Q2/18
Readout integration into DAQ and slow control	Q2/18	Q3/18
Cooling simulation for full detector		Q1/18
Full prototype –modified mechanics, MuTrig	Q4/18	Q4/18*

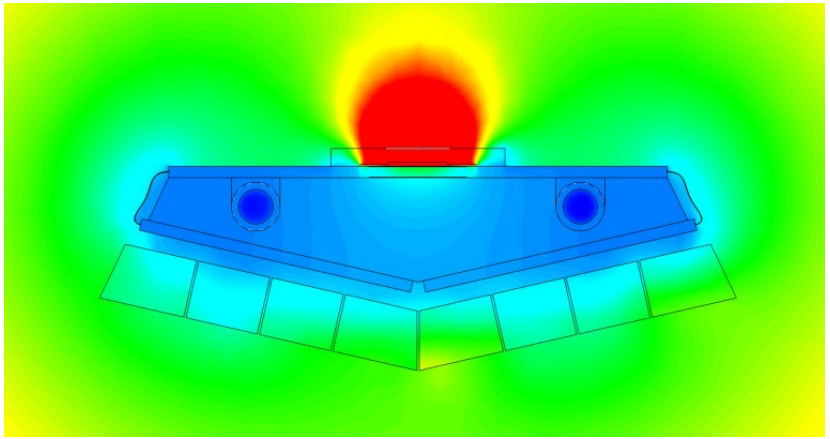
*based on funds

Tile mechanics r-phi detail



Submodule thermal simulation





Simulation input: P=2.1W
Tw = 15C
Ta = 21C
dV/dt = 4.7cm³/s

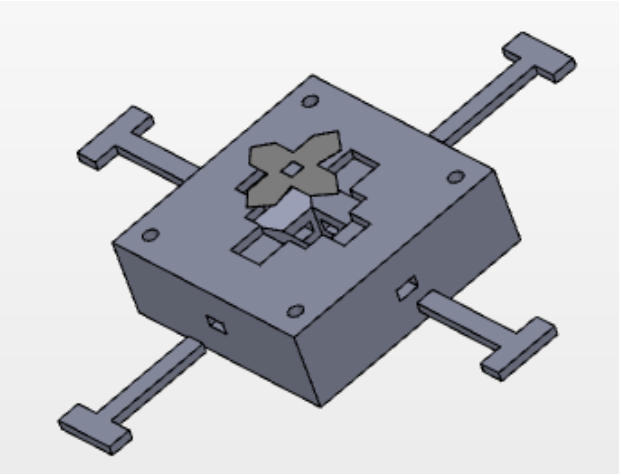
No. of lines per Module

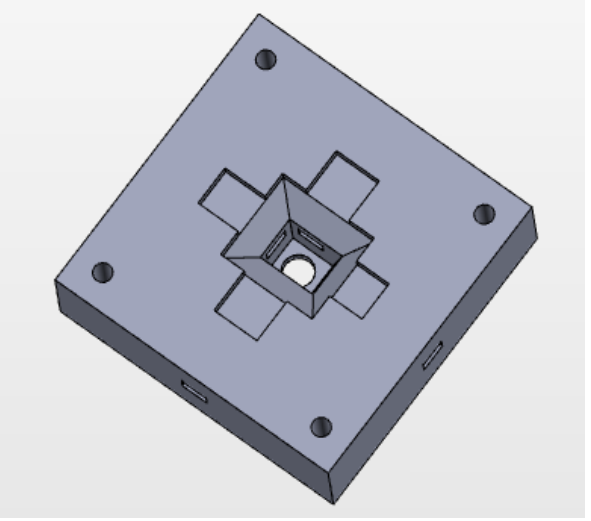
Component	Signal type	Signal names	Shared lines	Per FEB signals
SiPMs	HV	HV	7 ?	
MuTRiG	LV Power	1.8V-A, GND-A	2	
		1.8V-D, GND-D, 3.3V-D	3	
	clock	SER_CLK* 625 MHz/s PLL_REFCLK* 625 MHz/s	2	
	data	SER_DATA 1.25 GBit/s		2
	Slow control(up to 50 MHz/s, we use 2MH/z)	SCLK, SDI, SDO, CS (multiplex)	8	
		CH_RST, CHIP_RST	2	
	Debug/monitor	PLL_TEST_IN	2	
		EXT_TRIG* 1 (removed)		
		CEC_CDO, CEC_CS(multiplex)	6	
Temperature sensor	I2C	SDA, SCL (multiplex)	2	
Summary			34	2
Total per Module			62	
Total for recurl station			434	

The technical prototype: Tile Wrapping

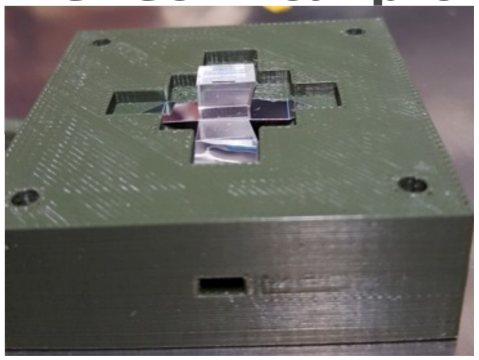
Wrapping tools:

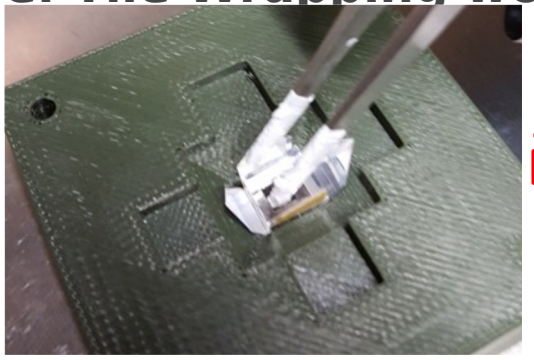
- Produce two for different type of tile
- Assembly of half module (16 channels) ~30min

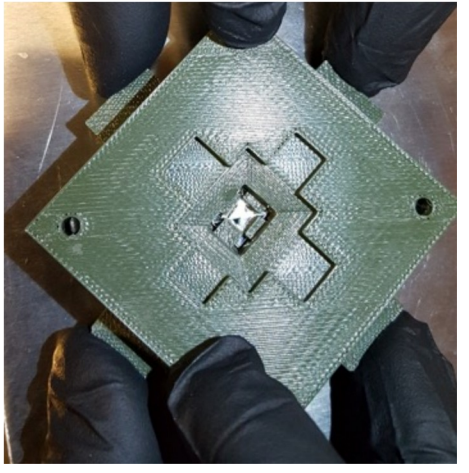




The technical prototype: Tile Wrapping work flow

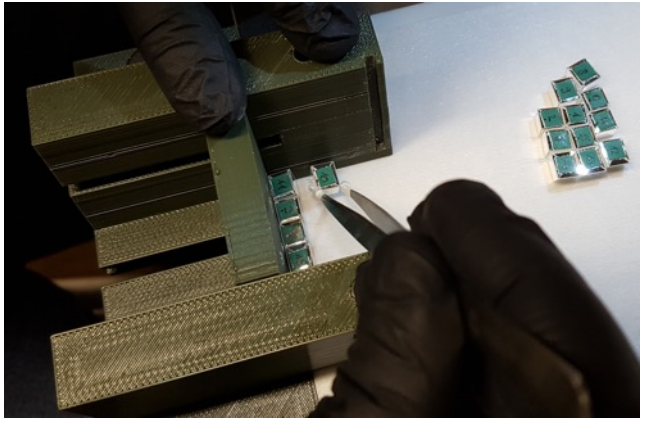






Submodule assembly

- Testing the ASIC and fully equipped the PCB (electronic lab)
- First measurement (DCR, Laser)
- Using micrometer for tolerance check of the tile size before wrapping
- Tile wrapping
- Glue 16 channel together, to avoid tolerance issues
- Dispense glue
- Monitor for bubbles after 24h of curing



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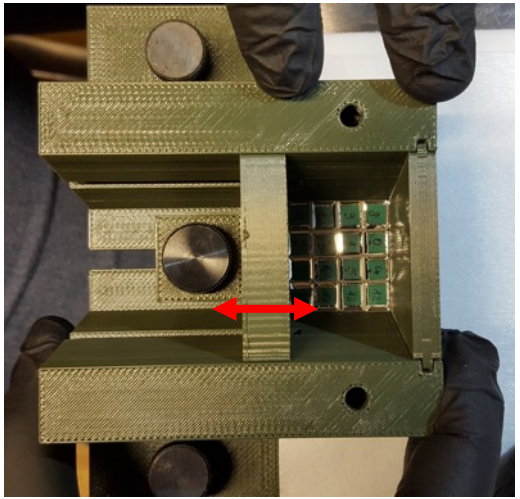

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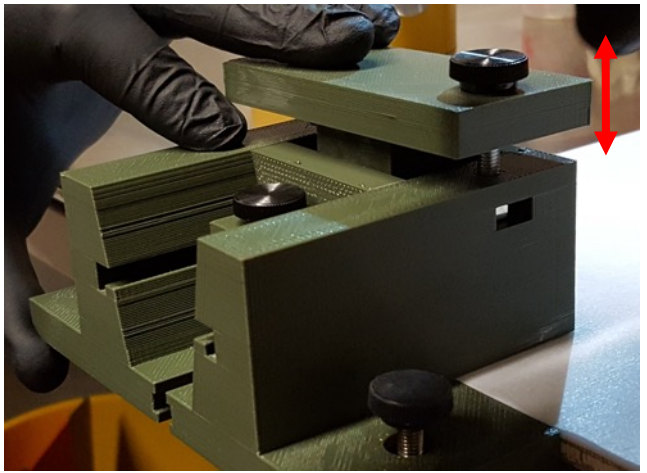

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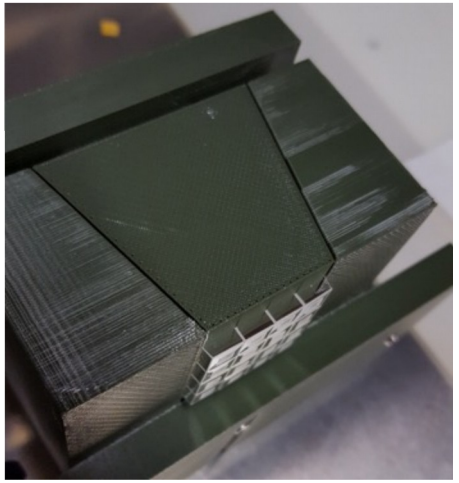

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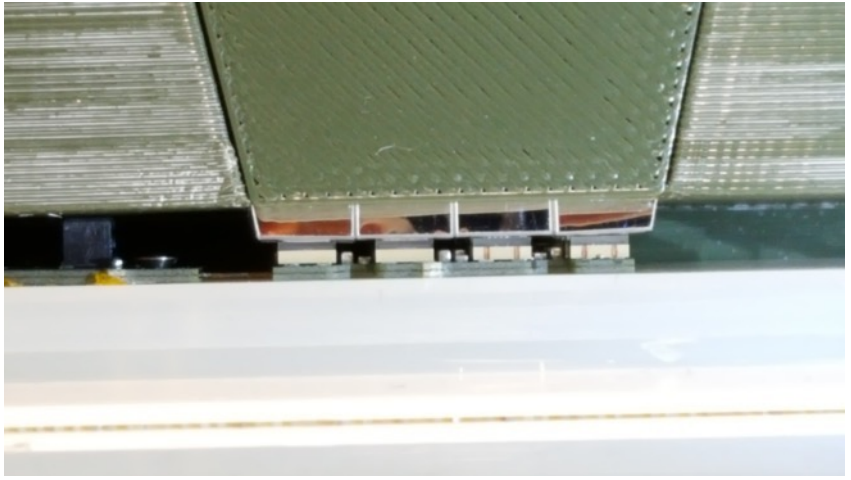

Submodule assembly

- Testing the ASIC and fully equipped the PCB (electronic lab)
- First measurement (DCR, Laser)
- Using micrometer for tolerance check of the tile size before wrapping
- Tile wrapping
- Glue 16 channel together, to avoid tolerance issues
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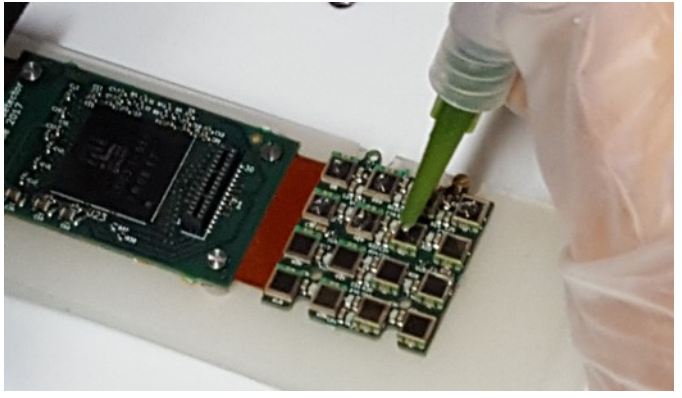

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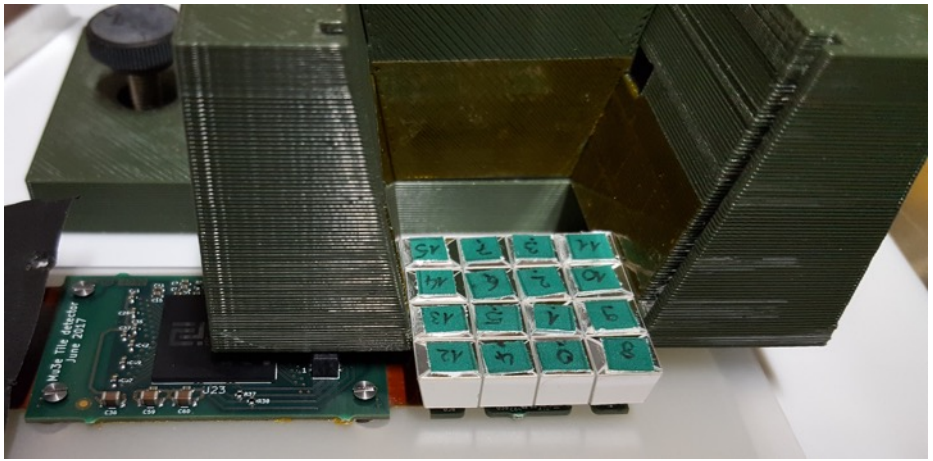

Submodule assembly – Glue issues

- Very important to monitor for bubbles – can reduce light yield by 50%
- After several trial, updates assembly tools and find the correct amount of glue, we managed to have a full matrix without bubbles
- New solution under test:
  - 3M OCA- layer of adhesive 125um protective film from both sides (125um)
  - Cut desired shape using the laser cutter
  - Only press, no bubbles!