MuTRiG Status and Issue Update

Wei Shen

Kirchhoff Institute for Physics (KIP),
Heidelberg University

Mu3e Integration Meeting
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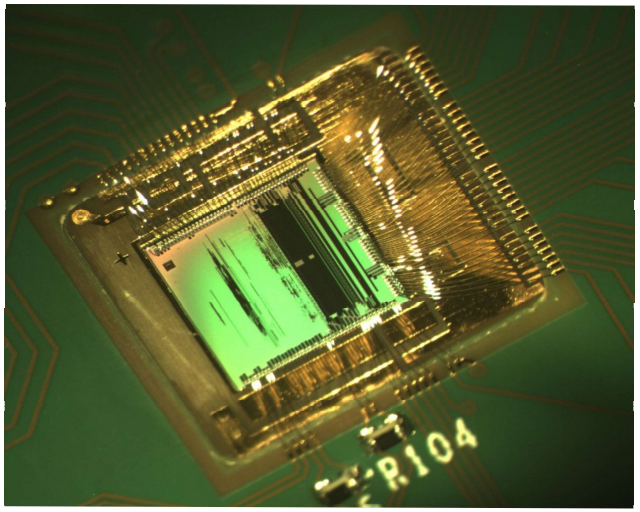
MuTRiG chip

- Mixed-signal SiPM readout ASIC for precise timing applications
  - 32 channels
  - Individual SiPM bias tuning
  - 50 ps time binning TDC
  - Gigabit serial data link (1.25 Gbps)
  - Switchable event length (48/27 bits)
- Digital functionality
  - External trigger
  - Cyclic Redundancy Check (CRC) for transmission error detection
  - Channel event counter

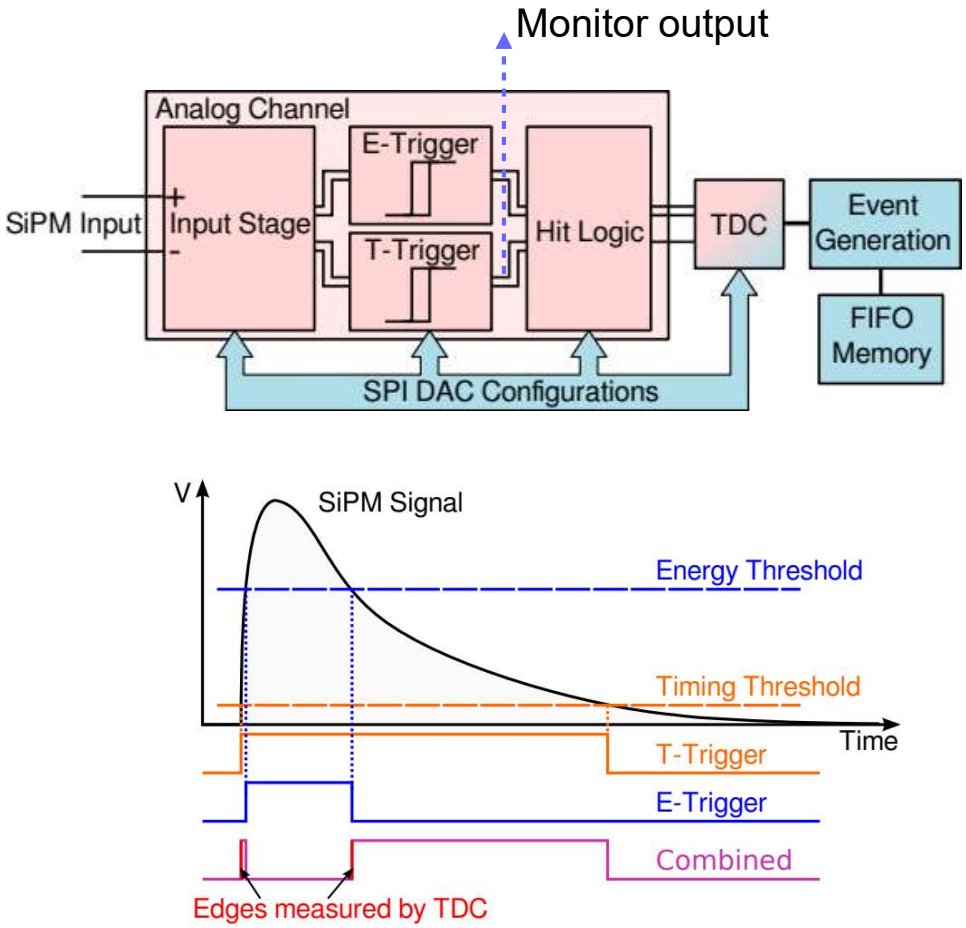


5 x 5 mm^2

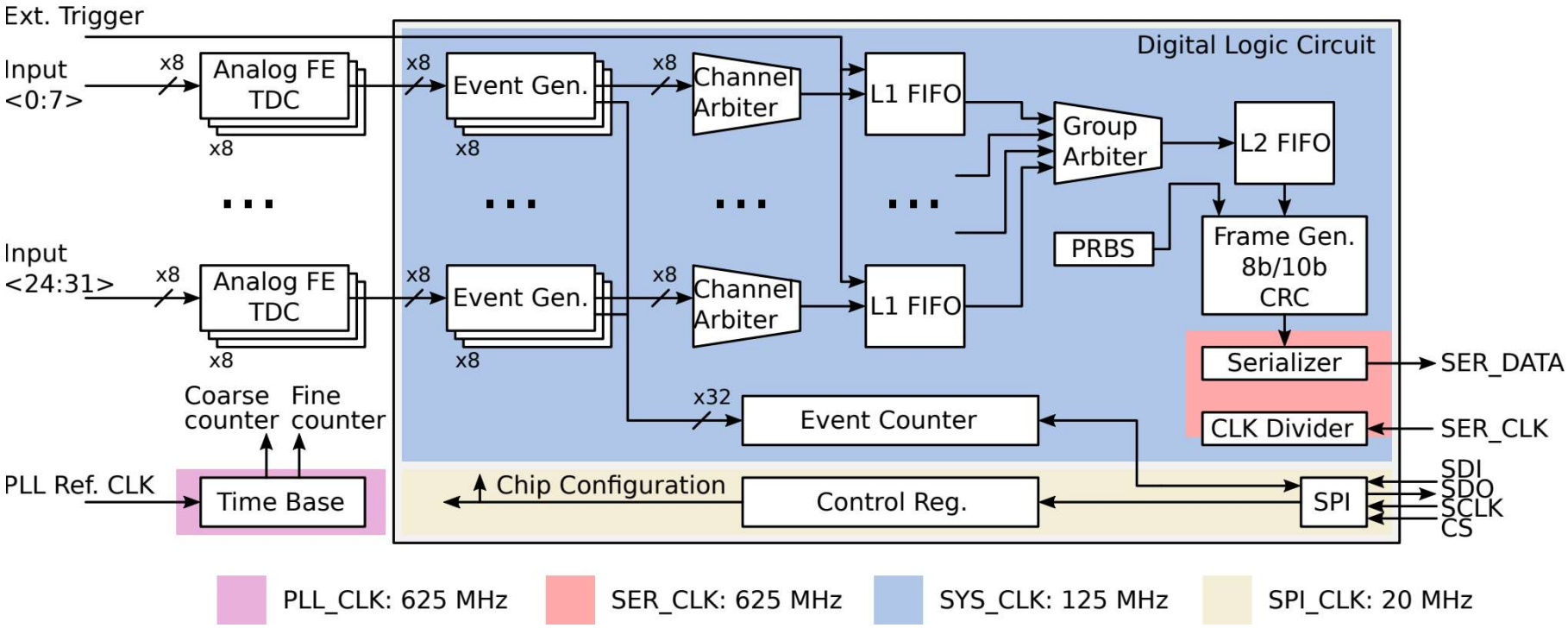
Channel diagram

- Fully-differential analog front-end – *for better noise immunity*
- Separate timing and energy threshold
- Energy measurement with Time-over-Threshold (ToT) method
- Monitor pins for debug

- Encode arrival time and energy information into two rising edges of the combined signal



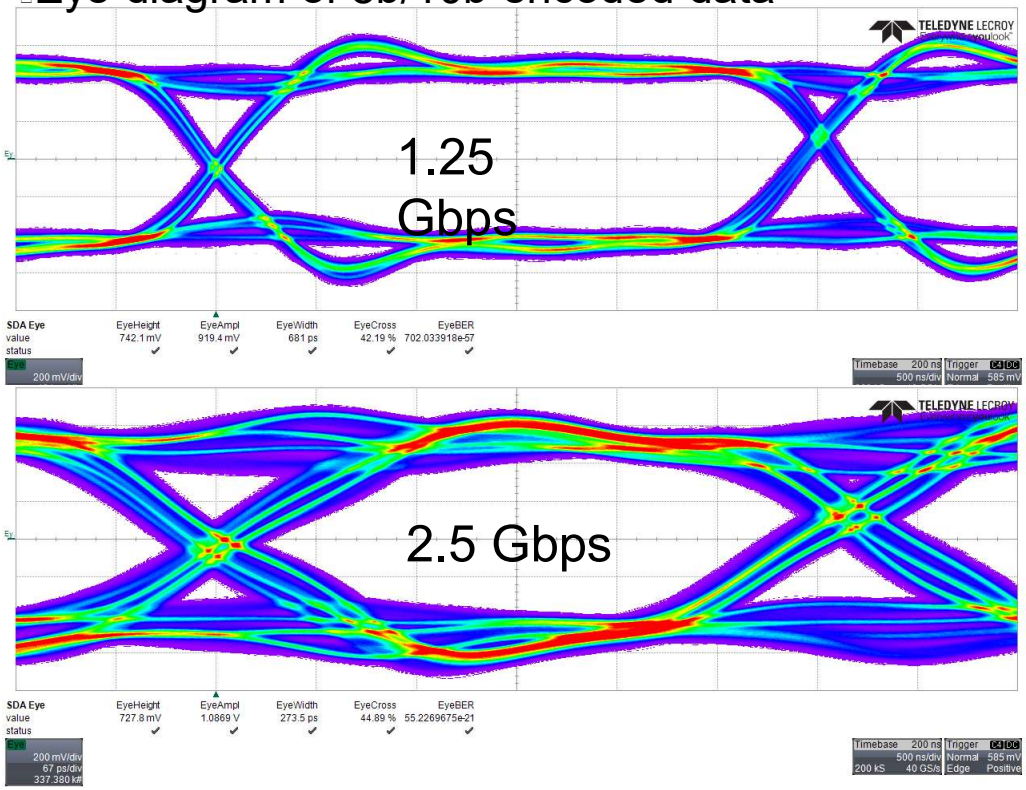
Chip diagram



- Two data frames : **Standard (48 bits)** and **short (27 bits)** event length
- Serializer clock 625 MHz
- Double data rate (DDR)

LVDS TX cell and Serial data link quality characterization

- Pseudo-random binary sequence (PRBS) is generated and observed on a scope after the customized LVDS TX cell.
- Eye diagram of 8b/10b encoded data

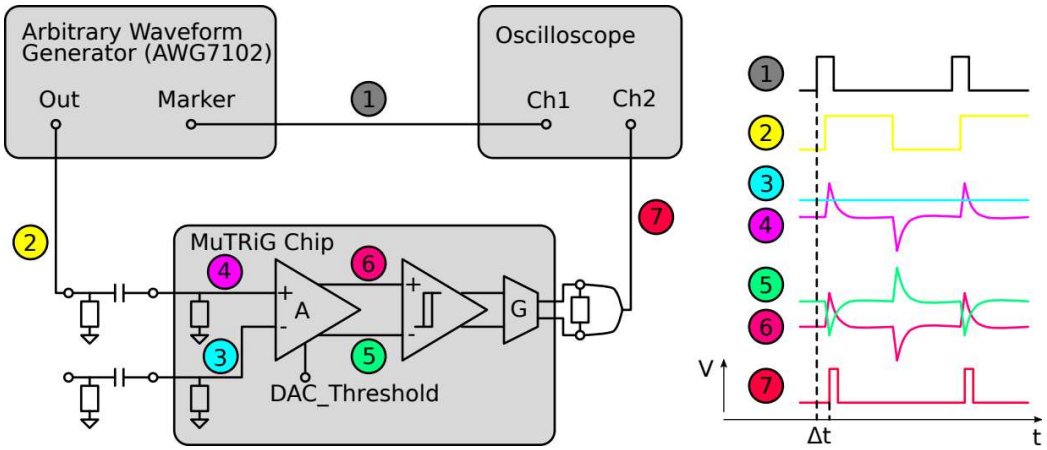


- PRBS sequences and CRC information are used for bit error detection with running setup for **~37h.**

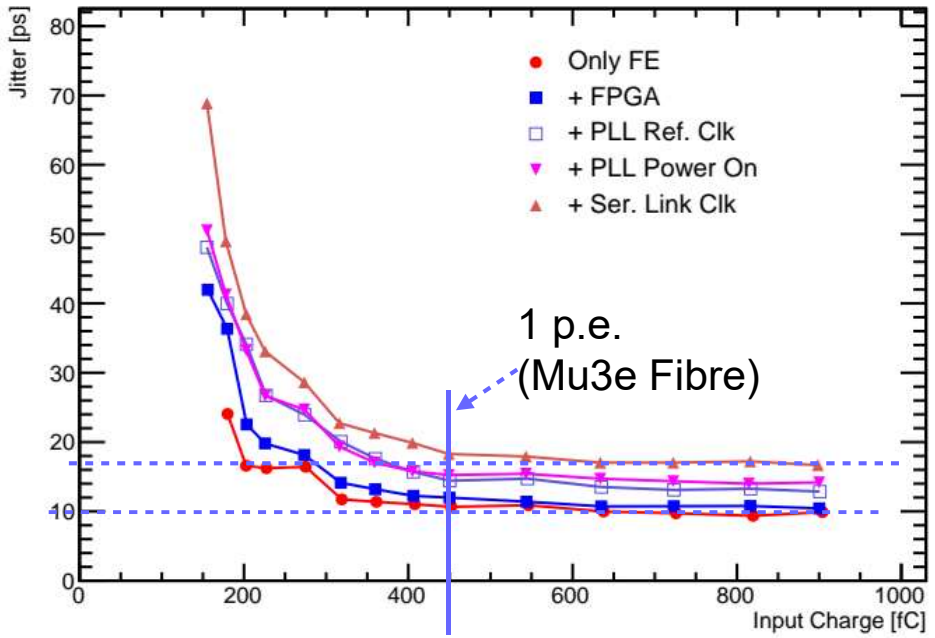
- Bit error rate (BER) - upper limit of $O(10^{-15})$ for bit rate up to 1.9 Gbps.

Bit rate	Bit Error Rate
1.25 Gbps	< 5.90E-15
1.50 Gbps	< 4.34E-15
1.60 Gbps	< 4.63E-15
1.90 Gbps	**< 3.65E-15**

Front-End jitter measurements

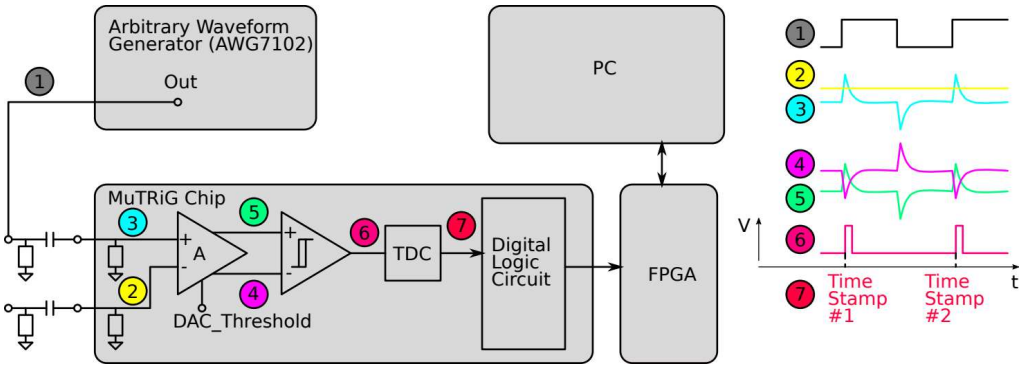


[Measurement setup, Capacitor = 15pF]

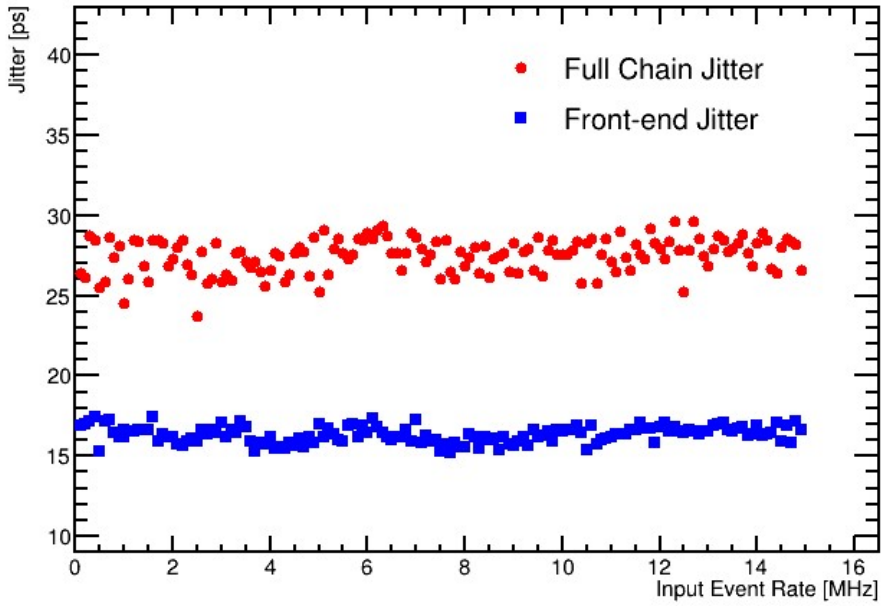


- For charges > 480 fC (1p.e. Mu3e Fiber)
  - FE Jitter **< 12 ps**
  - FE jitter **< 18 ps,** when FPGA, clocks and PLL are all on.

Full-Chain jitter measurements vs event rate



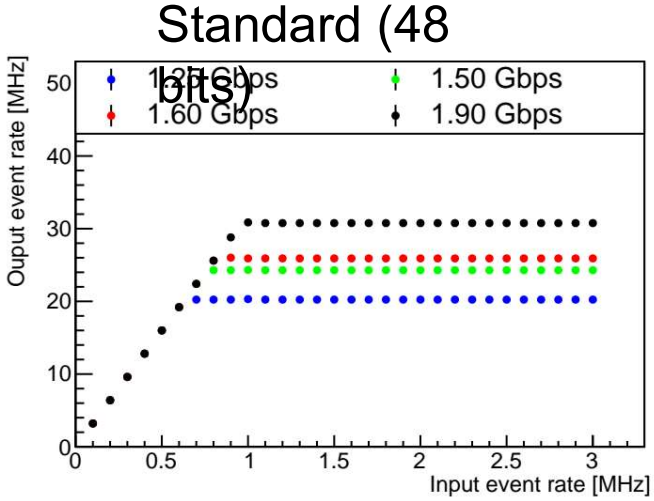
[Measurement setup, Capacitor = 15pF]

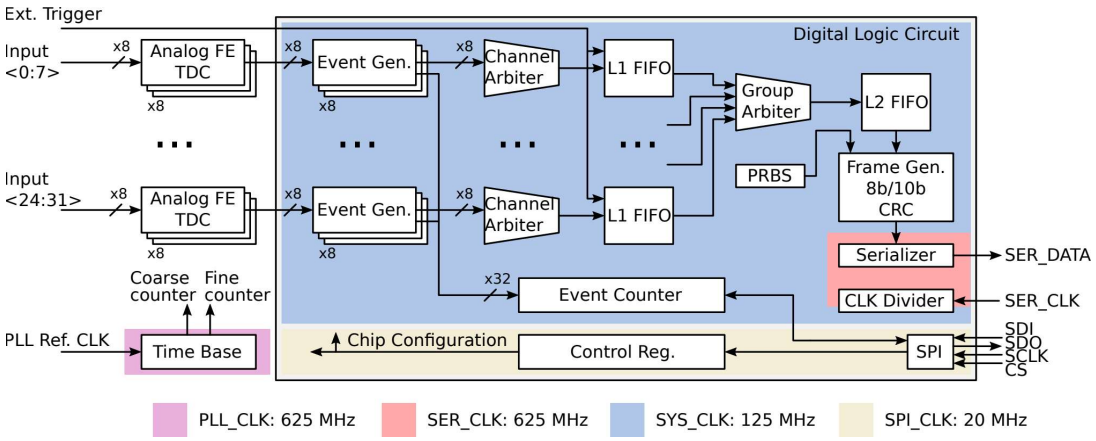


- **Jitter < 30 ps up to 15MHz** input event rate.

- Full Chain jitter is dominated by the digitization error from TDC

Maximum Event Rate @ different serial data link speeds



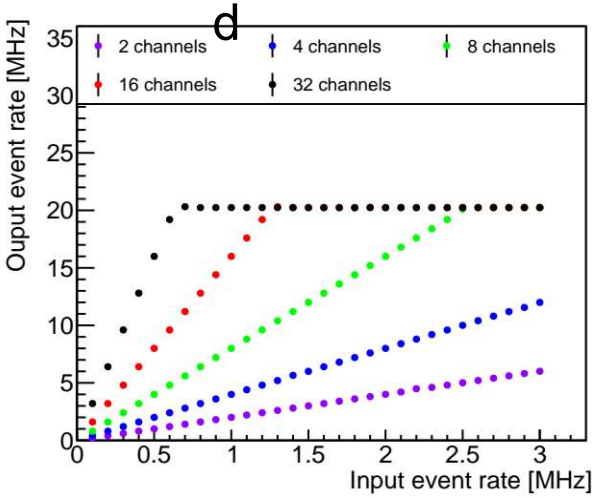


Bit rate	***SER_CLK freq.***	***Max. Event Rate (std event, 48 bis)***	***Max. Event Rate (short event, 27 bits)***
1.25 Gbps	625 MHz	20.24 MHz (632 kHz/ch) expected	25 MHz (781 kHz/ch) expected (1.2 MHz)
1.90 Gbps	950 MHz	30.77 MHz (962 kHz/ch)	38 MHz (1.188 MHz/ch)

Digital Functionality Validation

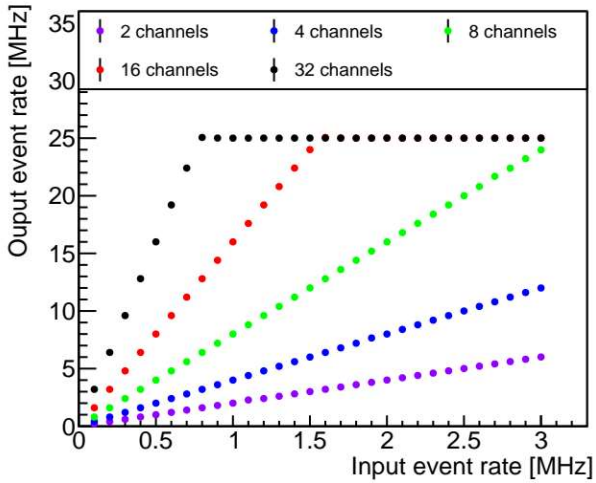
- Maximum Event Rate measurement

Standard



- **48 bit**/event: both time and energy info.
- Event Rate limit: 20.24 MHz (632 kHz/ch)
- More than sufficient for Mu3e Tile detector (60 kHz/ch)
- Limited by 1.25Gbps serial data link

Short



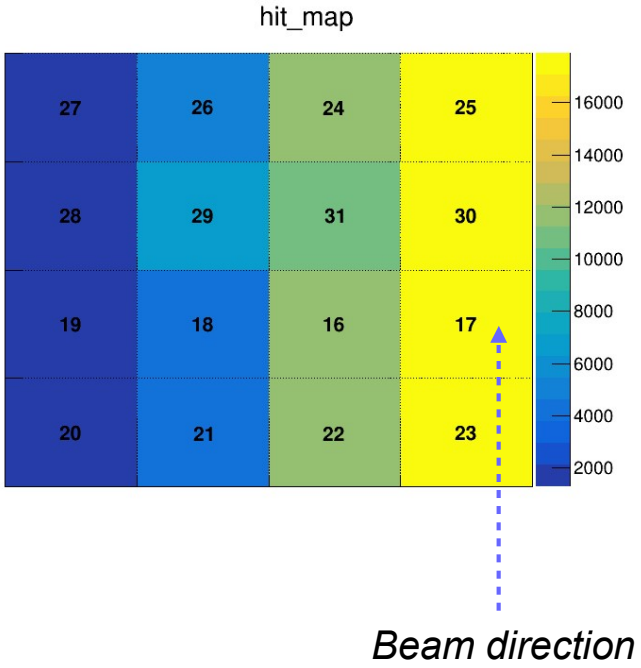
- **27 bit**/event: time info. + 1 bit energy info.
- Event rate limit: 25 MHz (781 kHz/ch)
- Not sufficient for Fiber detector (1 MHz/ch)
- Currently limited by digital part (fixed in next tape-out)
- Expected event rate 35 MHz (~1.1 MHz/ch)

Test beam results

- At DESY, Febriary 2018 with positron beam at 2.4 GeV

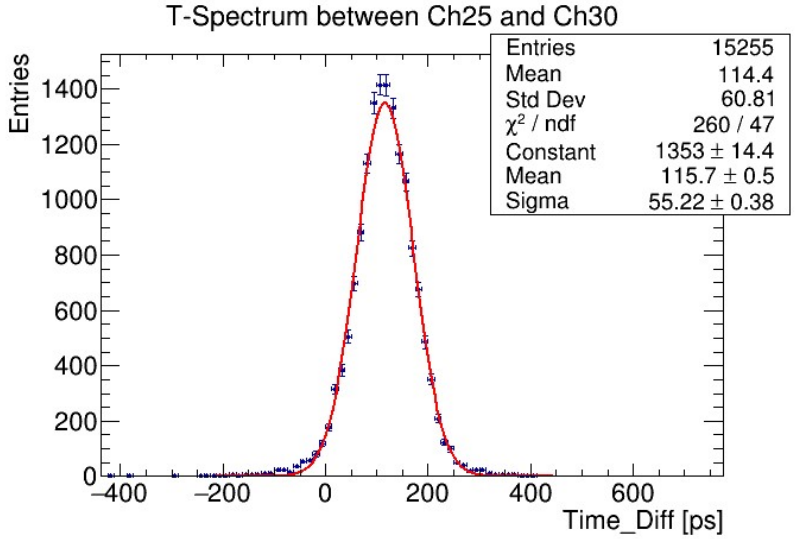
MuTRiG setup

Mu3e Tile detector



Test beam results – preliminary!

- Coincidence time resolution



- Scintillator:
  - - type: EJ228
  - - size: 6.5 x 6.5 x 5 mm^3
- SiPM:
  - - Hamamatsu 50µm pitch
  - - Size: 3 x 3 mm^2

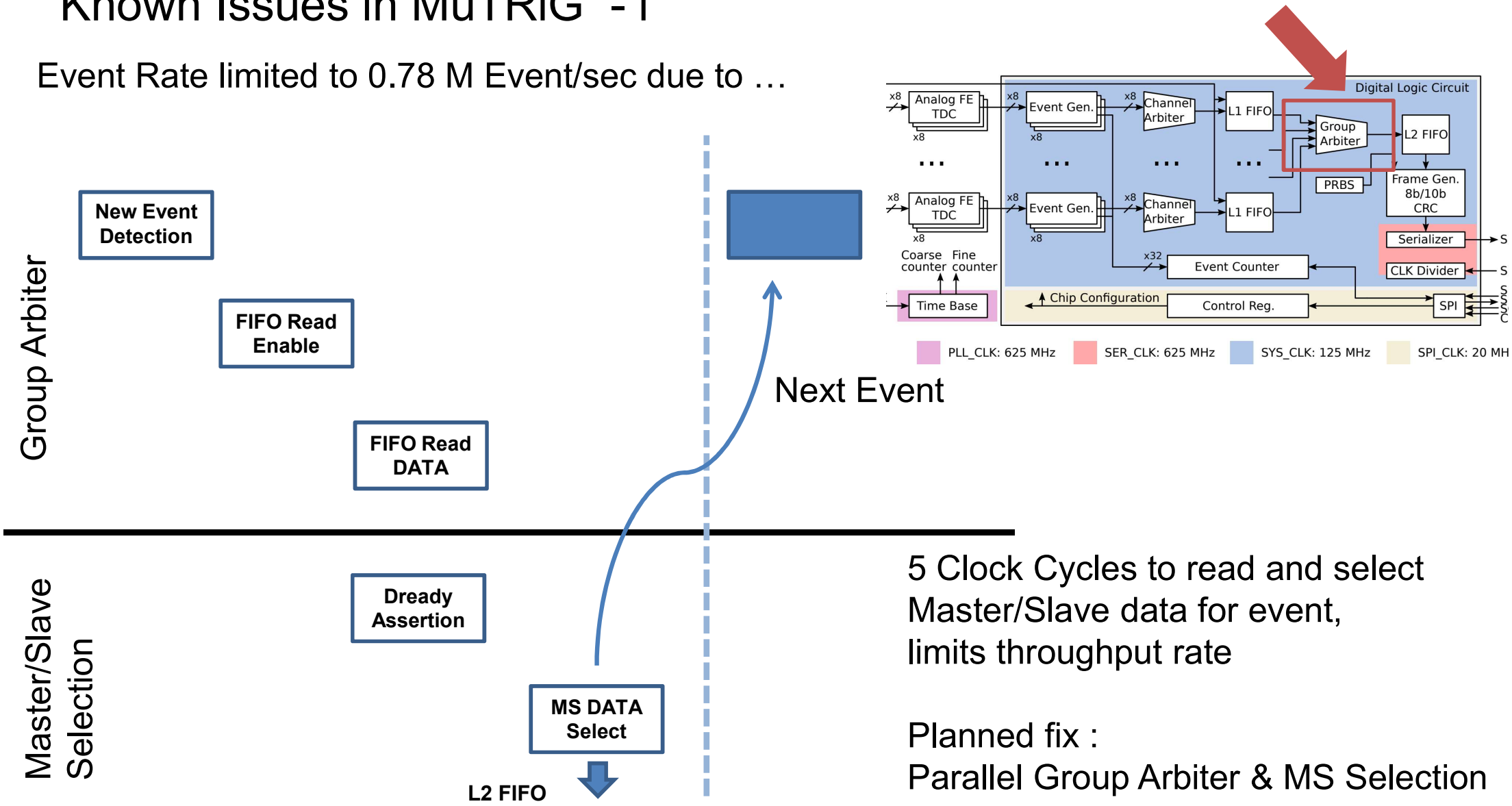
Channel N	σ
17	39.3 ps
23	45.6 ps
25	43.0 ps
30	34.7 ps

- **Achieved timing resolution** for the tested channels
- **σ = 40.6 ps << 100 ps!**

Known Issues & Plan

Known Issues in MuTRiG - i

Event Rate limited to 0.78 M Event/sec due to …

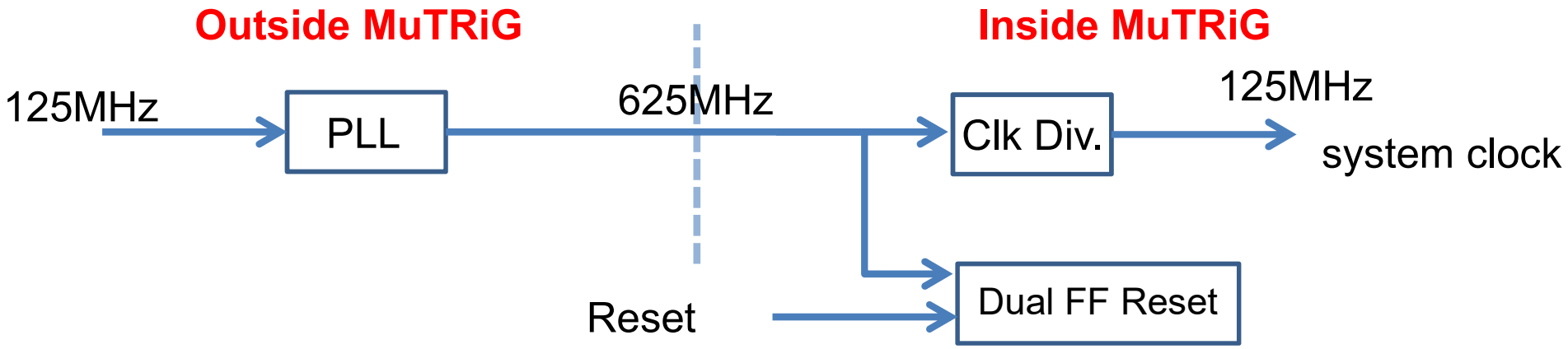


5 Clock Cycles to read and select Master/Slave data for event, limits throughput rate

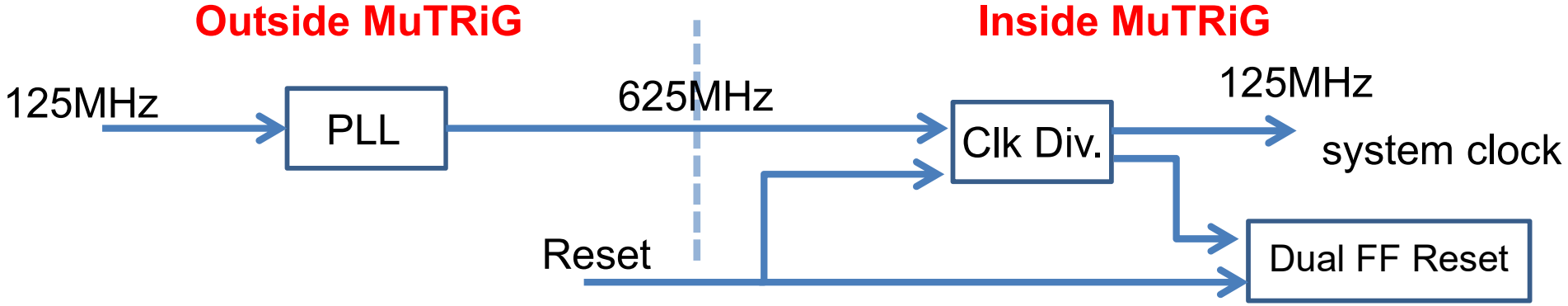
Planned fix :
Parallel Group Arbiter & MS Selection

Known Issues in MuTRiG - ii

Coarse Counter Reset not synchronized to 125MHz system clock with fixed phase after switch on



Planned Fix:



Packaging Related Issues

MuTRiG chip has not been packaged yet, however, the STiC chip is packaged with BGA of 1.5*1.5 cm2.

COST : 15k – 20k per design, according to number of chips

Question : For the tile detector , preferred one chip / Package, what about fibre tracker?

Problem:

STiC has experienced cooling issues with globtop and wire bonding
The thermal expansion coefficient difference of epoxy and aluminum wires creates Failure in connection

Packaged chip much better !!

Software Related Issues

CADENCE Innovus replaces First Encounter as the customed design flow tool

EUROPractice License on First Encoutner ceases
now flow using Innovus needs to be established,
most command should be the same except
clock tree synthesis and process corner treatment

This means :

Additional Design time needed, estimation , 2 months

Time Plan and etc.

4 months foreseen for the design effort of MuTRiG 2
this includes both flow and design modification

Submisstion estimation at the end of 2018 or Beginning of 2019

Nov. 5th , 2018 or Feb. 12, 2019

Design Compaign will be started in July first

Last but not least, Finance of submission and packaging is still not secured ……

Summary

- MuTRiG ASIC fully operational
  - Excellent analog front-end
  - Full chain jitter < 30 ps (charge = 480 fC; rate < 15 MHz)
  - The digital functionality works well *(External trigger, Switchable hit event structure, RPBS, CRC, channel event counter)*
  - BER upper limit of $O(10^{-15})$ for gigabit serial data link
  - Maximum event rate
    - Std Event structure: 632 kHz/ch @ 1.25Gbps;
    - Short event structure: 782 kHz/ch @ 1.25Gbps;
- Future plans
  - Digital part to be improved
  - Tests with Mu3e detectors
  - New submisstion at the end of 2018
  - Packaging plans need to be discussed