Chapter 12

Cooling infrastructure

The detectors, their electronics, the power converters and the data acquisition systems are located inside the densely spaced Mu3e magnet. The heat they produce is transferred to the outside by forced convection cooling. Except for the pixel sensor chips, we are using water cooling everywhere. For the pixels, a novel gaseous helium cooling has been developed.

12.1 Water cooling

Water cooling is used to cool all the front-end electronics which are located outside the active volume of the detector, i.e. the front-end ASICs of the timing systems, the front-end FPGA-boards, the DC-DC converters, voltage regulators, etc. The anticipated heat load per source is listed in Table 12.1 and totals to about 5 kW. To protect the detector from ice buildup, the water inlet temperature is required to be above 2 °C, although the helium atmosphere provides a dry environment with a dew point below −40 °C. Pipe systems inside the experiment distribute the water to the heat sinks, see Figure 12.1. The FPGA boards are cooled via a manifold embedded into the circularly shaped crates. The DC-DC converters for the pixel powering are directly connected to a cooling loop. Heat dissipation for the low-voltage power distribution between the DC-DC converters and the front-end electronics (MuTRiG and MuPix ASICs) is a potential issue for the copper rods around the beam-pipe. Due to this issue active cooling of them is provided through a dedicated cooling ring thermally coupled to the rods. The timing detectors have their own cooling loops to dissipate the heat from the front-end ASIC and to keep the SiPM at a controlled low temperature. Further details on detector cooling of the timing systems can be found in chapters 10 and 11, and on cooling of the FPGA boards inside the crate in chapter 17.

Chilled water will be used from the PSI main supply via heat exchangers. Additional chillers are in place for circuits requiring lower set temperatures. The timing detectors will receive their independent chilled water loops for enhanced control of their temperatures.

System	Est. power W
Crate (front end FPGA boards)	2700
DC-DC converters	1500
Copper rods	200
Fibre detector (MuTRiG, SiPM)	120
Tile detector (MuTRiG, SiPM)	420
Total	4940

Table 12.1: List of systems requiring water cooling inside the experiment, with a conservative estimate of the heat dissipation. All circuits will be run independently.

12.2 Helium cooling

All MuPix chips of the pixel tracker are cooled by gaseous helium of $T_{\mathrm{He,in}} \gtrsim 0\,^{\circ}\mathrm{C}$ at approximately ambient pressure. Assuming a maximum power consumption of the pixel sensors of $400\,\mathrm{mW/cm^2}$ the helium gas system is designed for a total heat transfer of 5.2 kW, which increases the averaged gas temperature by about 18 °C.[1] For this, the helium cooling system has to provide a flow of about $20\,\mathrm{m^3/min}$ (equal to 56 g/s of helium) under controlled conditions split between several cooling circuits (see section 7.6).

A process flow diagram for the helium plant is shown in Figure 12.2. Helium is pumped using miniature turbo compressors run at turbine speeds of up to 240 krpm. These units provide compression ratios up to ≈ 1.2 at mass flows in the range up to 25 g/s, depending on supplier and model. The energy consumption of the compressors for the full system is estimated to be around 6 kW in total. The helium circuits are designed with minimised pressure drops for a most economic system layout. The combination of a compressor and a valve for every circuit allows the control of the mass flow and the pressure differential applied individually. Compact, custom made Venturi tubes will be used to monitor the mass flows of every circuit. Leaks lead to losses and will contaminate the helium with air. In addition, outgassing organic residues from electronic components and adhesives need to be removed. Hence a cold trap is included in a by-pass configuration to keep the helium pure enough. An expansion volume will be present to compensate for the compression and expansion of the gas

[1] The pixel detector consists of 2844 chips (108 in the vertex detector, 3 × 912 in the outer layers), giving about $1.14\,\mathrm{m^2}$ of active instrumented surface ($20 \times 20\,\mathrm{mm^2}$ active area per chip, neglecting the chip periphery) or about $1.3\,\mathrm{m^2}$ including chip peripheries. The conservative (optimistic) scenario leads to about 5.2 kW (3.3 kW) of dissipated heat. The specific heat capacity of gaseous helium is $5.2\,\mathrm{kJ/(kg\,K)}$.

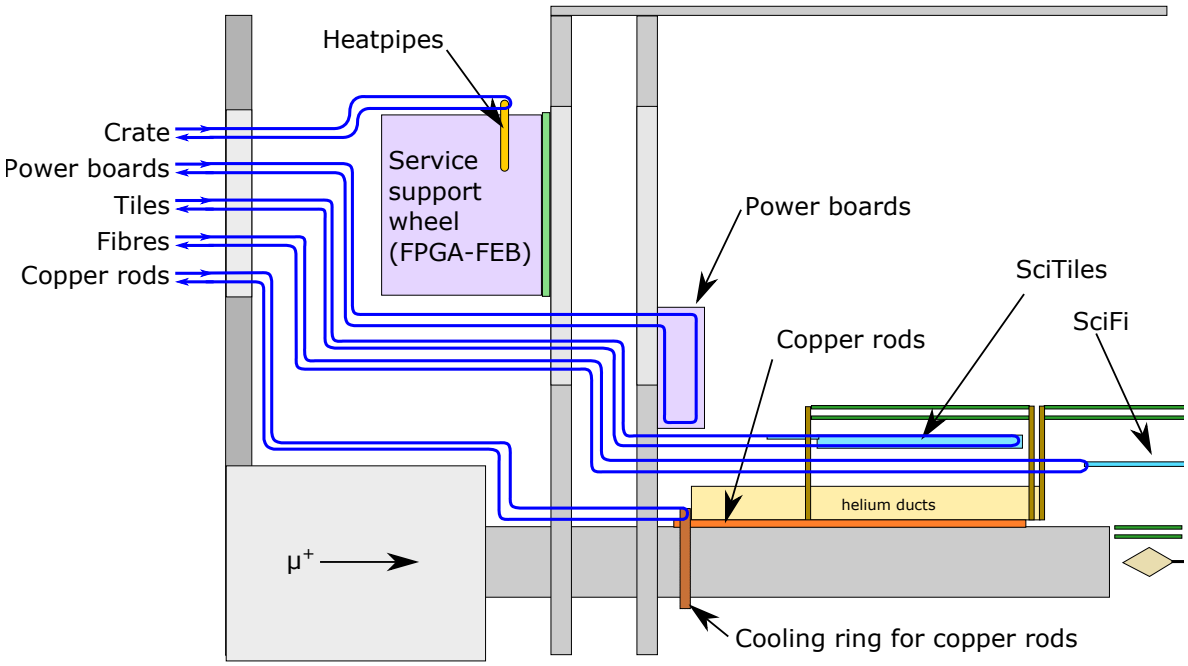

Figure 12.1: Schematic view of the water cooling topology for one quadrant of the experiment inside the magnet.

volume during ramp-up and ramp-down of the gas flows. A low pressure drop shell-and-tube heat exchanger is used to remove the heat from the helium.

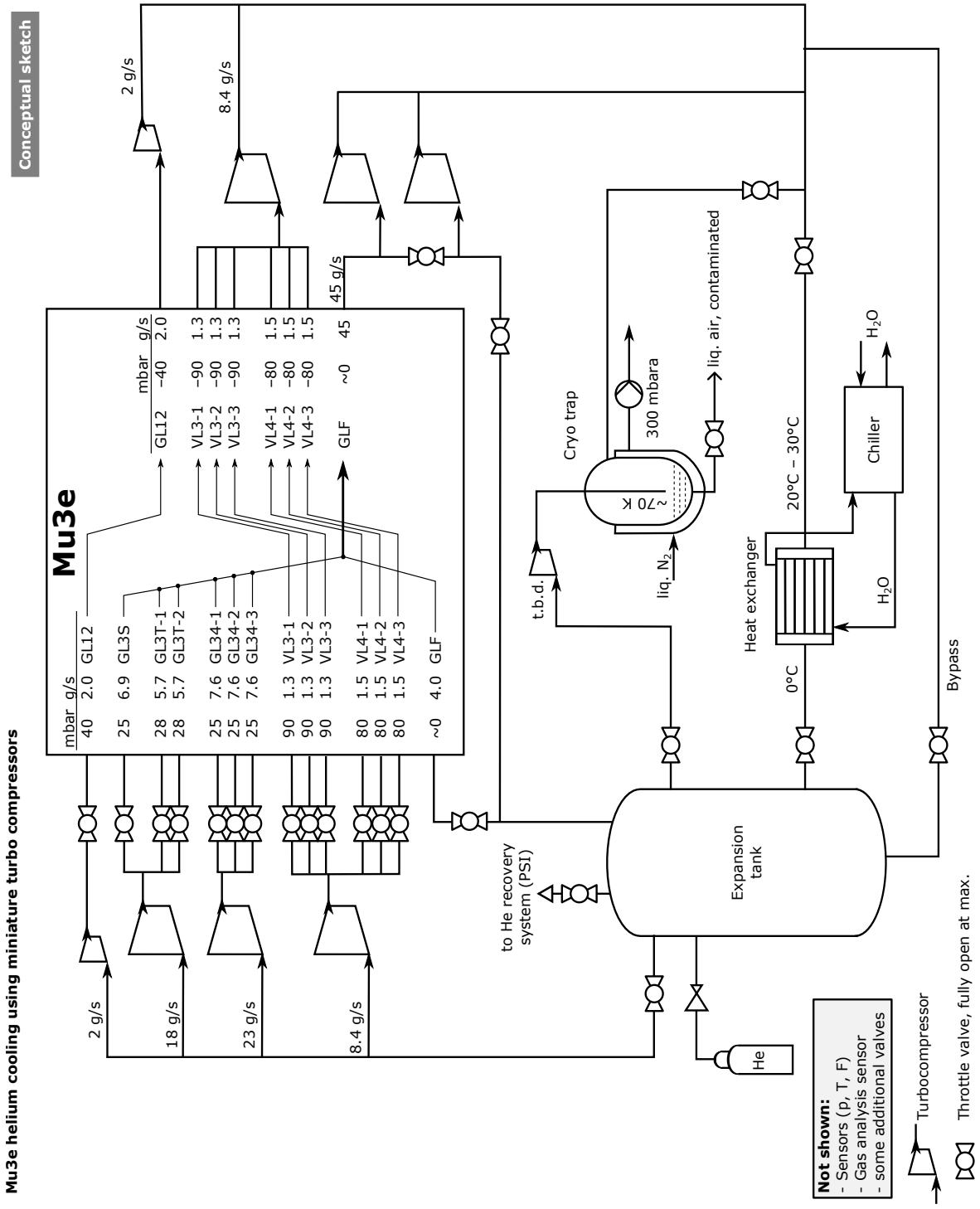

Figure 12.2: Conceptual process flow diagram of the Mu3e helium cooling infrastructure. Miniature turbo compressors in the circuit may be implemented using multiple units operated in parallel or in series, depending on needs.

Chapter 13

Mechanical Integration

The detector is maintained at its nominal position inside the magnet by a removable frame called the *detector cage*. The cage also carries infrastructure such as crates for the power converters and the front-end FPGA boards, and provides support for all cabling and piping.

13.1 Detector Cage and Rail System

The detector cage has the shape of a hollow cylinder with its axis horizontal, as shown in Figure 13.1. At each end, a ring frame made of pairs of glass-fibre reinforced polymer wheels has a clamp at its centre for the beam-pipe. Aluminium struts connect the two ring frames and form the cylinder. Gliders on the wider struts (at the 3- and 9 o'clock positions) guide the cage on the rail system inside the magnet.

To compensate for possible thermal expansion in the x (horizontal, perpendicular to the beam-pipe) direction, the gliders on the left rail are floating whilst on the other rail they are kept at a defined position. In the y (vertical) direction the position is defined by the top surface of the rail. The z position is kept fixed by screws.

The clamps in the centre of the rings at either end hold the two beam-pipes in position and take all the weight of the detector. Mechanisms to fine-adjust the beam-pipe pointing angles are built into the clamps. Finite element simulations were performed to test the sturdiness of the design. Load tests have been carried out on a full-scale mock-up, confirming the simulation results of a deflection of 0.3 mm under a typical detector load of 10 kg at the beam-pipe tips. The connection of the beam-pipes to the beam line is described in chapter 5.

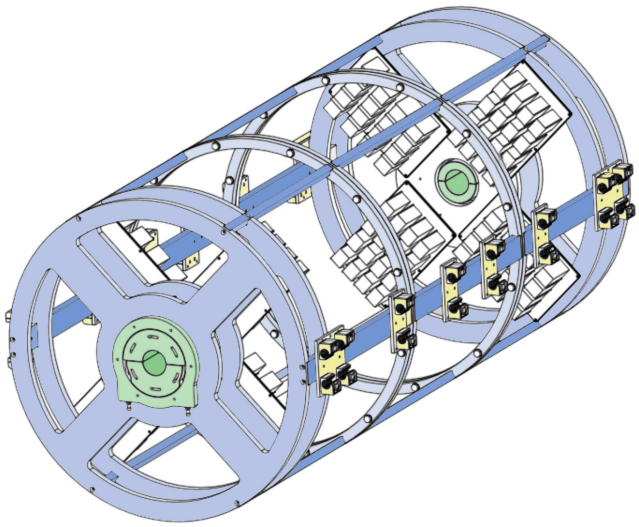

Figure 13.1: Detector cage structure consisting of two ring frames (light blue) connected by struts (dark blue). The clamps holding the beam-pipes are inside the ring pairs at either end (shaded green). The gliders (yellow) allow the cage structure to be moved into the magnet on the rail system.

Detectors can be mounted and dismounted in sequence from inner to outer without the need to retract the beam-pipes. For example to mount the central barrels, the vertex half-shells of layers 1 and 2 will be installed first, followed by the fibre ribbons. Finally, the pixel modules for layers 3 and 4 will be mounted. For this sequence, the cage can be placed on a special extraction cart on wheels. It has the same rail system as that inside the magnet. For better access, the cart has rollers allowing the rotation of the cage around its own z-axis in a safe manner.

The beam-pipes also provide support for other services. The copper bars to supply power to the central detectors (section 14.4) are glued onto the beam-pipe with a custom procedure to ensure proper electrical insulation, and manifolds for the helium cooling system are attached to the ends of the beam-pipes.

13.2 Mechanical support of detector stations

The detector components are mounted on the beam-pipes, see Figure 13.2. As shown in the previous chapters, both pixel and timing detectors follow a barrel concept. They are mounted on pairs of end rings, supported on the beam-pipes. Whilst the recurl stations have their support on one beam-pipe, the central barrel has one mechanical support on the upstream beam-pipe and the other on the downstream beam-pipe. To compensate for any tilt of the end rings and movements due to thermal expansion, the detector mounts are spring-loaded at one end.

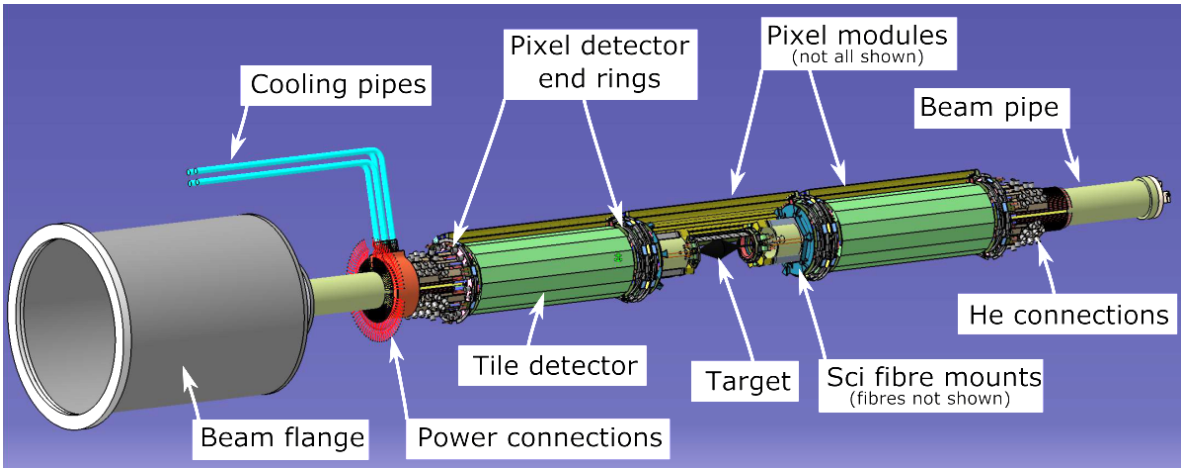

Figure 13.2: The Mu3e experiment mounted on the beam-pipes. Not shown are the detector cage and supplies. Some parts have been partially removed for visibility. LV: low voltage power.

13.3 Supply systems and cable routing

Service support wheels (SSW) are situated outside either end of the detector cage. They are loosely coupled to the cage in the z direction and have their own gliders to decouple mechanical forces from the cage. The SSWs hold crates for the front end boards, patch panels for the power connections and routing for the cooling pipes (water and helium). The DC-DC converter boards (low voltage supply) and the bias voltage generators are mounted on the inner side of the glass-fibre wheels. All services have connections at the outward facing planes of the SSWs. Figure 13.4 shows a conceptual view.

Services have to be routed from the inside to the outside of the experiment through flanges sealing the internal dry helium atmosphere from the ambient environment. Four identical flange plates are mounted on four turrets at the end plates of the magnet, two at either end. Ports for all media are present and provide suitable connectors. For the power connections, sealed heavy-duty double-sided 56 pin connector assemblies are used[1]. Tubes for the helium and water coolants are welded into the flange and will use industry standard fluid connectors. The fibre bundles are sealed with epoxy into brackets that are sealed with an O-ring to the flange. A drawing is shown in Figure 13.3.

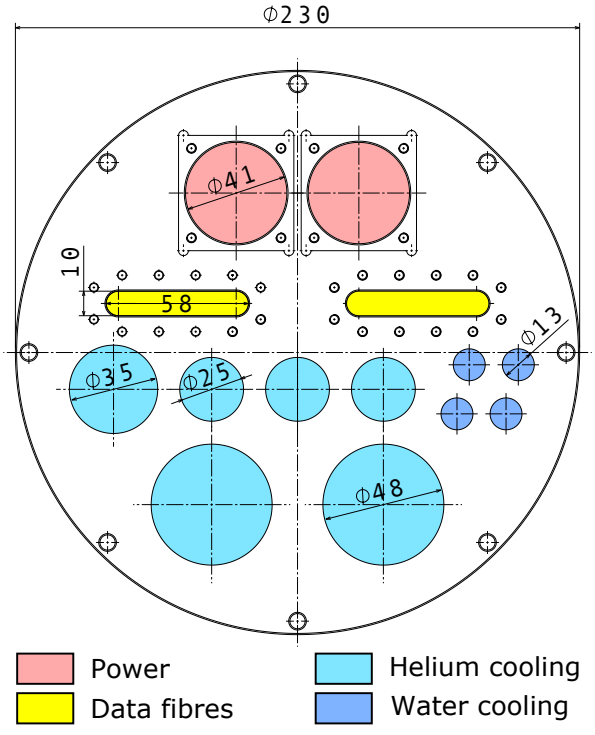

Figure 13.3: Drawing of the cabling flange. Additional ports will be added for auxiliary use. Dimensions in mm.

13.4 Access to the Mu3e detector

Extracting the experiment from the warm bore of the magnet requires an orchestrated procedure, which essentially looks as follows:

1. Detach the beam line, secure cables and hoses. Temporarily remove beam line parts as needed to make space.

2. Move the magnet into the extraction position.

[1] Supplier: Souriau-Sunbank

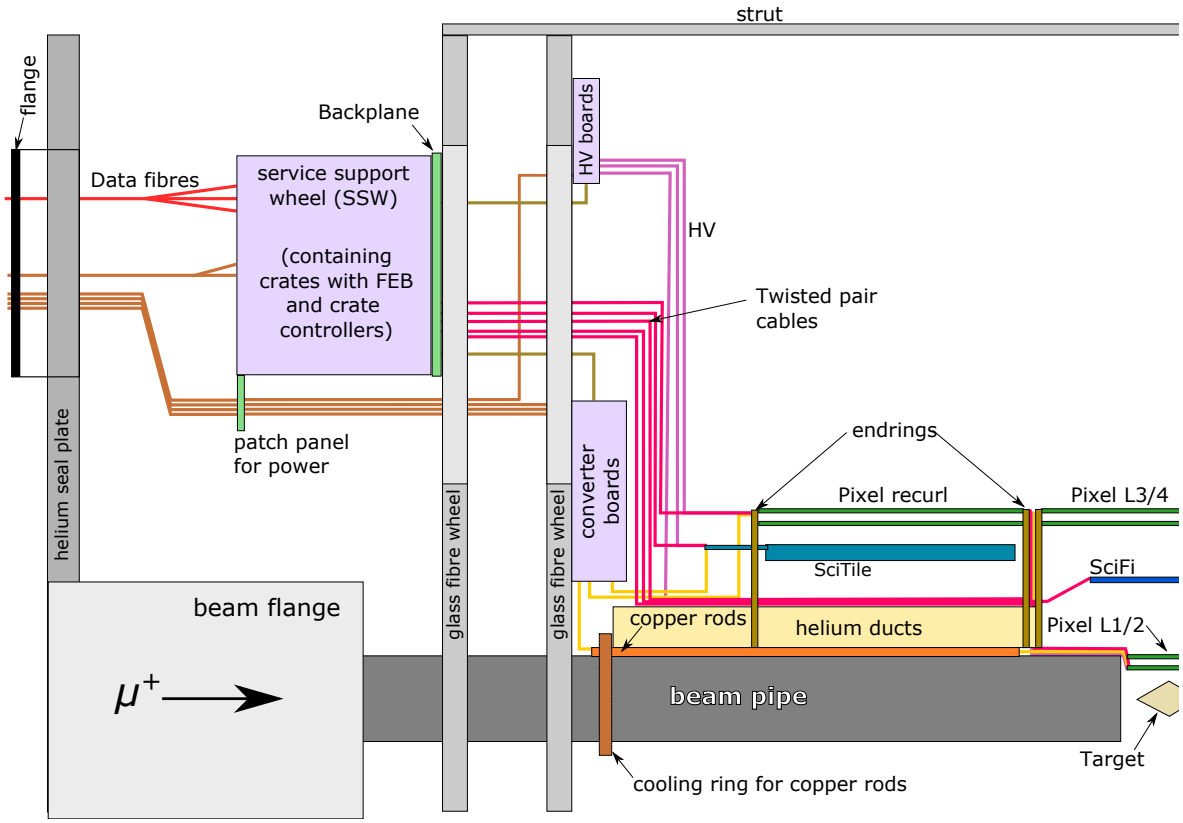

Figure 13.4: Conceptual view of supply system positioning and cable routing (rz-view, not to scale). All supplies can be disconnected for the extraction of the experiment. The feed-throughs on the helium seal plate are gas-tight.

3. Open the magnet doors. Remove access plates from the helium sealing plate.
4. Disconnect all cables and hoses though access holes.
5. Safely remove the sealing plates, secure cables and hoses while doing this.
6. Place extraction cart in front of experiment. Engage rail coupling. Carefully remove experiment, guided by the rails.

For detector insertion, the procedure is reversed. The extraction cart is the same as described in the previous section. Guide pins and clamps help to safely couple the cart to the rail system in front of the magnet.

For servicing the detector, a protective tent will be available that can be used either inside the area for quick work, or outside the area in a secure space. External crane attachment points are provided for transferring the experiment to outside of the beam area.

Chapter 14

Power Distribution and Cabling

With a power consumption from the pixel tracker, the SiPM readout electronics, front-end board, and step-down converters (see Table 12.1) of up to 10 kW, the Mu3e detector needs a robust but also compact power-distribution system. The conceptual design for such a system is shown in Figure 14.1. Power supplies located on the lower infrastructure platform deliver 20 V DC, a voltage high enough to allow for a compact and flexible set of power cables, which are brought into the experiment through a high-density power connector. From there, the power is distributed to either the front-end board crates with embedded buck converters, or to the power boards which step down the voltage for the MuPix chips, and the tile and fibre readout boards. In addition, separate power is provided to the slow control systems which need to run when the main detector power is switched off.

14.1 Power Partitions and Grounding

The Mu3e experiment is divided into 112 detector partitions, which also act as independently controlled power partitions (see Table 14.1). The DC power supplies for these partitions will be the TDK-Lambda GENESYS low-voltage power supply, which are known to be reliable, for example they are being used in the MEG experiment. Each supply can provide up to 90 A / 2700 W, which is distributed to several power partitions via a power relay bank. A massive common return line per supply minimizes the voltage drop. Each power supply output is floating, and the return line is referenced to the common ground inside the experimental cage. Slow control systems such as the alignment system, environment monitoring, the controller boards regulating the detector power, and all safety critical systems are powered separately. This enables the powering of all diagnostic tools of the experiment prior to the turn on of the high-power detector electronics.

This powering scheme means that care has to be taken to not introduce ground loops when connecting the various detector partitions to e.g. a slow control bus or a high-voltage input. To avoid this all data connections to the outside go via optical fibres, the readout is therefore fully electrically decoupled.

14.2 DC-DC conversion

Switching power converters will be used to step down the 20 V to the voltages needed by the detector and electronics (Table 14.2) Typical efficiencies are of the order of to 70% to 90%, depending on the current and the voltage step. Compact high-power converters typically used for FPGA boards such as the LTM4601 (Analogue Devices) have a ferrite core inductor, with is incompatible with the high magnetic field environment of the experiment. Mu3e has selected the following solution: a commercial synchronous buck converter combined with a custom air coil, where the coil properties and the switching frequency are optimized for the required output voltage and current. As they are mounted outside the active area of the detector, these converters don't have to be radiation hard.

14.2.1 Front-end board converters

The front-end boards with an Arria V FPGA, and the LVDS and optical tranceivers (section 17.2) require several DC voltages at typical currents of 1-3 A. Three switching DC-DC converters will generate 1.1, 1.8, and 3.3 VDC with Peak-Peak ripple below 10 mV (see Table 14.2). Passive filters and active filtering with devices such as the LT3086 (Analogue Devices) further reduce the voltage ripple, and allow intermediate voltages to be generated. The switching converters on the front-end board are based on a compact TPS548A20 synchronous buck converter with integrated switches (Texas Instruments), combined with single layer cylindrical air coils. Figure 14.2 shows a stand alone 2x4 cm 1.8 V prototype, which has demonstrated good performance at operating conditions. The converter embedded on the front-end board will have a similar footprint, with an additional copper shielding box covering the coil to reduce EMI and improve mechanical stability [76].

14.2.2 Power boards

With currents potentially up to 30 A and very few options for additional filtering further down the line, the requirements for the active detector DC-DC converters are more challenging. The TPS53219 buck controller and CSD86350Q5D power MOSFET switch from Texas Instruments were identified as meeting these requirements. A first prototype was developed (see Figure 14.3). This board has space for various input and output filter configurations, and

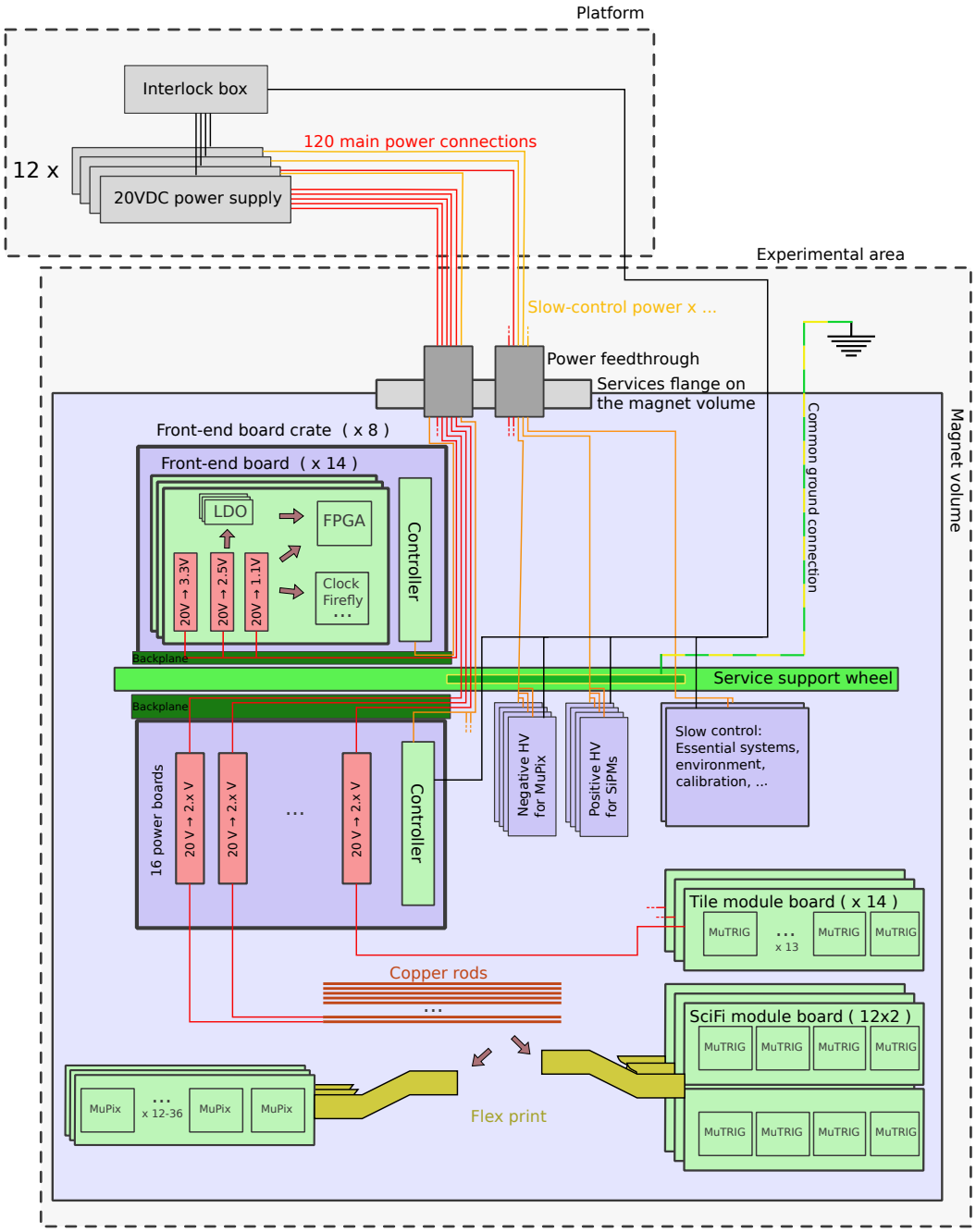

Figure 14.1: Schematic view of the power distribution inside the detector. Floating 20 VDC supply lines provide up to 12 A of current each (red lines). Custom DC-DC converters on the front-end board and close to the active detector step this 20 VDC down to the required voltages. Separate power is provided to the slow control systems (orange lines), which need to run independently from the main detector power. Note that these services are distributed over the upstream and downstream Service Support Wheel (SSW). This SSW also acts as a common ground plane, with a single ground connection to the outside.

has dimensions close to the final form factor. The configuration shown, with a toroidal coil in combination with a secondary LC filter, has the best noise figure with a Peak-Peak ripple of approximately 10 mV. The board was stress tested in a magnetic field, and successfully used to power a MuPix 8 pixel detector during a DESY testbeam campaign.

The final power board has a secondary output filter, and several additional features such as current monitoring, and interface connector for the back plane, and an embedded

Partition type (ASIC)	#partitions	#ASICS/ partition	Maximum power per partition [W] Excluding	Including DC-DC	Total Power including DC-DC losses [W]
Pixel(MuPix)					
layer 1	4	12	19.2	25.6	102
layer 2	4	15	24.0	32	128
layer 3	3 × 12	32, 36	51.2, 57.6	68.3, 76.8	2660
layer 4	3 × 14	36	57.6	76.8	3230
Fibre(MuTRiG)	12	8	9.6	12.8	153
Tile(MuTRiG)	14	13	15.6	20.8	291
Front-end board	8	14 boards	266	350	2800
Total					**9370**

Table 14.1: Power partitions for the Mu3e detector ASICs and electronics inside the magnet bore. The high-power elements on the front-end board are the Arria V FPGA, clock chip, and the transceivers. A respective maximum power consumption of 1.2 W and 1.6 W for the MuTRiG and MuPix chips is assumed. The upper limits on the power figures are driven by the cooling system, and depend on power losses in the entire power distribution system. For the total power budget, a 75% efficiency of the DC-DC converters is assumed.

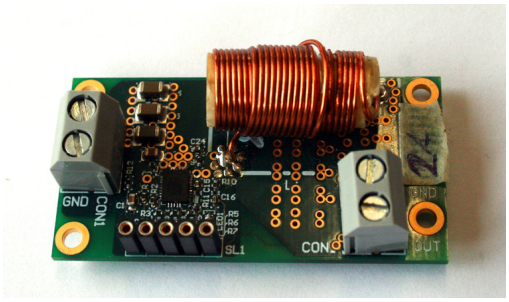

Figure 14.2: The second prototype for the buck converters for the frontend board. Good performance with efficiencies >75% in a 0.7 T magnetic field was demonstrated.

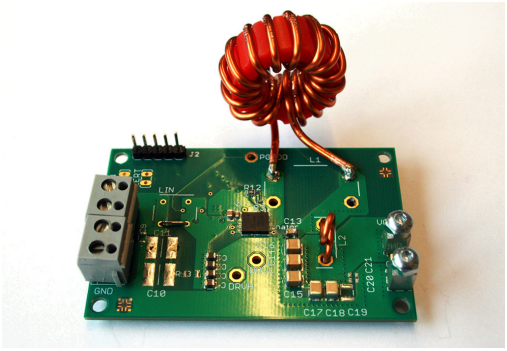

Figure 14.3: A 4.5 x 7 cm prototype for the power board, with a 0.5 µH toroidal inductor and a secondary LC filter at the output. With an output ripple of 10-20 mV, this has been used to succesfully power MuPix 8 sensors.

temperature interlock connected to a temperature diode on the MuPix sensor [77].

In the experiment, 16 power boards are mounted in a crate on the SSW (see Figures 14.1 and 13.4), with a MSCB slave (chapter 16) as controller. This controller adjusts the output voltage, switching frequency, and monitors several parameters. It also interfaces the DC-DC converters with an external interlock system.

14.3 Bias voltage

Bias voltages between 50 V and 120 V are required for the SiPMs used in the fibre tracker and the tile detector as well as for the MuPix chip. As only moderate currents of few µA per channel are needed, these voltages can be generated with a Cockroft-Walton chain. Converters supplying positive voltages have been developed and optimized in the context of the MEGII experiment. For Mu3e this design is carried over to a new board which will be mounted inside the magnet volume.

The pixel tracker requires a negative bias voltage of up to -100 V for each chip. For economic reasons, a set of four power groups is provided with a common voltage with dedicated current measurements and the possibility to turn off each power group individually. Since voltage generators which run at the high magnetic field are not available commercially, a custom board based on the Cockroft-Walton voltage multiplier design has been created. Figure 14.5 shows the simplified block schematic of this device. A micro-controller connected to the MSCB slow control system operates the DAC, ADC and switches of the voltage generator. It is capable of generating a bias voltage from $0 \ldots -150$ V out of a single power supply of 5 V. First tests with a prototype indicated that an absolute voltage accuracy of ±1 mV at a current of 2 mA can be achieved with a residual ripple below 10 mV. Each channel contains a shunt resistor and an ADC, which can measure the individual current. High voltage CMOS switches operated by the micro-controller can switch off individual channels in case the corresponding pixel chips would have a problem.

Figure 14.4 shows the top and bottom sides of a prototype of the high voltage board. It has a size of $30 \times 60\,\mathrm{mm}^2$. The Cockroft-Walton chain can be identified on the bottom side of the board. No magnetic components have been used

Component	Voltage [V]	Typical current [A]	Min. inductance air coil [µH]	coil design
Front-end board	1.1	2	2	cylindrical
Front-end board	1.8	1.7	6	cylindrical
Front-end board	3.3	2.2	4	cylindrical
MuPix partition (layer 1,2)	ca. 2.3	10	0.5	toroid
MuPix partition (layer 3,4)	ca. 2.3	21	0.4	toroid
Fibre partition	ca. 2.0	7	0.7	toroid
Tile partition	ca. 2.0	9	0.7	toroid
Tile partition	3.3	3	3.3	toroid

Table 14.2: Specifications for different buck converter channels stepping down the voltage from 20 V with an efficiency >70%. The quoted MuPix voltage takes into account an anticipated voltage drop of 200 to 300 mV between the converter and the chip.

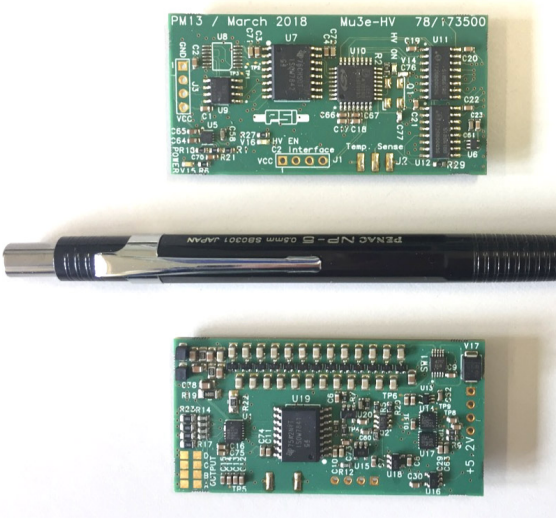

Figure 14.4: Prototype of the high-voltage generator board with top side (upper picture) and bottom side (lower picture).

in the design, making it possible to operate the board in magnetic fields of up to 2 T.

14.4 Cabling

The basic concept of the cabling inside the detector is shown in Figure 13.4. From the power boards, the connections to the detector components are carried out with minimal possible length using solid copper cable of 2.5 mm^2 gauge. Because all connections have to be done outside the detector acceptance, only the space around the beam pipes is left. Copper rods with a cross-section of $5 \times 2.5\,\text{mm}^2$ are used to bridge the connection between the detector endring mount and the outer end of the beam pipe. These rods are individually insulated using a polyimide foil wrap, and held in place by epoxy. The rods are in a densely packed environment, hence the dissipated power will be actively removed using a copper cooling ring (see section 12.1). The cables are connected using screw-mounted copper clamps.

Data cables between detectors and the front-end boards are micro-twisted pair wires: AWG 36 wires with a Polyimide isolation and an impedance of 90 Ω from *Heermann GmbH*. Each bundle of up to 50 pairs has a typical outer diameter of 2 mm. The bundles are arranged around the water cooling pipes: see Figure 14.6 for a sketch of the arrangement. The data cables are attached to the detector elements using soldered connections on flexible printed circuit boards, which connect to the PCB or HDI via interposers. The attachment to the frontend boards takes place on the patch panel of the SSW using zero-force connectors.

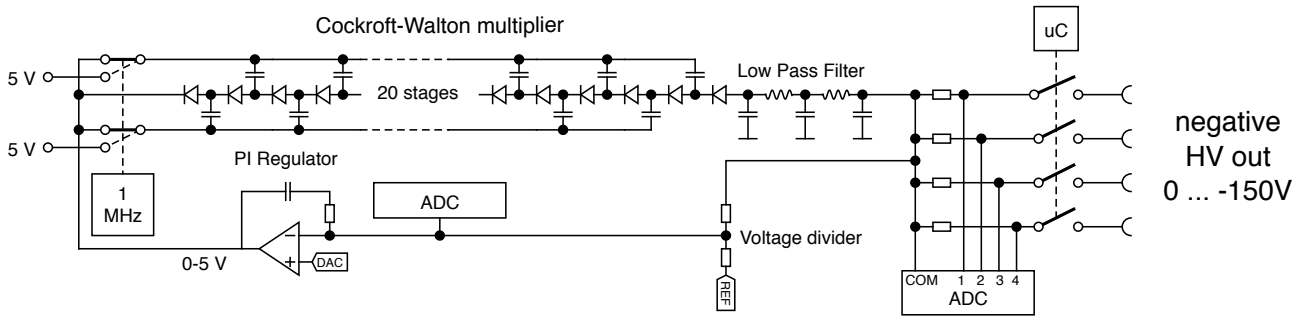

Figure 14.5: Block schematic of the pixel high voltage generation.

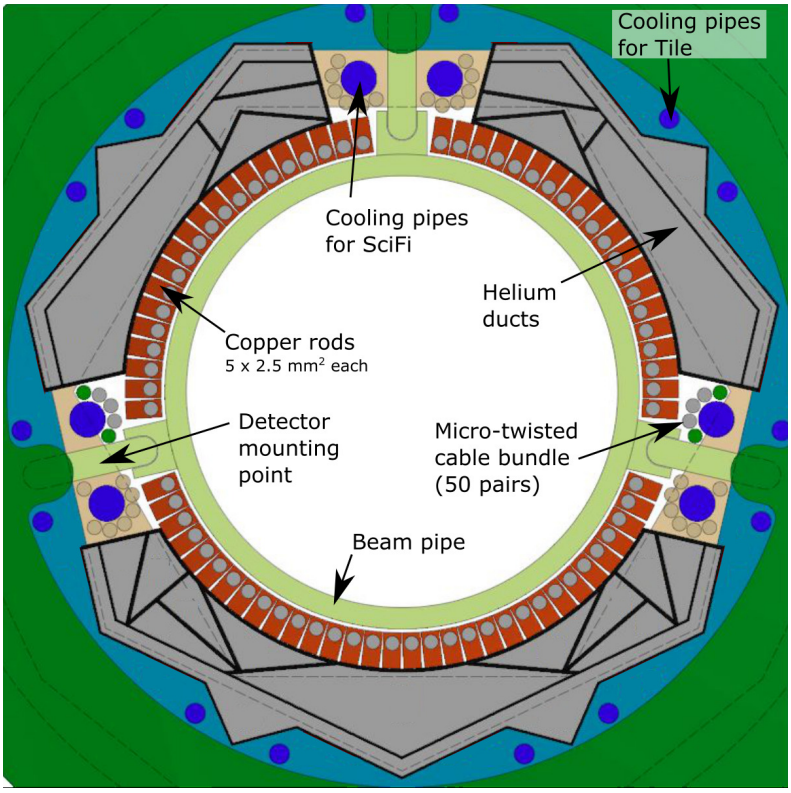

Figure 14.6: Cross section of a recurl station. The micro-twisted pair cables come in bundles and are shown as circles around the cooling pipes for the fibre detector (the colour code shows detector assignment: green for fibres, grey for vertex layers, brown for pixel outer layers. The helium ducts have separated channels for different destinations. Their cross sections are optimised for minimal pressure drop.