Fast Monolithic Pixel Detectors

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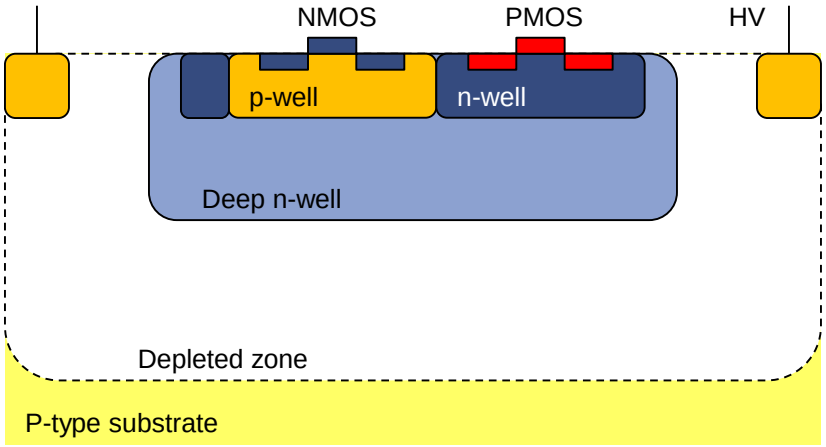
Fast CMOS Sensors - Motivation

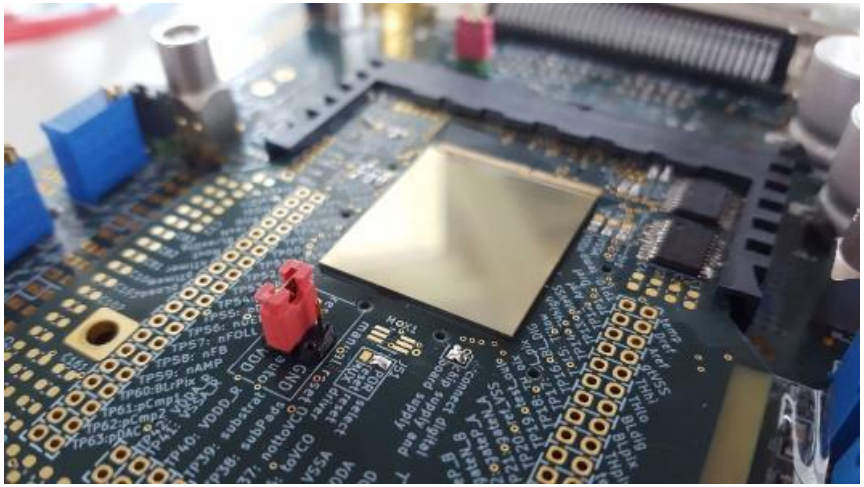
- The main challenge of a Mu3e Phase II is the increase of the hit occupancy in all detector systems.
- Most critical for the scintillating fiber detector (SciFi) which will essentially be blind due to pileup. SciFi time resolution of 500ps is not sufficient for fully resolving combinatorial background.
- => We propose to exploit a (1) timing silicon detector with ultra-fast resolution of 100 - 200ps.
- A further challenge is the increase of the number of hits in the pixel detector.
- Idea: shortening the size of the reconstruction frame is effective in fighting the combinatorial background.
- Requires time resolution of the pixel system of about 1ns.
- => Further optimize the (2) pixel detector design and to gain a factor 4-5 in the time resolution.

- High voltage CMOS monolithic active sensors (HV-MAPS) are a novel type of CMOS active pixel sensors, optimized for detection and tracking of ionizing particles that can be implemented in the CMOS processes. The pixel contains one sensor electrode formed with a deep n-well implanted in p-type substrate.
- CMOS pixel electronics are placed inside the deep n-well.
- By biasing the substrate with a high negative voltage and by the use of a lowly doped substrate, a depleted region depth of typically 30µm can be achieved. The electrons generated by a particle are collected by drift.
- Signal charge collection is fast because of short drift path and high drift speed.
- Time resolution is usually limited by rise time of the amplifier and signal fluctuations (time walk effect).
- => High time resolution can be achieved with fast amplifiers.
- Fast amplifiers require large bias current, leading to large power consumption.
- Idea:
- Use most efficient amplifier input device which provides maximum gain and minimum noise for given bias current.



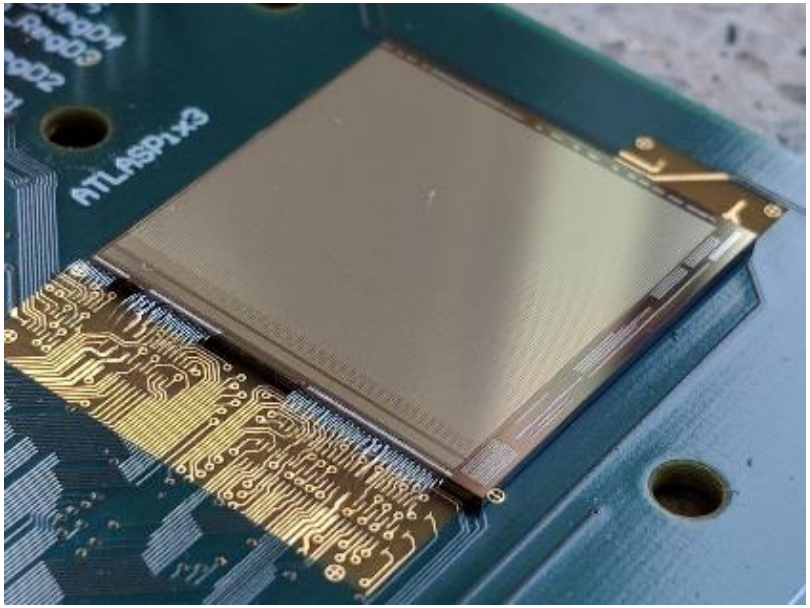
Existing Sensors

- MuPix10 is the first reticle-sized sensor produced at TSI and fulfills all specification requirements of the Mu3e experiment.
- It contains 256 x 250 pixels of 80µm x 80µm size. The chip area is 20.66mm x 23.18mm.
- The main chip part is organised in 128 double-columns. One double-column consists of 500 pixels (two columns) and 500 hit digitizers with attached end-of-column multiplexer.
- The chip periphery also contains the readout control unit, the clock generator based on a phase-locked loop, configuration registers, digital-to-analog converters and IO pads.



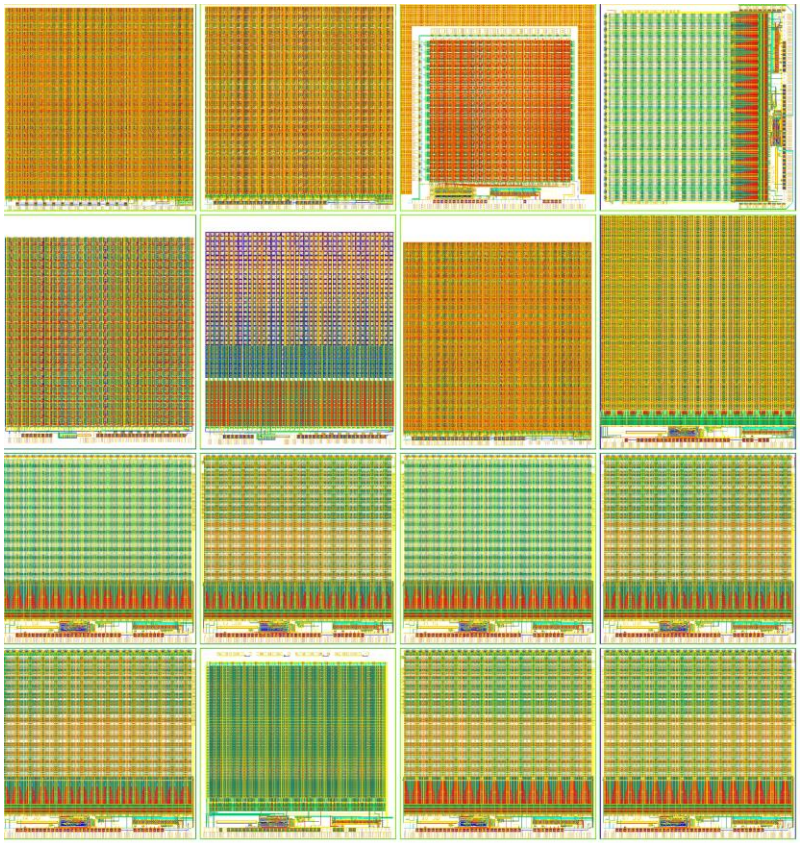
- [1] H. Augustin et al., "The MuPix sensor for the Mu3e experiment," Nucl. Inst. Meth. A 979 (2020)

- ATLASPix3 is a reticle-sized HV-CMOS sensor designed for ATLAS. The sensor has been produced by TSI within an engineering run on high resistivity substrates. Detection efficiencies of >99.5% have been measured in beam (DESY and PSI).
- The time resolution after time-walk and binning corrections is ~4.5ns sigma. The production yield is about 85% and the power consumption is of the order of 120mW/cm^2.
- Simulated time walk is ~15ns for signals from 2ke to 20ke and input referred threshold of about 1ke.

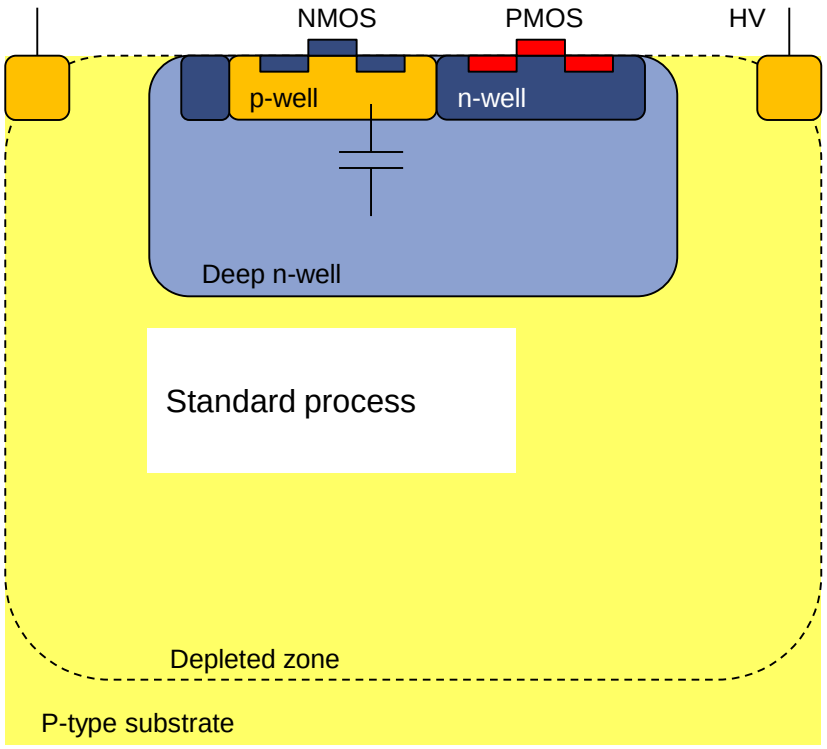


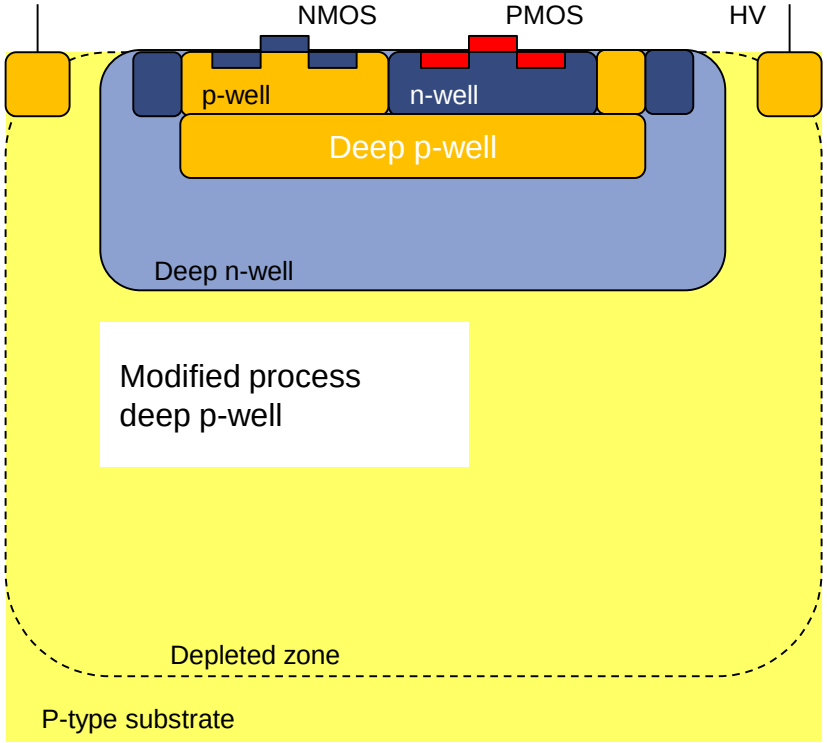
- [2] ATLASPIX3 from I. Peric, et al, IEEE JSSC, 2021, DOI: 10.1109/JSSC.2021.3061760

- Recently, we have designed test chips to study various circuits in a systematic approach.
- We implemented different types of amplifiers, techniques to reduce detector capacitances by reverse biasing of in-pixel implants, different pixel geometries with guard ring variants for higher breakdown voltages, different types of comparators, a novel current-based differential signal transmission and a time to digital converter (TDC) based on time stretching with 100p resolution.
- A design with an additional deep p-well implant was produced that is used to better isolate the comparator from the deep n-well.

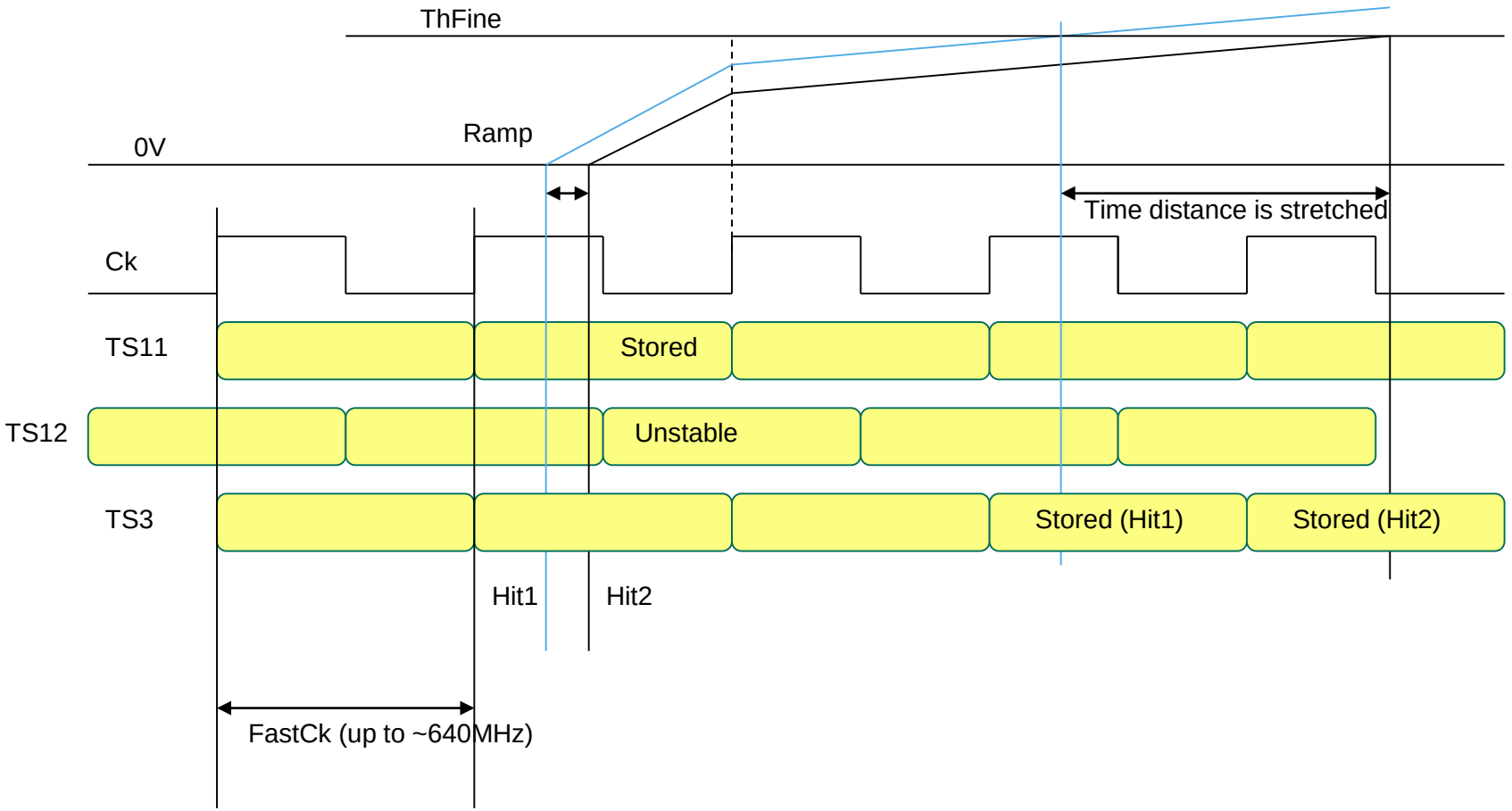


- Modified process

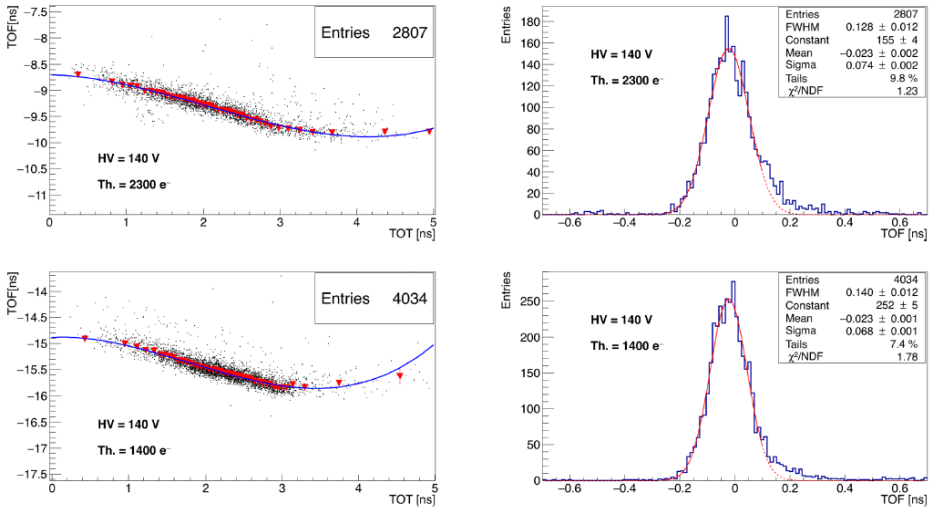




- Time to digital converter (TDC)



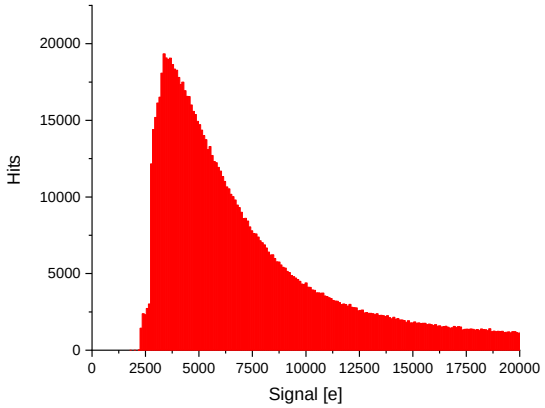
- We collaborate with the University of Geneva on the development of HVMAPS sensors in SiGe BiCMOS technology SG13 from IHP in Frankfurt (Oder).
- The technologies SG13S/G2 allow production of SiGe heterojunction bipolar transistors (HBTs) and CMOS transistors on the same substrate.
- HBTs are superior in comparison to CMOS transistors because they offer much higher gain over capacitance ratio, called transition frequency than the CMOS transistors.
- => Fast amplifiers with small time walk can be implemented
- Recent results [3] demonstrate that time resolutions below 100ps (RMS) are possible with particle sensors implemented in the IHP process.

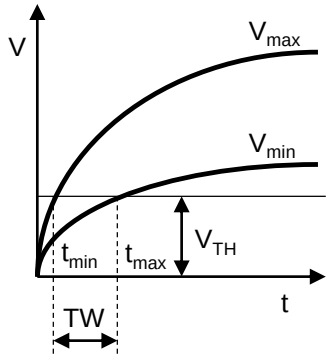


[3] G. Iacobucci et al., „A 50 ps resolution monolithic active pixel sensor without internal gain in SiGe BiCMOS technology“, JINST 14 P11008 (2019)

Planned Sensors with high time Resolution

- The time resolution is mostly limited by the time walk that results from fluctuations of the input charge signal
- TW = T_r Q_{th}/Q_{min}.(T_r is the amplifier signal rise rime, Q_{th} is the input referred threshold and Q_{min} the minimum signal)
- Rise time depends on voltage gain A (for CSA C_i/C_f), capacitance C_o and transconductance g_m
- $T_r = A/(C_o\, g_m)$



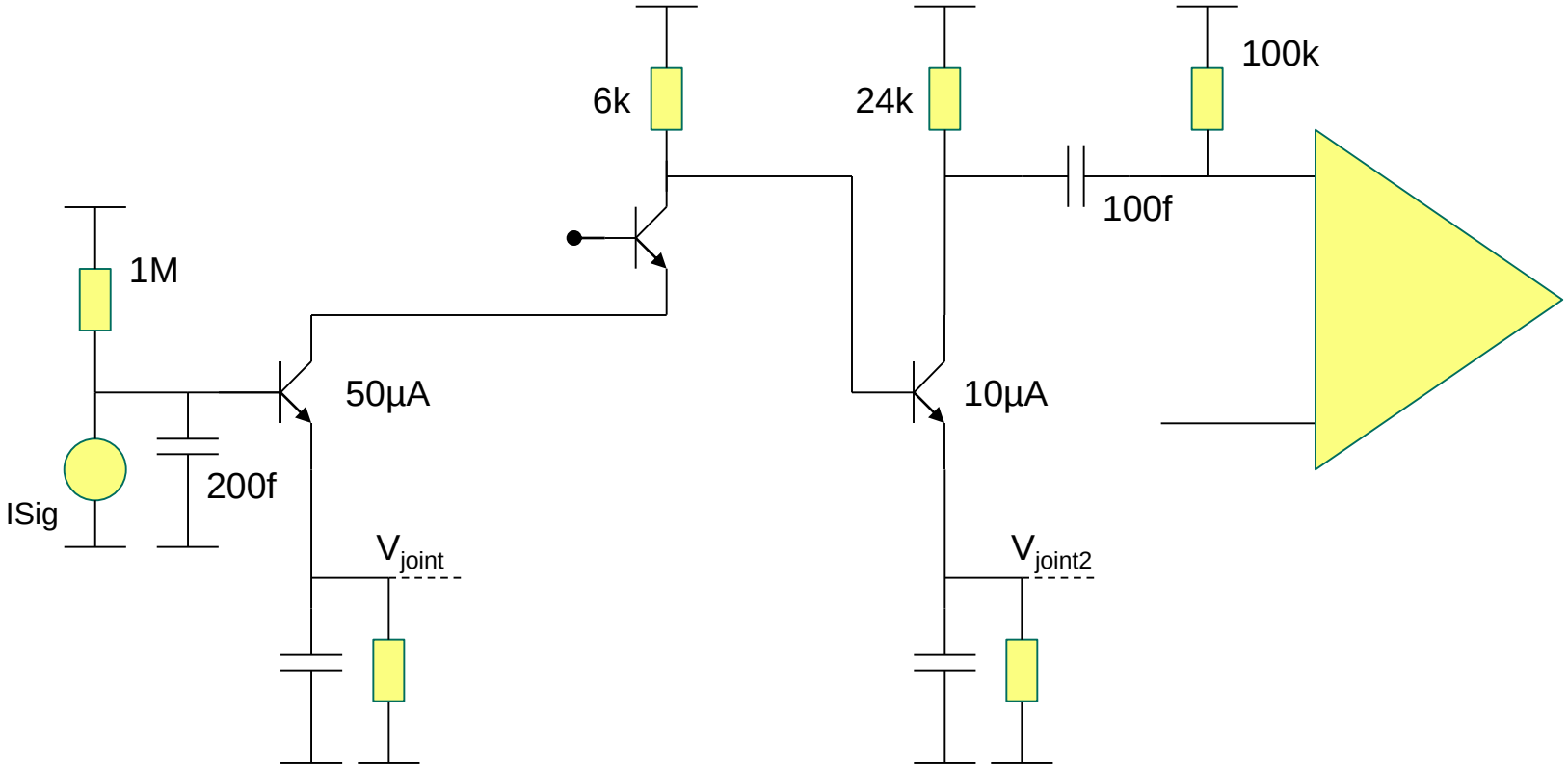


- We plan to enhance the time resolution by employing the following measures:
- 1. Employing of cascaded amplifiers and current-mode signalling
  - The rise time can be shortened when the voltage gain A is reduced.
  - We can replace one amplifier with gain A with two cascaded amplifier stages, each with smaller gain, without reducing the overall gain.
  - Such a cascade would have a by factor $A^{1/2}$ reduced time constant, and thus a better time resolution.
- 2. Precise amplitude measurement time walk correction
  - One approach for improving the ToT measurement is to split the signal path after the amplifier. One path will be used to measure the signal arrival time. The other path will use a low pass filter for noise reduction. By measuring the ToT with the filtered signal, the amplitude will be reconstructed with a smaller error.
- 3. Reduction of detector capacitance
  - In present HV-MAPS, a large fraction of the input capacitance is caused by the capacitance between the deep n-well and the metal shield. The metal shield can be reduced by optimising the layout of the metal layer.
- 4. Increase of the bias voltage
  - Bias voltage of 200V is possible if the guard ring is optimally designed. In the case of mupix10, the breakdown voltage is about 100V. There is potential for further improvements.
- We believe that a time resolution of 1ns (RMS - after corrections) can be reached with these improvements.

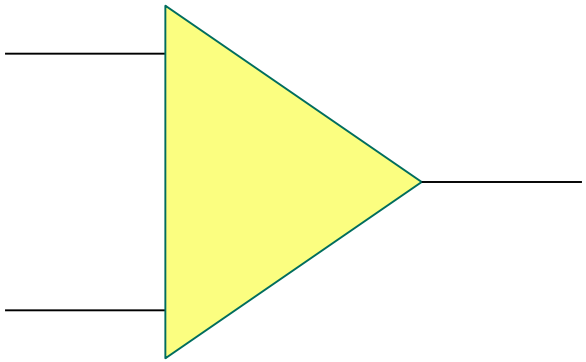
- The goal is to develop a timing monolithic sensor (called PicoPix) which can be used to build an ultra-thin detector with a time resolution of the order of 100ps and covering an instrumented area of about 2000cm^2
- Presently, we achieve with ATLASPix3 a time resolution of about 7.5ns before time walk correction and 4.5ns after time walk- and binning corrections.
- The goal is to improve the time resolution by more than one order of magnitude. We believe that this is possible based on the following considerations:
- The pixels of the PicoPix sensor can be large, at least 20 times larger in area than in the case of the MuPix10 or ATLASpix3.
- In MuPix10, only a small fraction of the input capacitance originates from the deep n-well to p-substrate junction. Much larger fractions of the input capacitance arise from the transistors placed inside the deep n-well and the parasitic capacitances from the deep n-well to the metal shield used to protect the n-well from the signals routed above. These contributions do not scale with the pixel area. A pixel with 20 times larger area can have roughly the same capacitance if the capacitances from the transistors and the shield are reduced; that is feasible with a simplified amplifier structure and optimised shield layout.
- => The bias current of the amplifier can also be 20 times larger without increasing the power budget.
- Increasing the bias current leads to an increase of the transconductance.
- 20x increase of g_m will lead to a 20x reduction of time walk, if the input capacitance is unchanged.

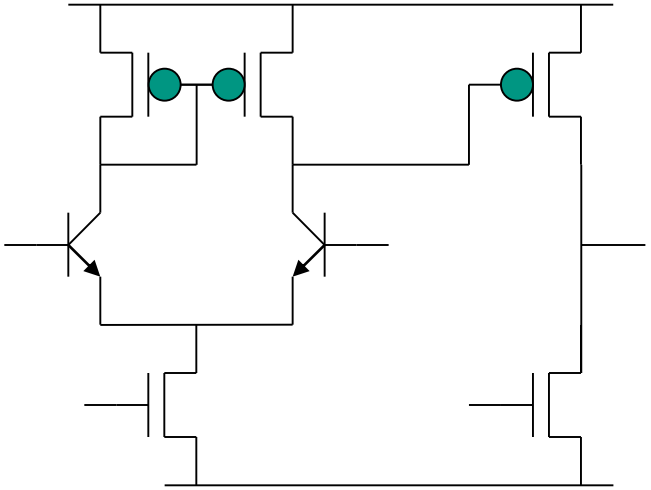
- A higher bias current opens further possibilities in the amplifier design.
- The charge sensitive amplifier can be replaced with a simplified voltage amplifier.
- A simpler structure with fewer transistors leads to a smaller input capacitance and improves the response time.
- The idea is to use a cascade of low gain amplifiers without feedback instead of one high gain amplfier with capacitive feedback. The advantage of low gain amplifiers is that they can be produced without PMOS transistors, using a single BJT or NMOS. This reduces detector capacitance. Simulations show significant improvement of time resolution. Simulated time jitter (the lowest limit of time resolution) is of the order of 100ps.
- The idea can be implemented in HVCMOS or in BiCMOS technology.

- PicoPix1 will be implemented in IHP SG13G2 technology
- Two stage amplifier

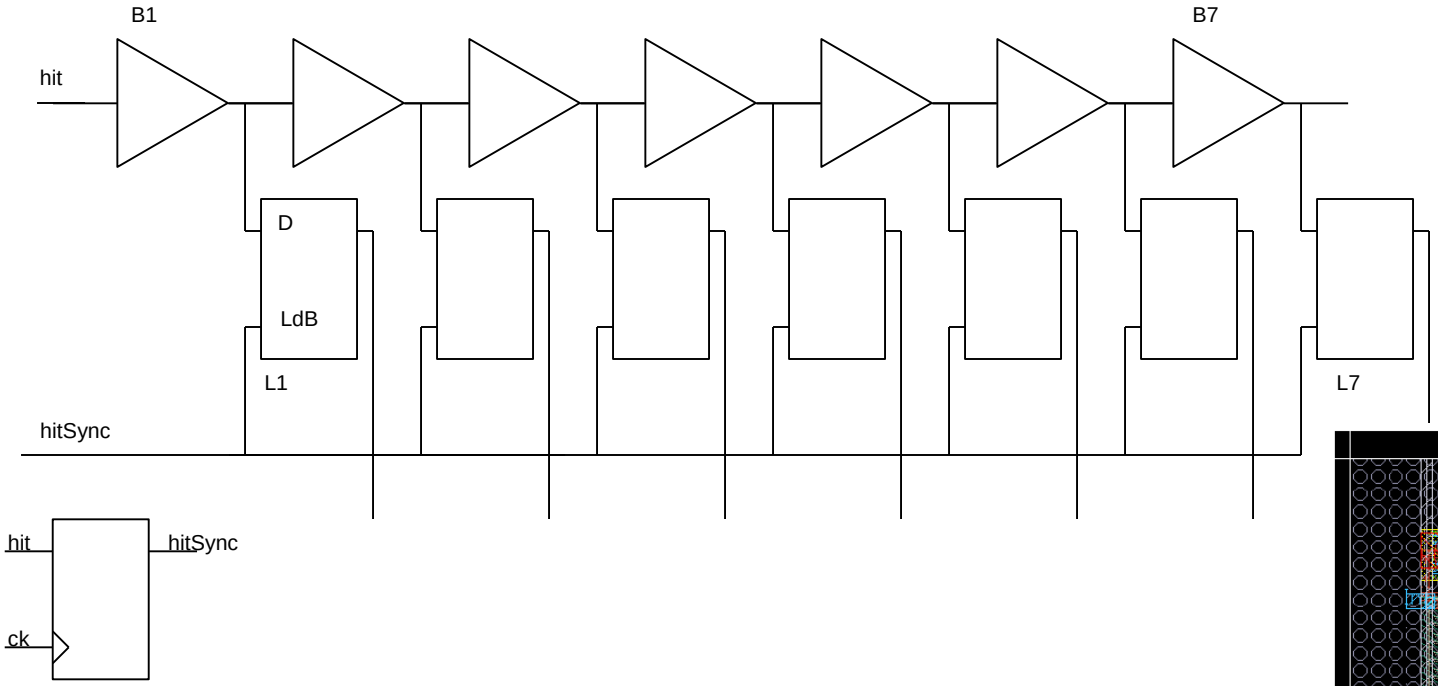


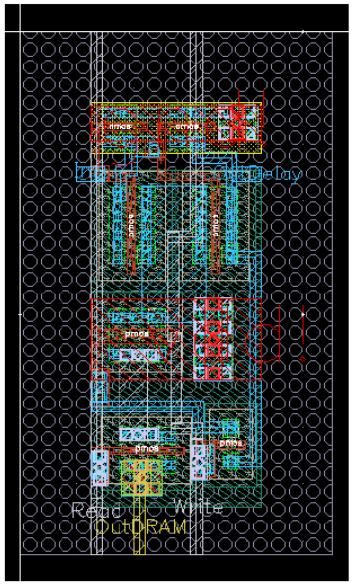
- Comparator



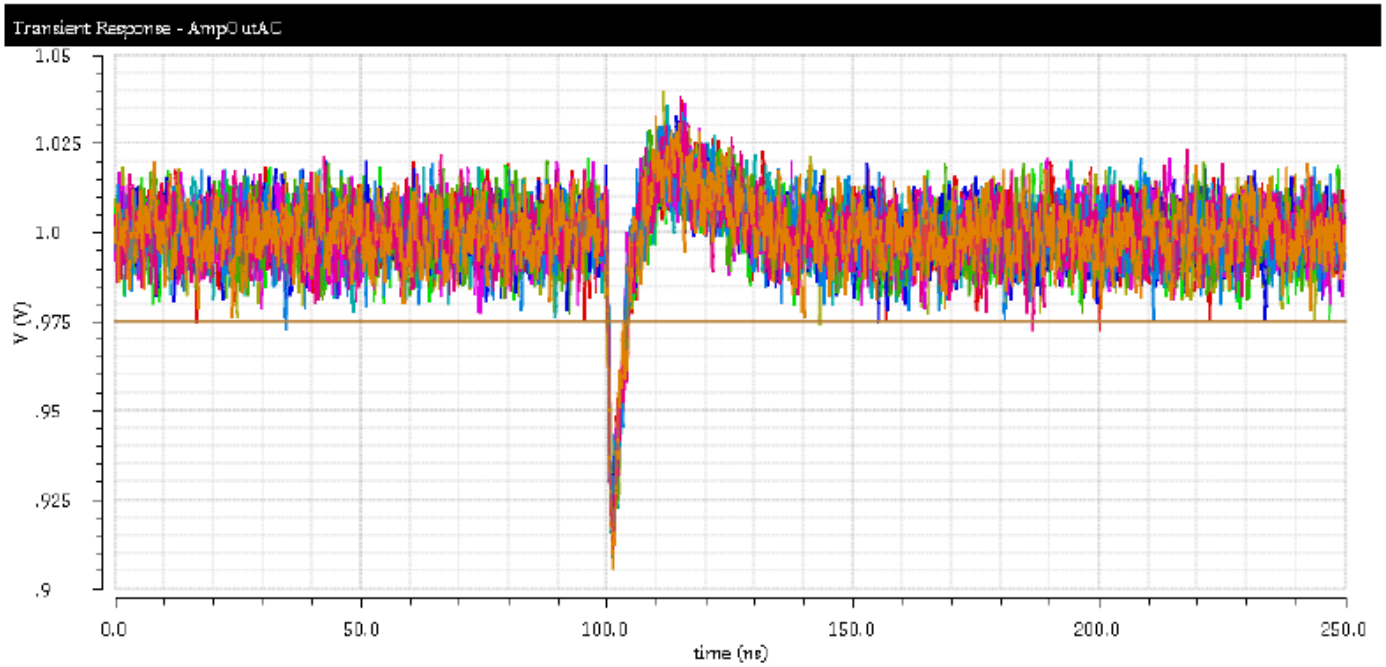


- Time to digital converter

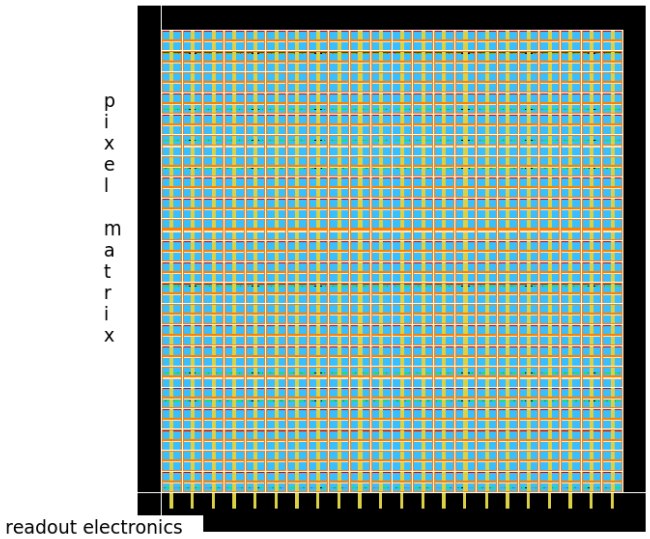


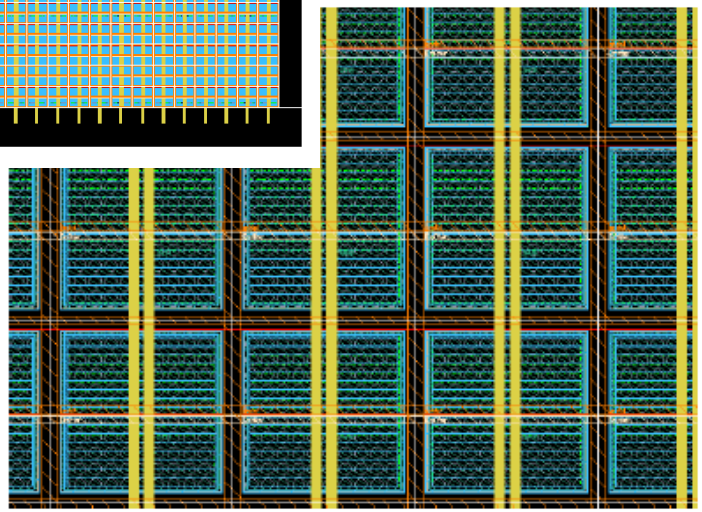


- C_{det} = 200fF
- Q_{signal} = 0.25fC
- v_{signal} = 84.36mV
- ENC = 126e
- Tr = 1.21ns
- Time jitter after comparator ~70ps
- TW after comparator for signals 0.25fC – 2.5fC ~ 700ps and threshold ~ 6 x noise
- Results 20x better than for ATLASPix3 design

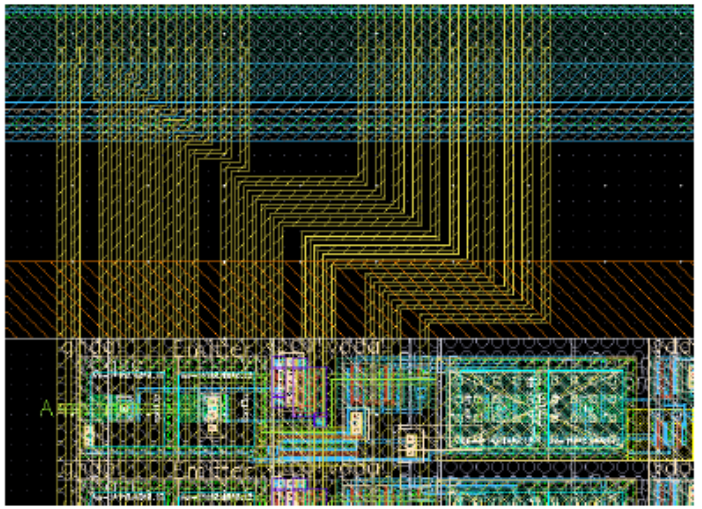


Pixel matrix

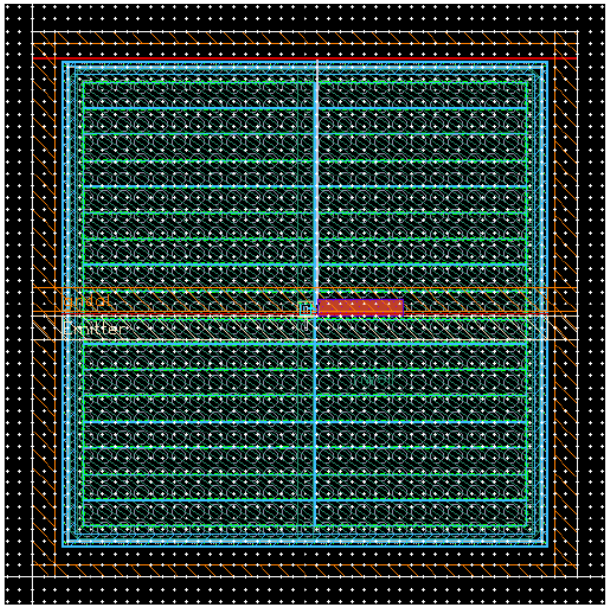




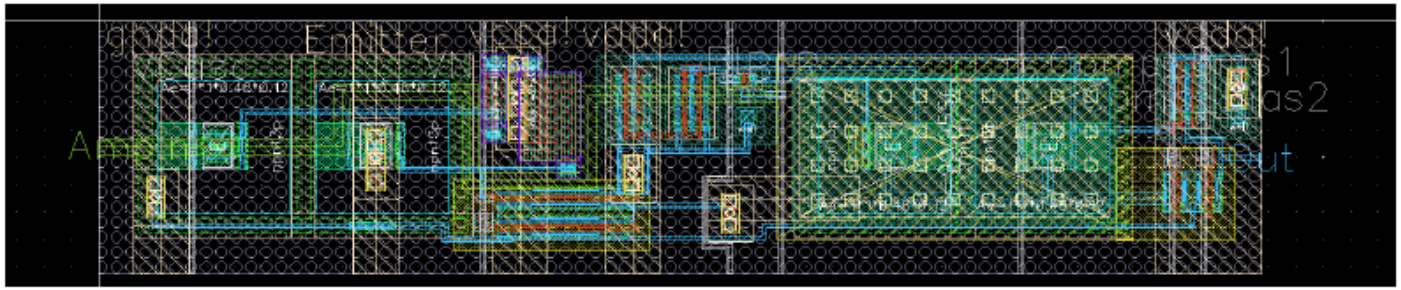
Pixel matrix



Second amplifier stage and comparator



Pixel



Second amplifier stage and comparator

Summary

- The main challenge of a Mu3e Phase II is the increase of the hit occupancy in all detector systems.
- One solution: fast monolithic CMOS sensors.
- Several large HVCMOS/HVMAPS sensors are available, among them MuPix10 designed for Mu3e.
- We believe that the time resolution of pixel sensors with 80µm x 80µm can be improved to 1ns (RMS).
- In the case of larger pixels (> 250µm x 250µm), time resolution of 100ps (RMS) seems possible. This will lead to the timing HVMAPS detector.
- We have already started the developments of fast HVMAPS sensors in TSI 180nm HVCMOS and IHP 130nm SiGe BiCMOS processes. Submission of the first test chip is planned for summer 2021.