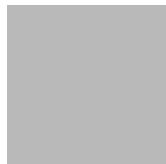


PAUL SCHERRER INSTITUT



Babak Kalantari :: Electronics/AEK :: Paul Scherrer Institut :: GFA-PSD seminar
26.04.2021

AEK Hardware Toolbox for upcoming projects Status & Roadmap





Strategy for future Electronics (aka NPP strategy)

- New projects are coming up: **SLS 2.0, Porthos, HIPA upgrade, ...**
- VMEbus is not compatetive anymore, **issues:** performance, functionality, availabilitiy
- Today's demand: handling more data -> faster processing, higher bandwidth
- Tremendous advances in electronics and computer technology in the past 20 years

- **EINet-GERTS** worked out the strategy, approved in 2018 by ElGo:

Two-pillar development lines:

- standard **CompactPCI-Serial** (CPCI-S) for modular systems

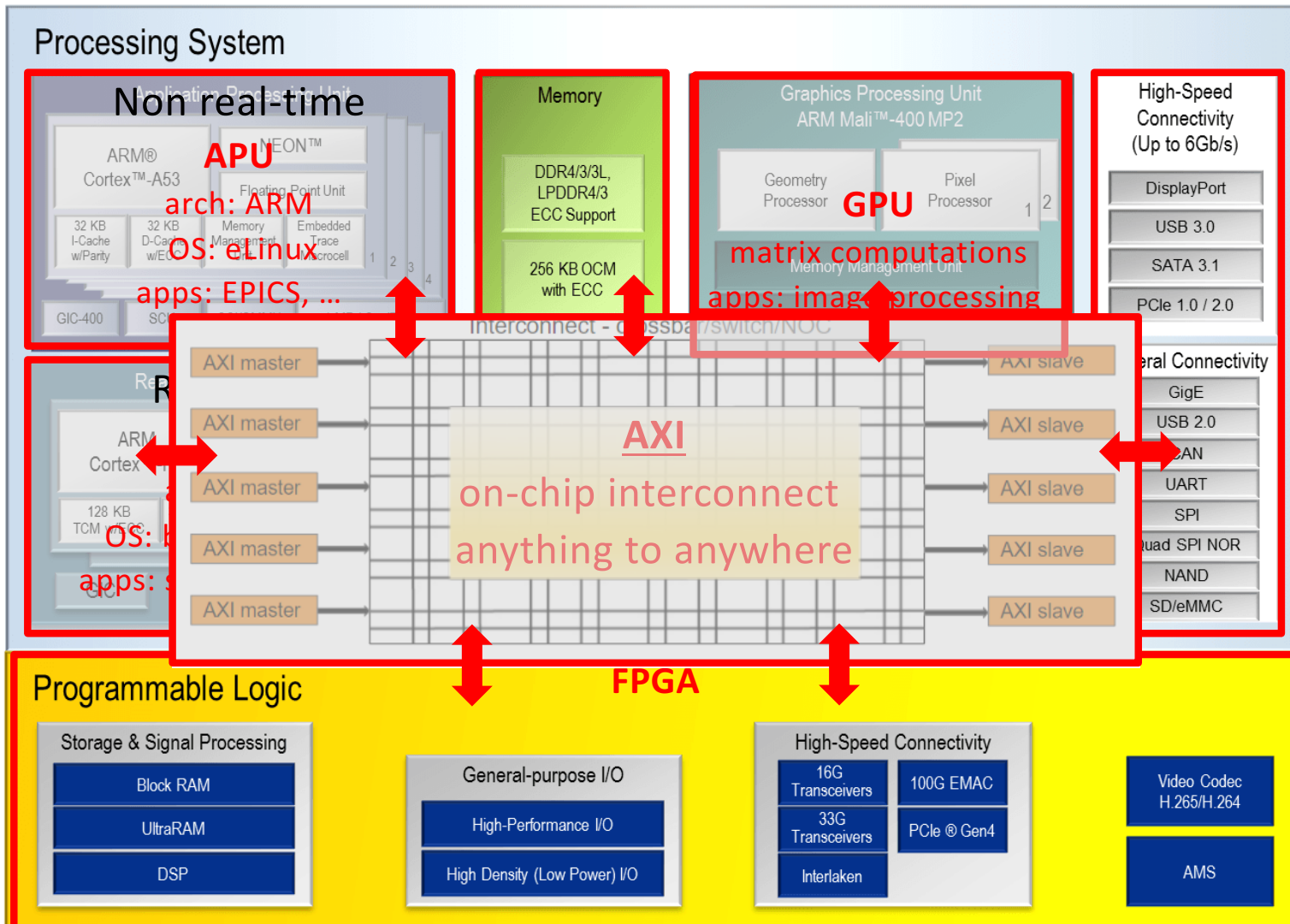
Zynq UltraScale+

common, embedded processing architecture

- application specific (optimized) embedded systems

CPCI-S bus standard recommendation was made by expert workgroup of EINet-GERST and was approved as strategy for future electronics by ElGo. Study document: <http://i.psi.ch/sCP84>

Zynq UltraScale+ MPSoC common architecture



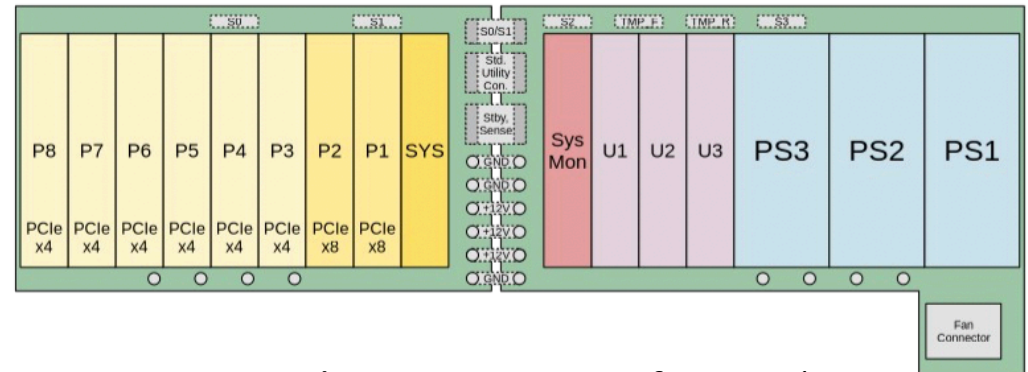
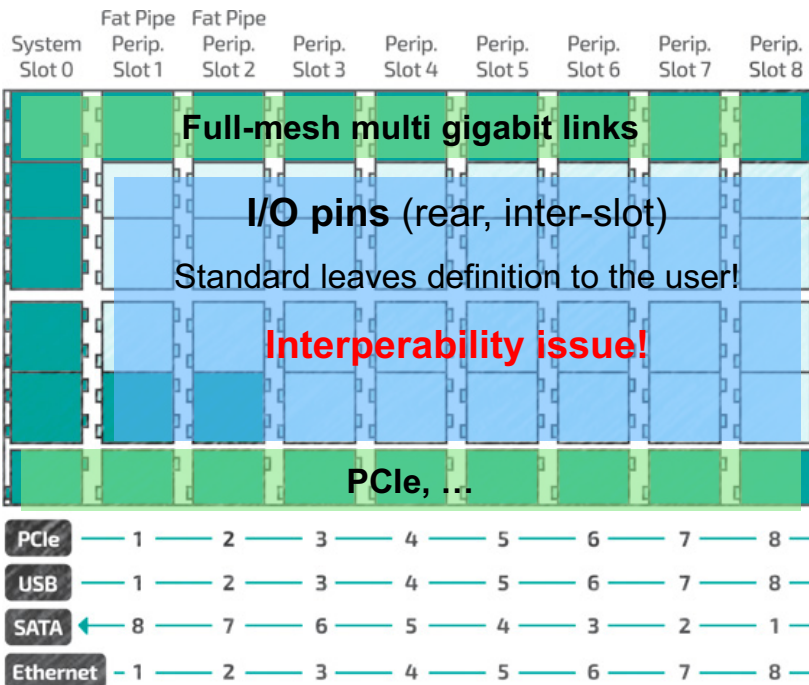
CPCI-S standard and CPSI-S recommendation



CPSI-S is a recommendation by PSI for definition of the user I/O pins.

This recommendation defines signaling and/or function of each user I/O pin to address interoperability issue. This allows PSI engineers to independently develop interoperatable cards, therefore eases effective collaboration among PSI divisions. Currently two FPGA cards are in parallel under development in GFA & NUM.

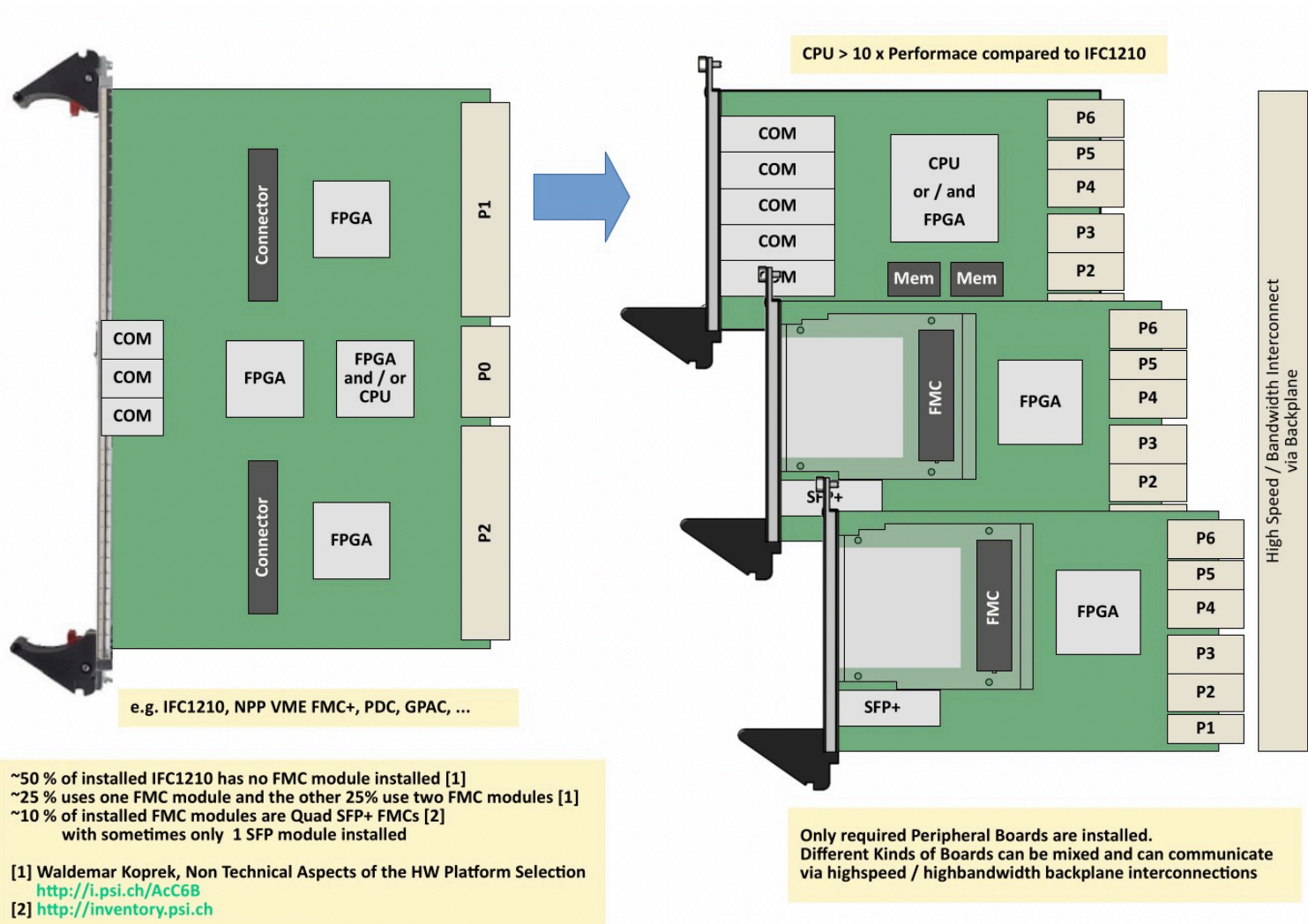
Through activities coordinated via EInet-GERTS, CPSI-S recommendation has found its way to PICMG® and is seriously being considered to go into the next revision of the worldwide standard CPCI-S.0 R2.0.



- Minimal pin assignment for RTM's
- Universal FPGA Board Pinout
- System Monitor Pinout
- See more details on CPSI-S: <http://i.psi.ch/Ri1NB>

• CompactPCI Serial is particularly well suited for high speed (12 Gbps) / high bandwidth data communication applications. App areas include robotics, machine control, industrial automation, telecommunications, medical equipment, energy sector applications, and ground transportation, avionics and shipbuilding.

CPCI-S: changing to 3U form-factor more modular, more Flexible!



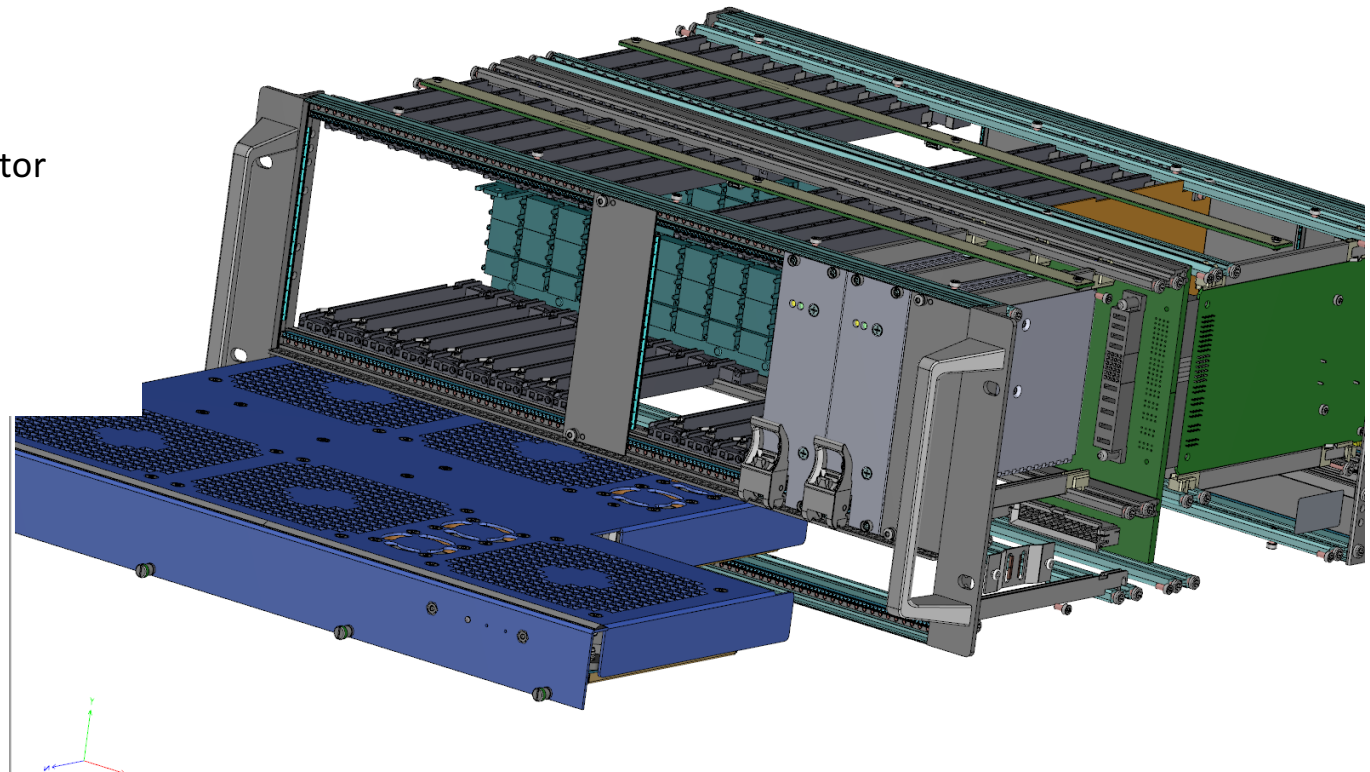


CPCI-S Toolbox

- Number of improvements on COTS crates were required
- Contractor for improvement of COTS crate is Elma



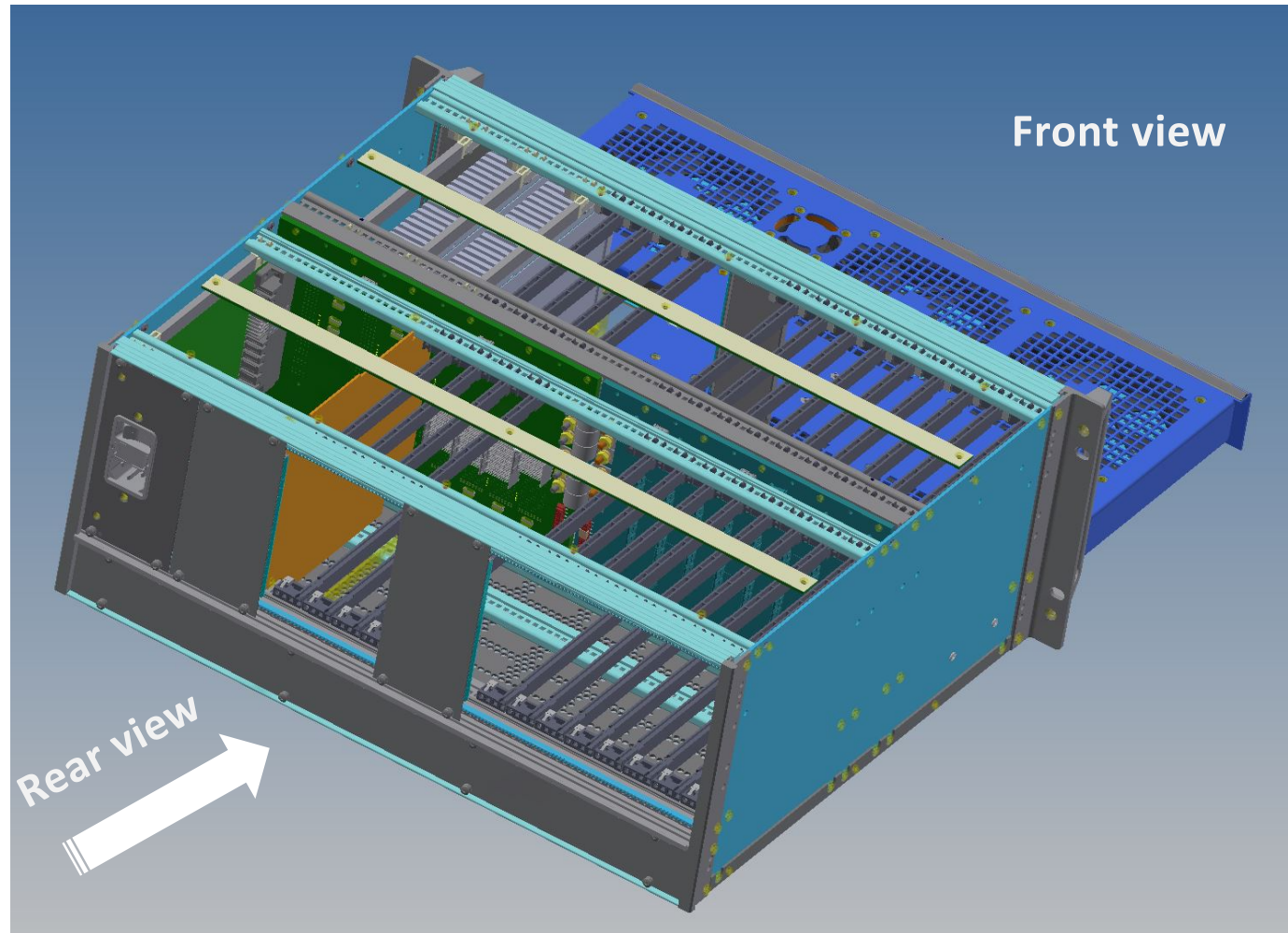
- ✓ Scalable power supply: up to 3x PSU
- ✓ Optimized cooling
- ✓ Easier maintenance
- ✓ Front/Rear temperature monitor
- ✓ Noise reduction
- ✓ Separate power backplane
- ✓ Rear length extension



Status CPCI-S Crate

- Current state: mechanical/electrical review ongoing,
- prototype delivery: Q3/2021
- Contact: S. Schnabel

- ✓ Extended rear size (160 mm)
- ✓ System monitor & control
- ✓ Modular SysMon card
- ✓ 3x utility slots
- ✓ 1x SysMon slot
- ✓ Individual board On/Off

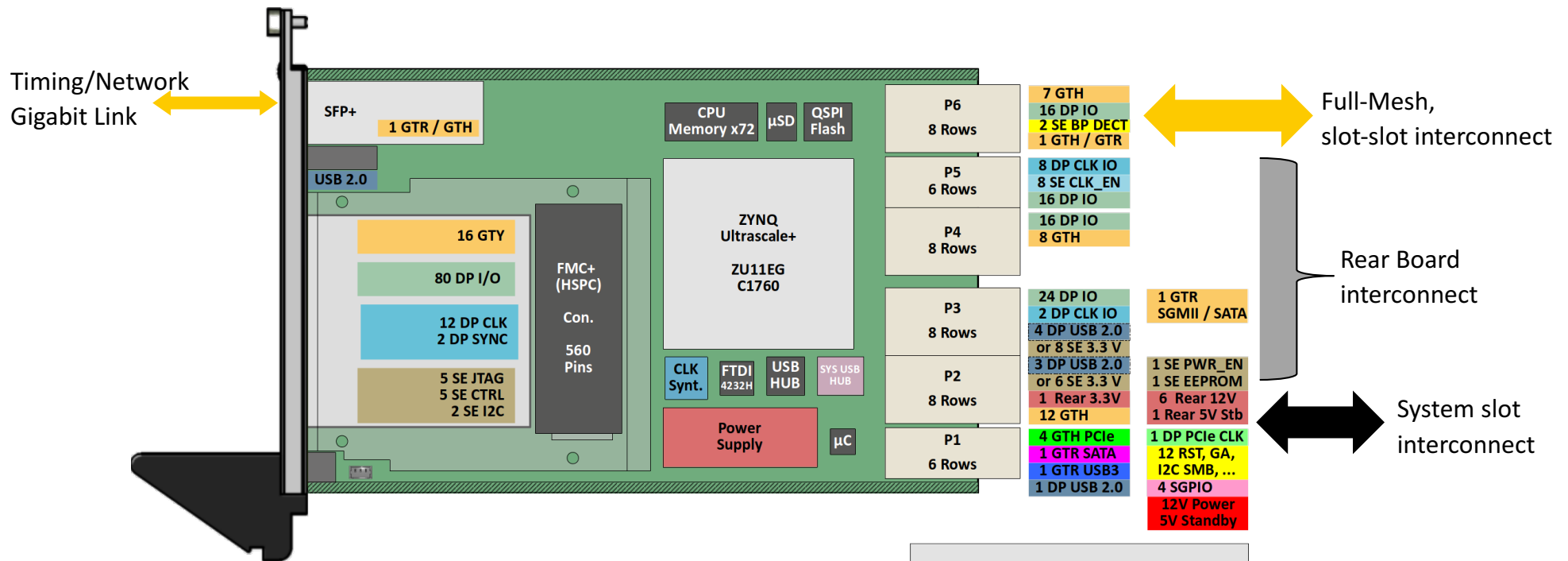


CPCI-S FMC+ Carrier (CPSI_UFC)



CiBOARD

- Mixed intern-extern development; ext. partner: CiBoard in Germany
- Project lead in GFA (Electronics)
- project team: GFA + NUM (HW/FW/SW experts) -> coordination EInet-GERTS

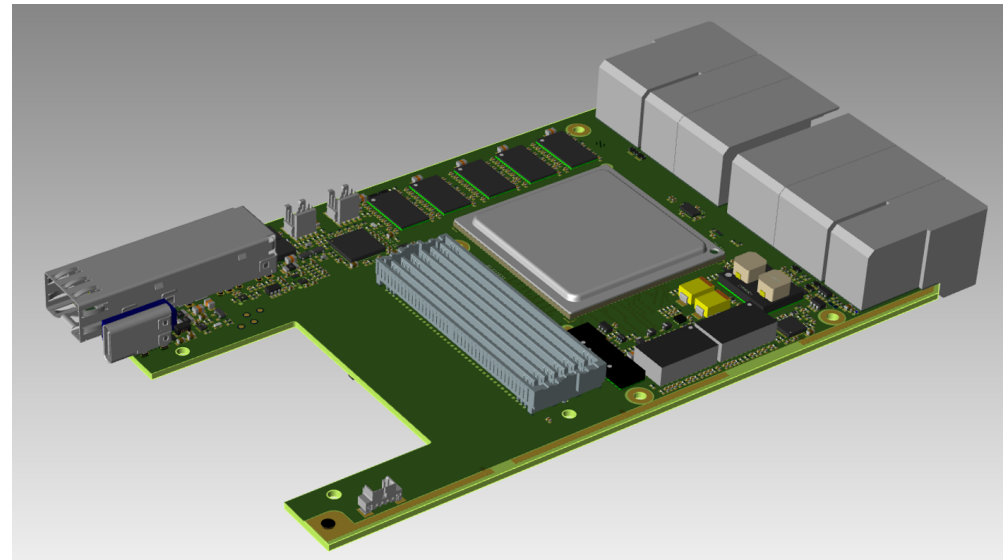
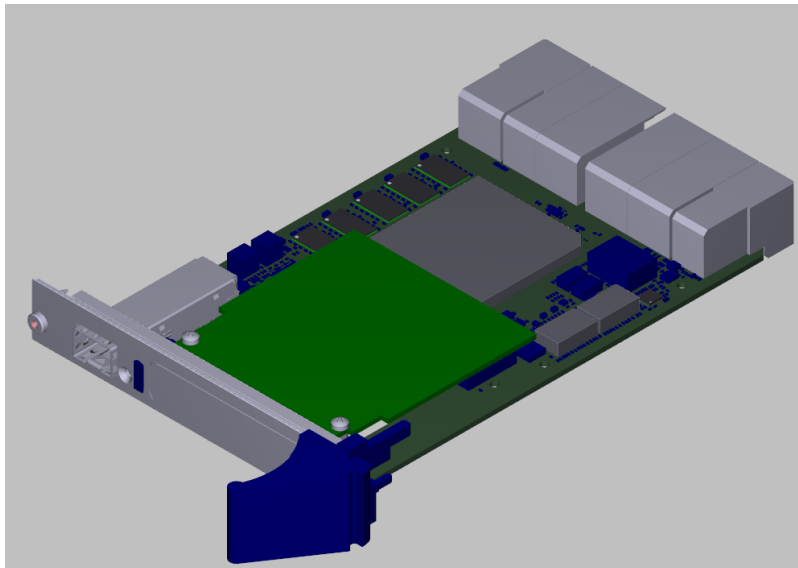


GBT: GigaBit Transceiver
 DP : Differential Pair
 SE : Single Ended

ZU11EG Speed Grade -1 / VCC_{INT} 0.85 V
 GTR : GBT with 6.0 Gb/s (4 - PS)
 GTH : GBT with 12.5 Gb/s (32 - PL)
 GTY : GBT with 25.78 Gb/s (16 - PL)

CPCI-S FMC+ Carrier (CPSI_UFC)

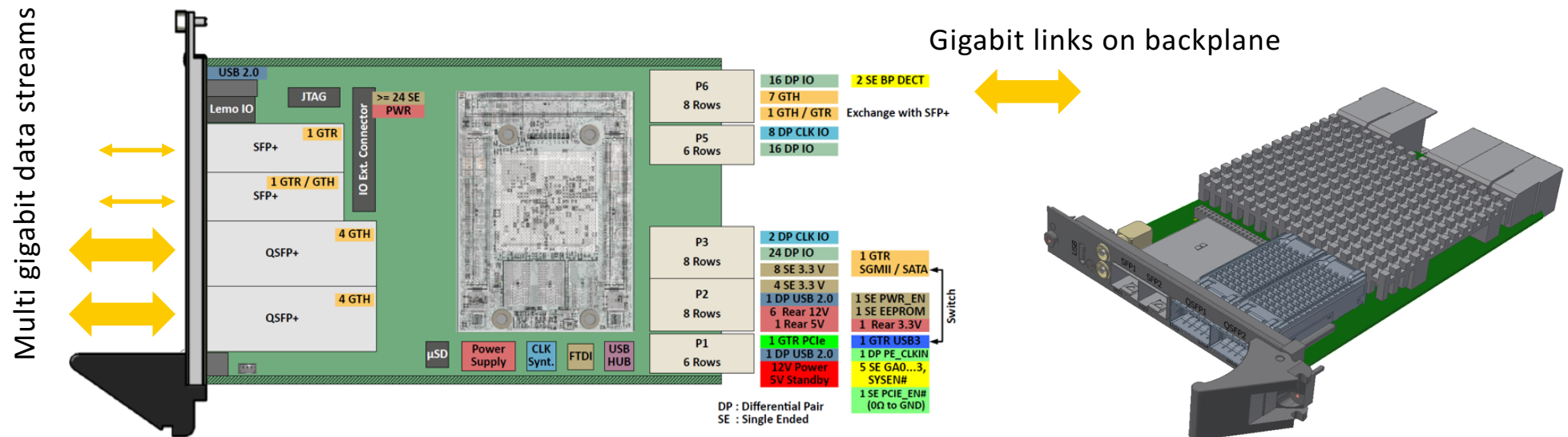
- High-end carrier with a high performance, large Zynq US+ MPSoC (ZU11EG)
- Application: LLRF, high-end DAQ & control (e.g. scope recorder, fill pattern readout)
- State: schema completed; layout being finalized at CiBoard,
- Test framework and infrastructure is being worked out by project team
- Prototype delivery to PSI: Q3/2021
- Contact: E. Johansen



CPCI-S COM-IO Board (CPSI_CIO)

➤ Development will be done fully at PSI

- Uses commercial Enclustra SoM with Zynq US+ arch
- Project lead for hardware development in NUM
- project team: GFA + NUM (HW/FW/SW experts) -> coordination EInet-GERTS
- GFA apps: Event timing, stream processing; NUM apps: DAQ for SINQ instruments
- Schema review completed! prototypes expected Q3 2021
- Contact: G. Theidel



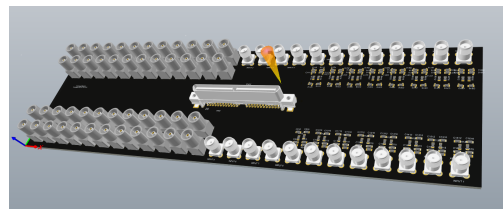
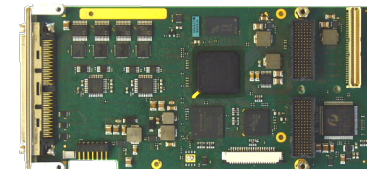
➤ In AEK Portfolio (10x pcs in stock):

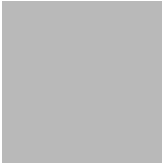
- CPCI-S Intel CPU card from EKF
 - Xeon(R) 3.00GHz, Quad core, 16 GB RAM
 - Details -> <https://www.ekf.de/s/sc5/sc5.html>
 - Apps: general control system, specially CPU/memory intensive applications



- TXMC635 multi-channel multi I/O (XMC module)

- 32x ADC 8x DAC, (16-bits), up to 1 MHz,
- 48x digital i/o up to 62 MHz
- Customizable logic (reconfigurable FPGA)
- Scope app FW/SW available! (incl. streaming to CPU memory)
- Terminal box prototype to be revised!
- Detail -> <http://www.tews.com/Products/ArticleGroup/TXMC/TXMC635.html>

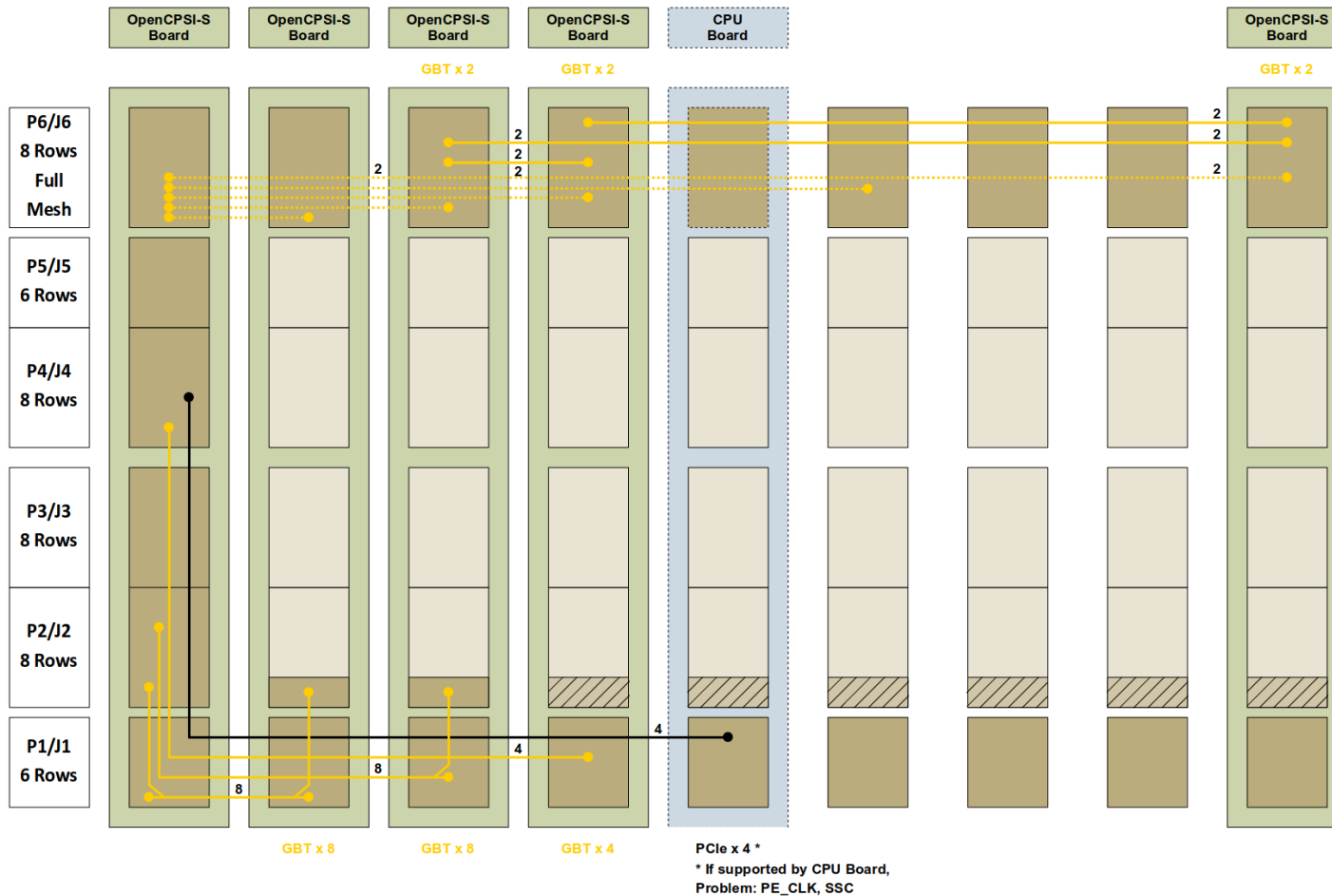


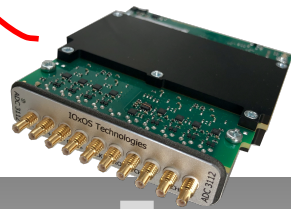
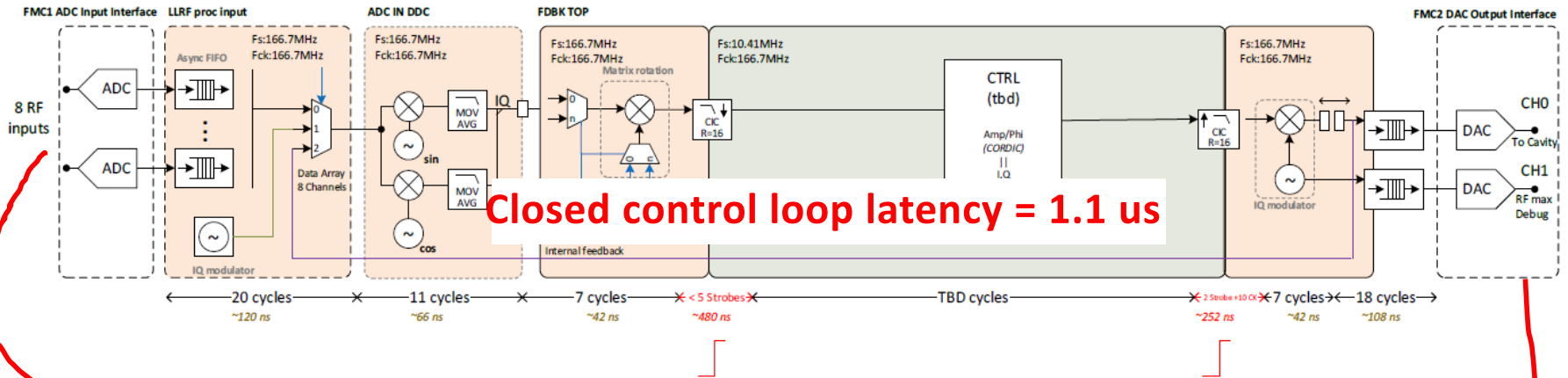


System implementations with CPCI-S tools

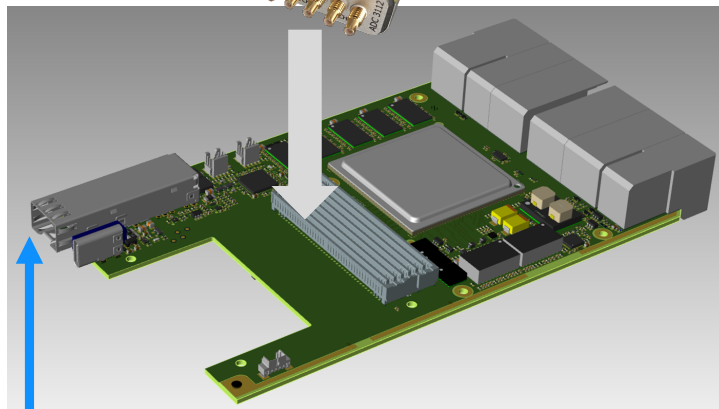
CPU-Centric System with FPGA Boards

High Bandwidth Connection between OpenCPSI-S Boards with COTS Backplane





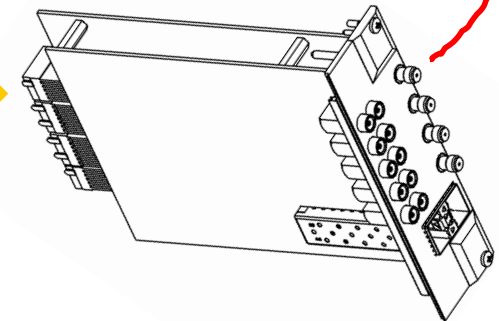
8x ADC @250 MSPS
(FMC Module)



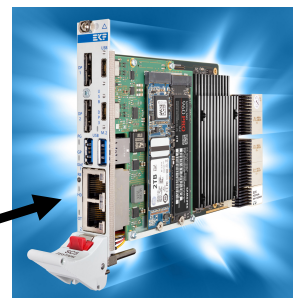
CPSI_UFC
(FMC+ carrier)



PCI-S backplane



CPSI_RTM_DAC
2x DAC @500 MSPS
(Rear Transition Module)



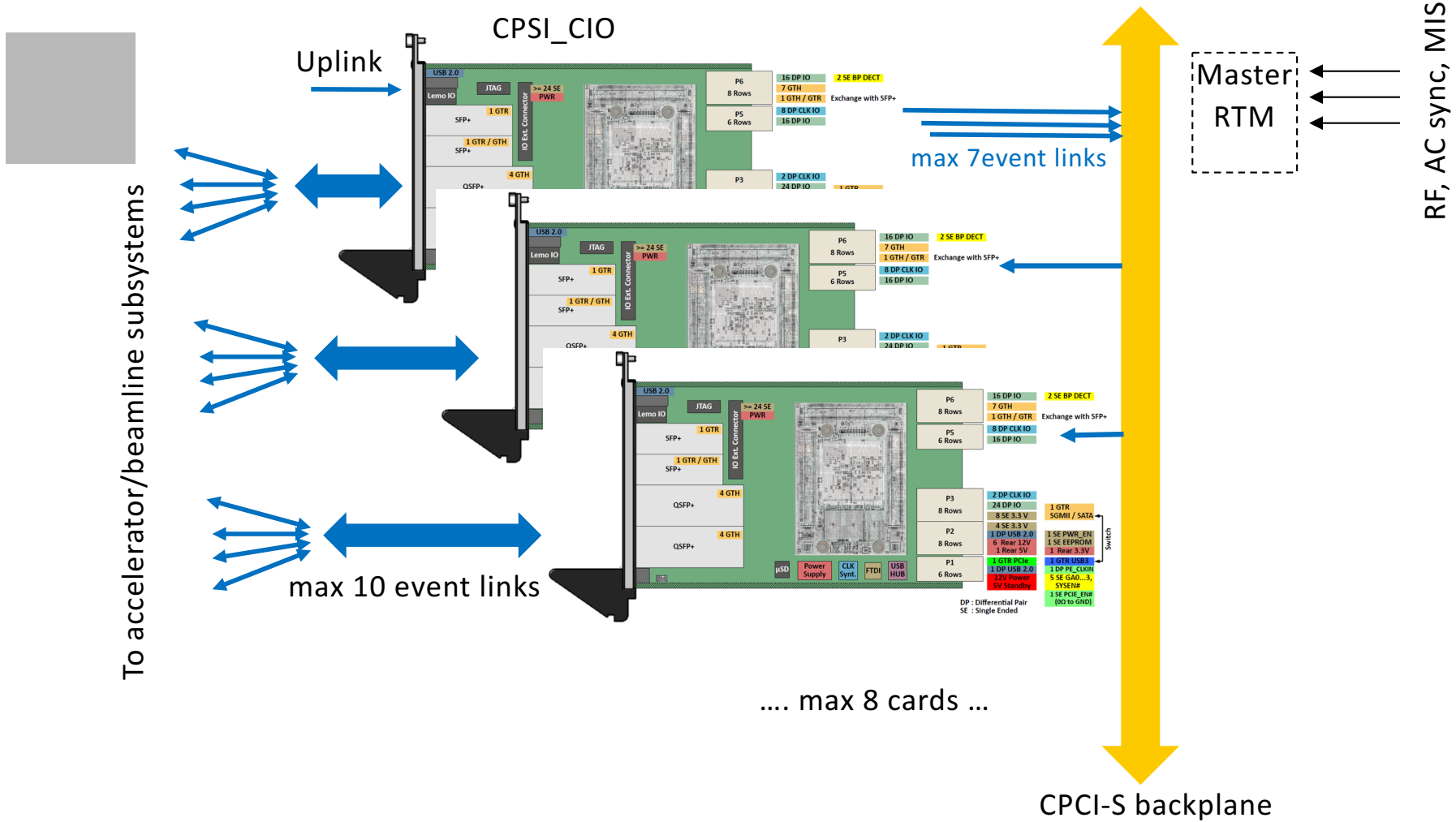
powerful system CPU

Control System
(EPICS)

Timing

SLS2.0 Timing

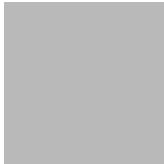
Master, Distribution, Receiver



Example of one timing master/distribution system within one CPCI-S crate. Timing network comprises multiples of demonstrated system.

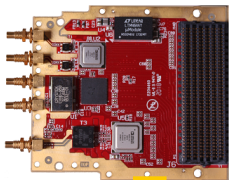
Fast Digitizer

candidates: SLS2.0 fill pattern monitor, scope recorder

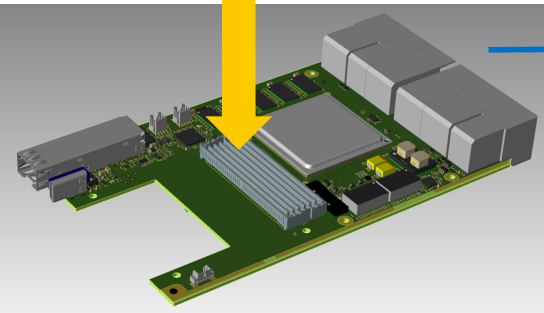


fill pattern sensor (APD)

signal conditioning
(gain/level shifter)
CPCI-S PAC2 or commercial



10 GSPS ADC
(from hitechglobal)



CPCI-S backplane

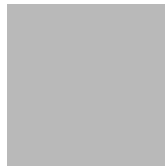


High performance system CPU
(for fill pattern, optional)

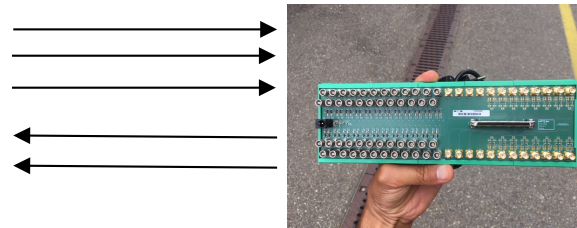
Fast streaming via PCIe
(DMA, PCIe Gen3, x8)

- Both apps require considerable amount of firmware and software developments
- Scope recorder will be a separate project for which AEK still needs inputs from users

Low-medium performance low-cost DAQ candidates: SLS2.0 ICT, Debye DAQ upgrade

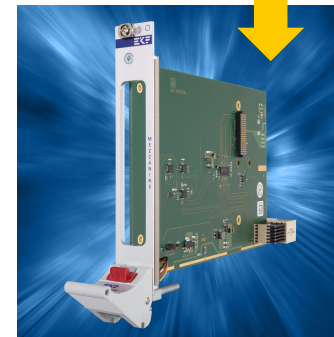
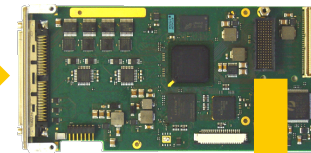


I/O
(ai/ao, bi/bo)



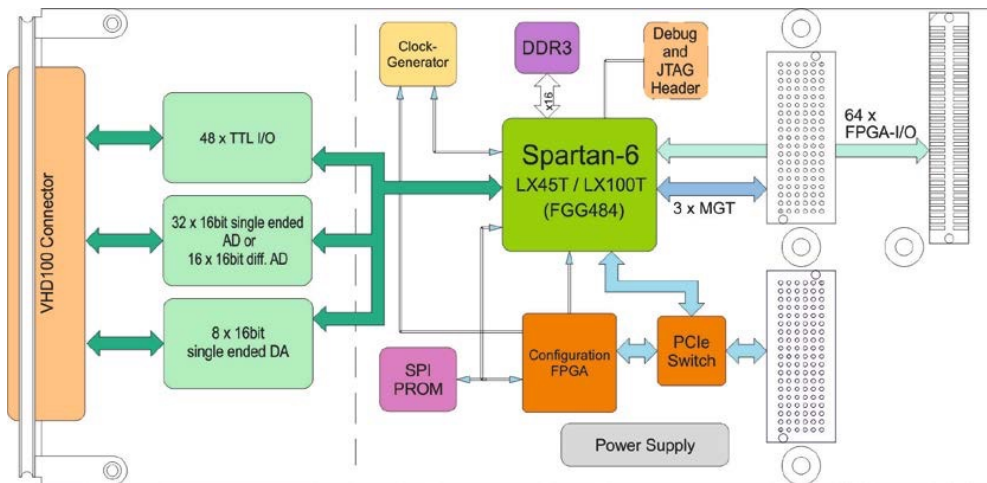
Terminal box

TXMC635



CPCI-S backplane

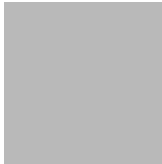
streaming via PCIe (DMA)



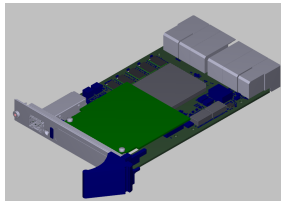
➤ Hytec replacement but...

- ✓ with higher performance, more channels & configurable application logic.
- ✓ glue ai/ao (1 MHz), bio (62 MHz), scalers, timers with self-specified logic
- ✓ Continuous/triggered acquisition

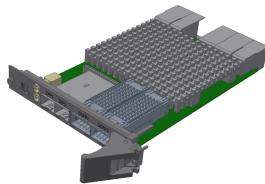
CPCI-S Toolbox Roadmap



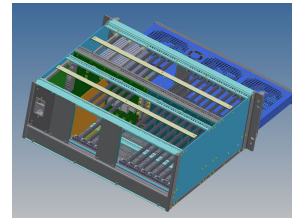
CPSI_UFC



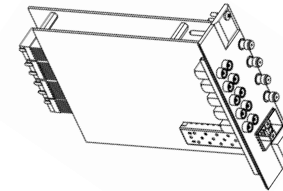
CPSI_CIO



CPSI-S crate



CPSI_RTM_DAC

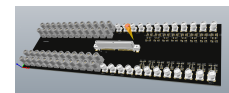


Board name	Prototype available	Current state	Comment
System CPU	COTS	in AEK Stock	preparing standard Linux boot
Multi IO TXMC635	COTS	in AEK Stock	generic scope app FW/SW
CPSI_UFC	Q3/21	Layout	Q2/22 HW/functionality tests
CPSI_CIO	Q3/21	Layout	Q2/22 HW/functionality tests
CPSI-S Crate	Q3/21	Review	Q2/22 HW/functionality tests
CPSI_RTM_DAC	Q4/21	Schematics	Q2/22 HW/functionality tests
Crate SysMon board	?	in specification	NUM card available (fallback)
Timing RTM	?	In specification	Master rear board

System CPU

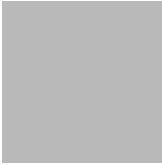


Multi I/O



SysMon card

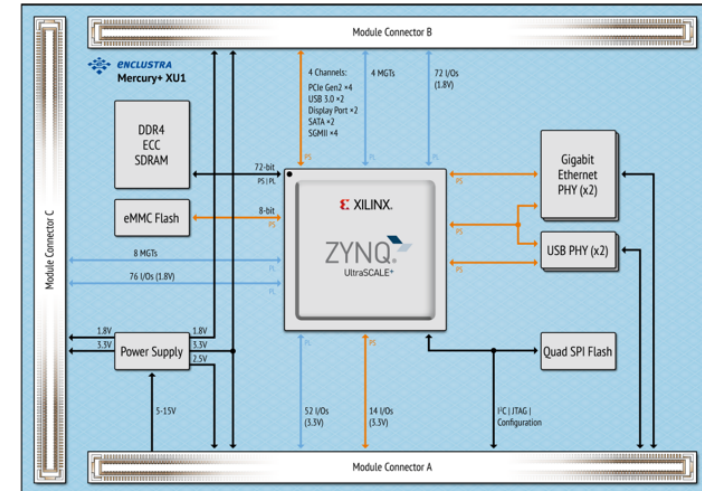
Timing RTM



Application specific Electronics

- Development of electronics tailored to specific application:
 - Requirements cannot be met with CPCI-S toolbox: environment conditions (noise, humidity, vibration), high level of signal integrity, mechanics & space, etc.
 - Where relatively large number of the same system has to be deployed
- Zynq Ultrascale+ MPSoC is the common building block

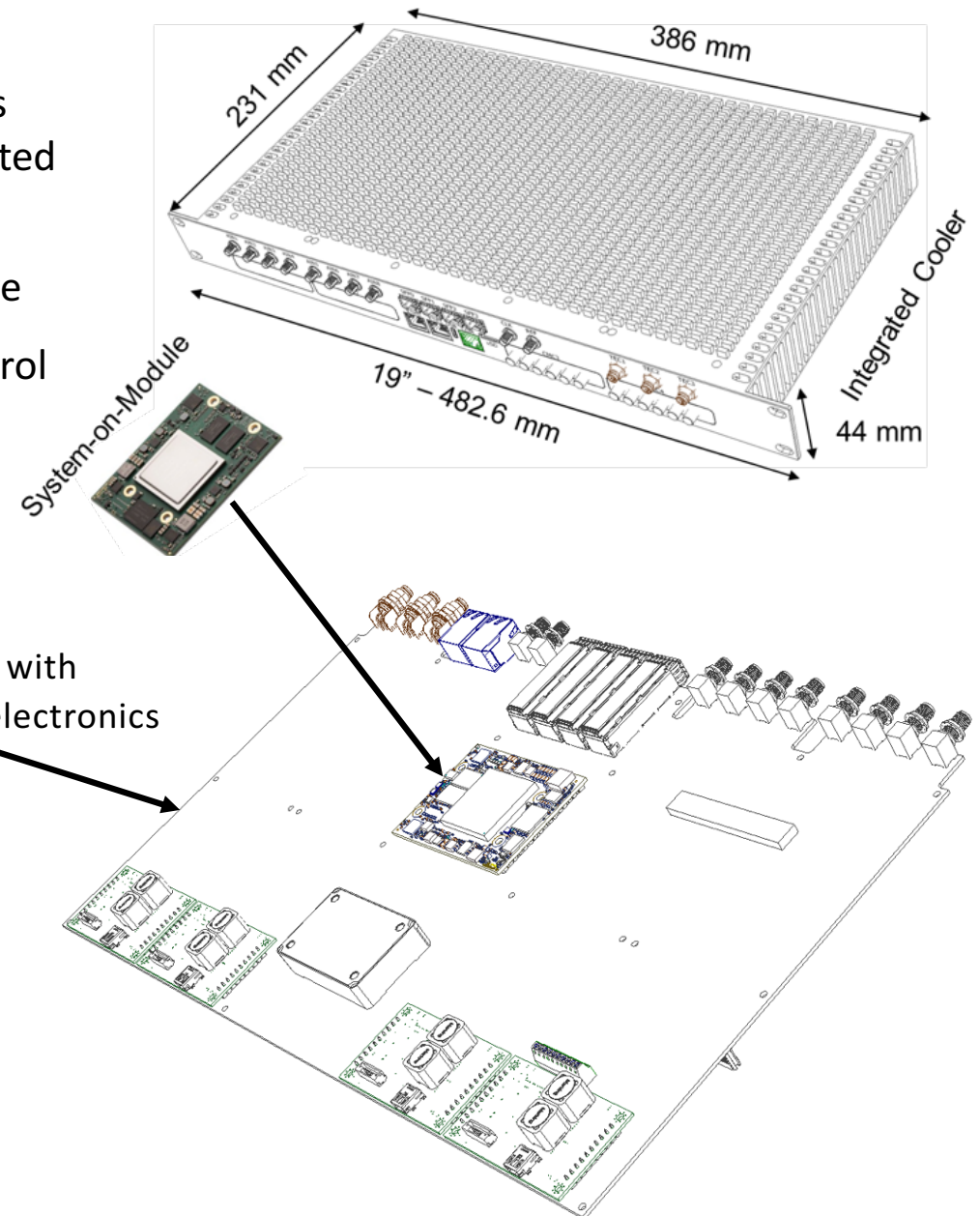
- Mostly use System on Module (SoM)
 - Important peripherals integrated (memory, ...)
 - Pre-engineered & tested
 - Hardware/software integration guidance



- Variations of SoMs will be kept under control by section Electronics in coordination with EInet-GERTS. This is to keep the support overhead under control specially for control system software but also for hardware integration.
- Supported SoM variants are currently: **XU1-6EG**, **XU5-5EV**, **XU1-6CG**,

SwissFEL Laser Synchronization SoM-DLL

- Synchronisation of various laser systems (e.g. in Athos & Aramis ES) with distributed reference clock of the accelerator
- Vibration, humidity, temperature sensitive
- Stability, reliability and supervisory control

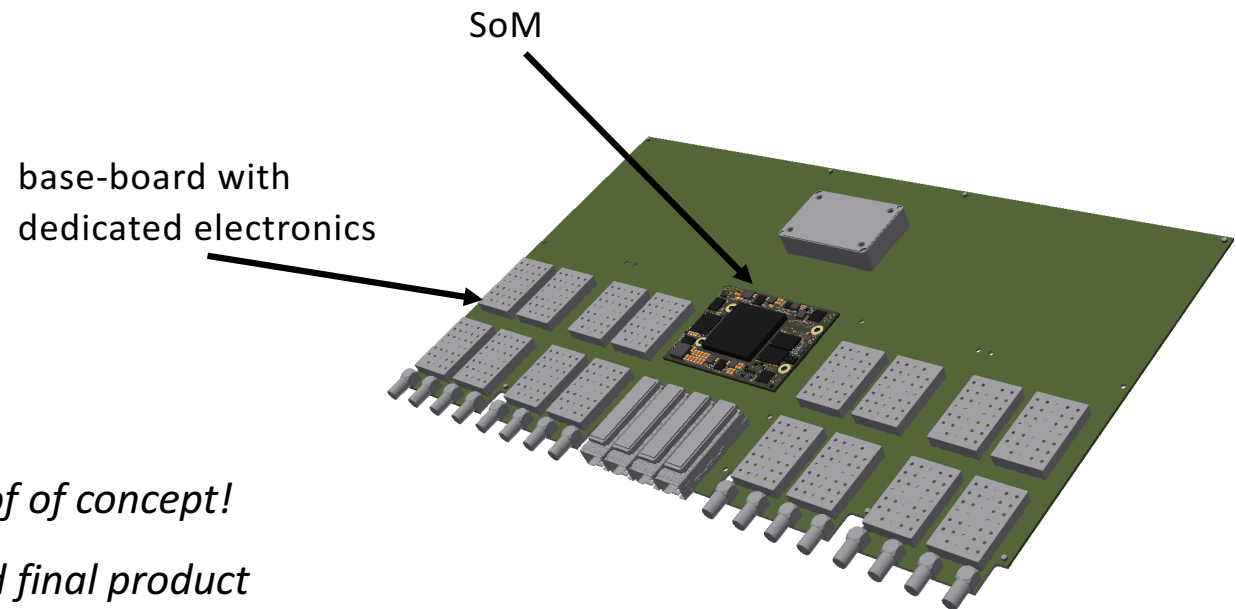
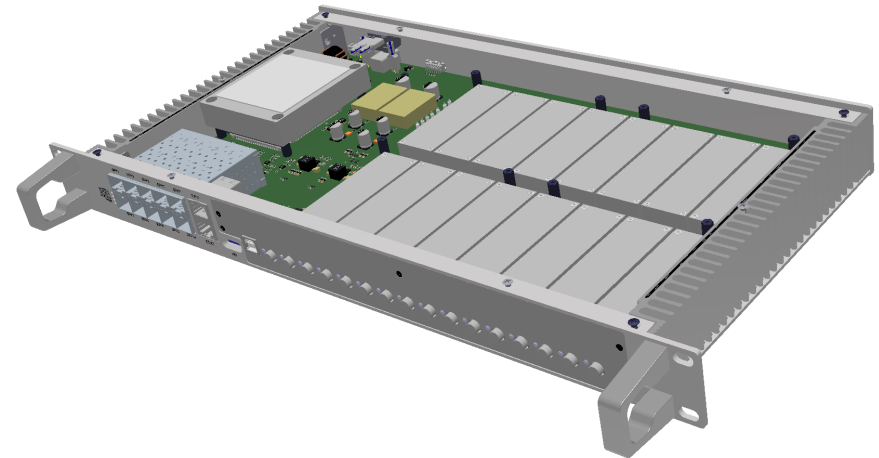


- *In close collaboration with Timing & Synchronisation group (8232)*
- *Currently in hardware concept & design phase.*
- *Contact: P. Pollet*

HIPA beam diagnostics upgrade

SoM-CAM

- Replace old CAMAC electronics in HIPA
 - Various Current Acquisition Modules
- Beam current measurement, generate Intrlocks
- High dynamic range: Log-Amp ($10E-12..10E-3$ A)
- Shares high synergies with SoM-DLL

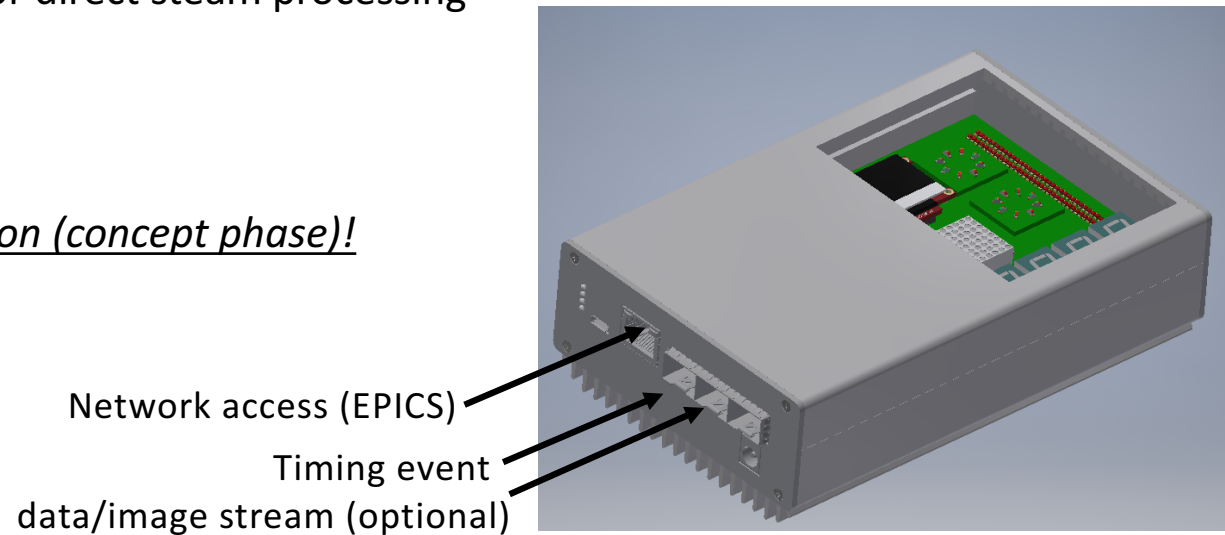
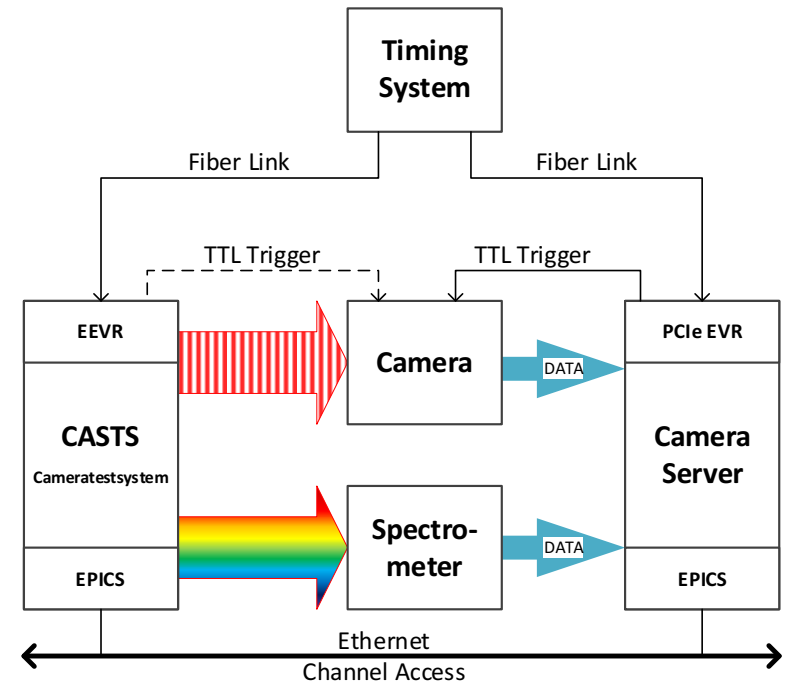


- *Pre-project completed -> proof of concept!*
- *Project in preparation to build final product*
- *Contact: E. Johansen*

Camera Test System CATST

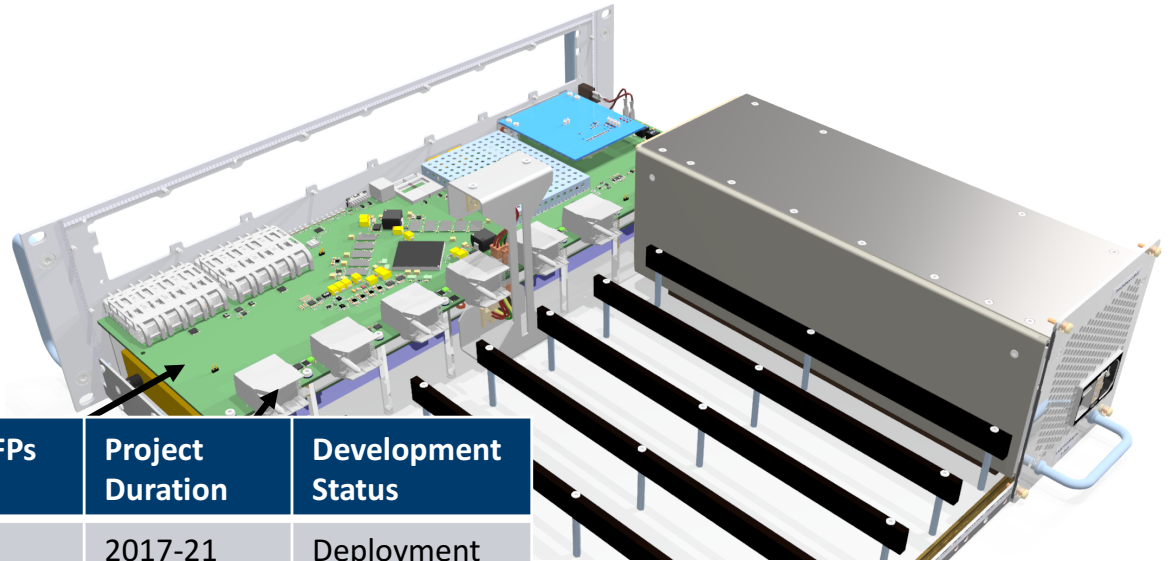
- Portable test-bed for investigating real-time behavior of camera or spectrometer systems
- Generates timing synchronised image patterns
- Uses same SoM as SoM-DLL and SoM-CAM
- can runs EPICS on the box
- Direct event link (EEVR)
- Additional Gigabit links for direct steam processing

- Project in early preparation (concept phase)!
- Contact: L. Moser



BPM Electronics (DBPM₃) SLS2.0,

- Optimized for BPM Systems
- Monolithic base-board (Back-end)
- Modular Front-End (RFFE)



Application	#DBPM3 Units*	BPMs or SFPs per Unit**	Project Duration	Development Status
SwissFEL undulator BPM	24	4	2017-21	Deployment
SLS1 RF BPM Upgrade	76	3	2019-23	Prototype
SLS1 Fast Orbit Feedb.	18	16	2020-23	WIP
SLS2 RF BPM	31	3	2023-24	Prototype
SLS2 Fast Orbit Feedb.	27	16	2022-24	Concept
HIPA RF BPM	20	3	2025+	Concept



- Implementation of the platform through close collaboration with accelerator feedback and measurement group (8231)
- Contact: B. Keil

various RFFE depending on facility or app area

Planning and Priorities

- Presented timelines are best estimate as of today:
 - Pandemic situation has affected industry -> large lead time for components
 - Some control system software (& firmware) developments happen after HW is stable

- AEK follows a clear process for accepting requests and planning projects
 - <https://intranet.psi.ch/de/aek/aeksupport>

- We do systematic project/resource planning (<http://i.psi.ch/ID002>)

- Some resource conflicts require decisions at division(s) level
 - Appeal to management for support and understanding in such situations

Many thanks to:

**AEK colleagues at sections
controls & measure/sync.**

**as well as colleagues at
EINet-GERTS**

