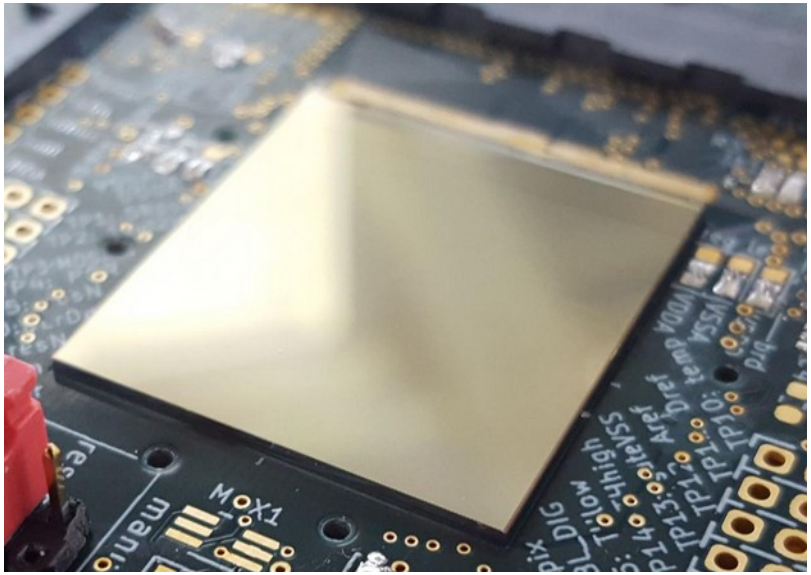
Mupix10 Status and MuPix11 Preparation

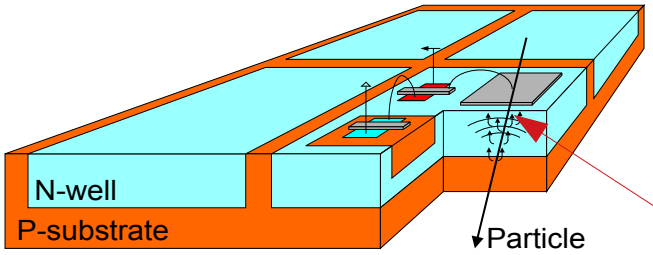
Review Meeting date XXX

High Voltage-Monolithic Active Pixel Sensors



High Voltage - Monolithic Active Pixel Sensor (HV-MAPS)

I.Peric, et al., NIM A 582 (2007) 876



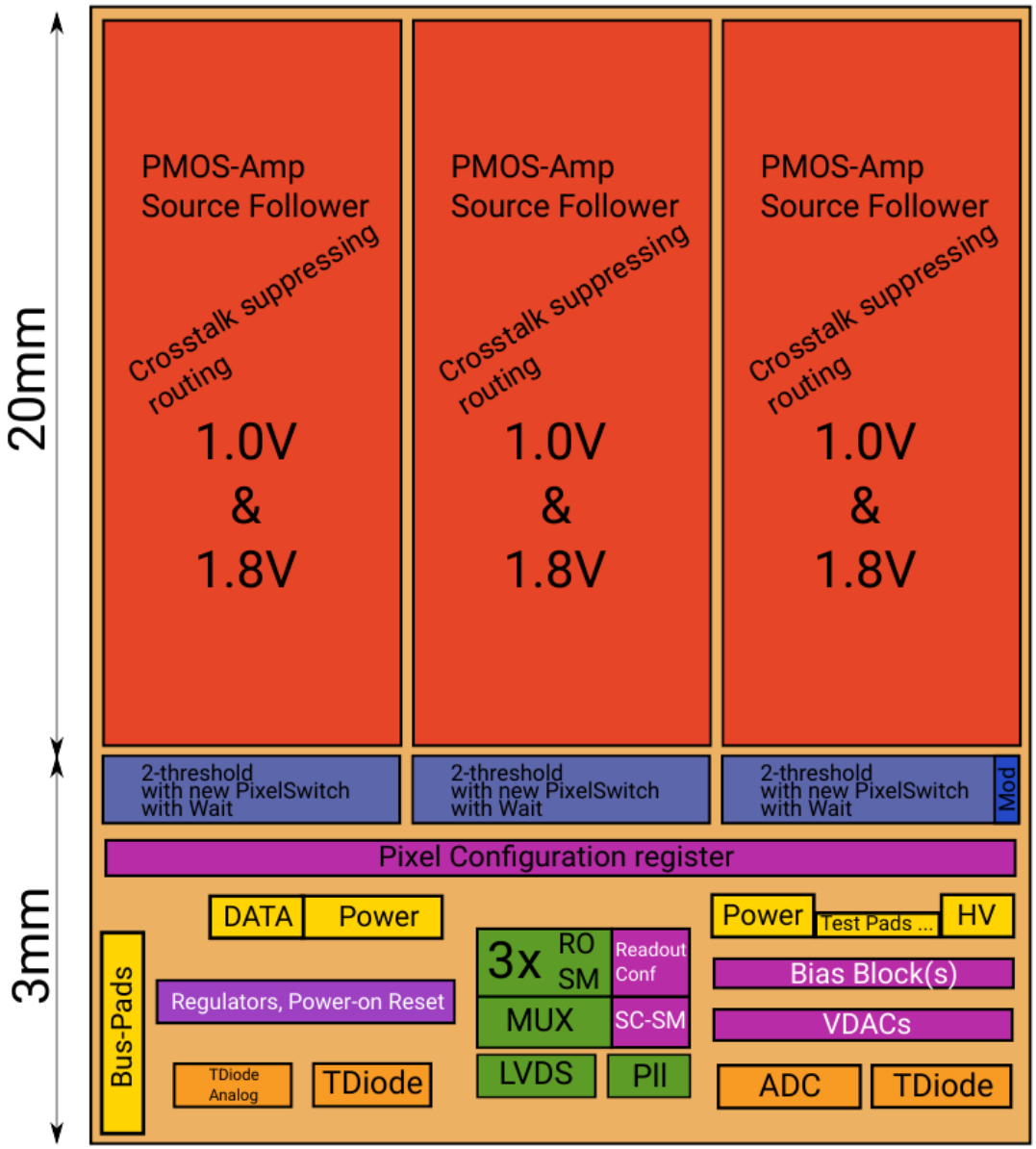
transistor logic embedded in N-well
("smart diode array")

charge collection by drift!

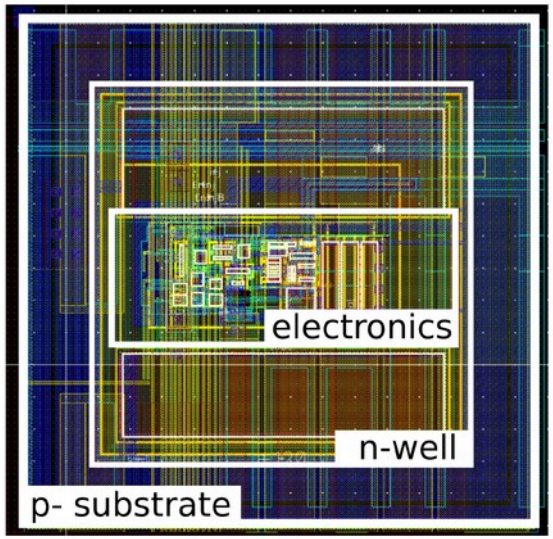
active sensor → hit finding & digitisation & zero suppression & readout

- low noise O(75-100e^-) → low threshold
- small depletion region of ≤ 30 µm → thin sensor ~50 µm
- HV-CMOS (60 - 120 V) process → fast charge collection
- industrial standard process → low production costs
- continuous and fast readout (serial link) → high rate applications

Mupix10 Design & Specifications



Pixel Matrix



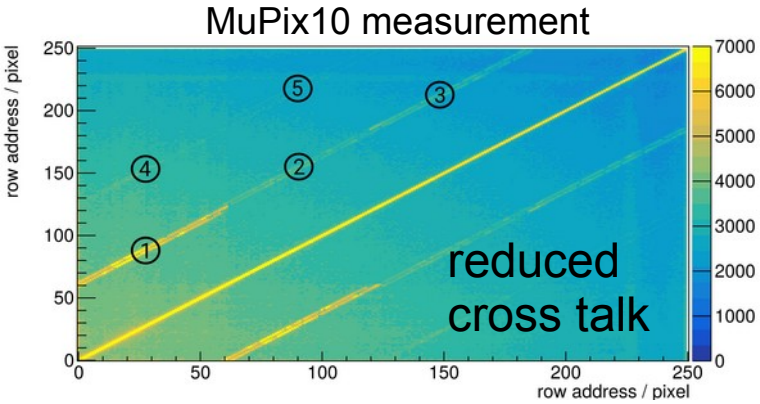
Specification from TDR

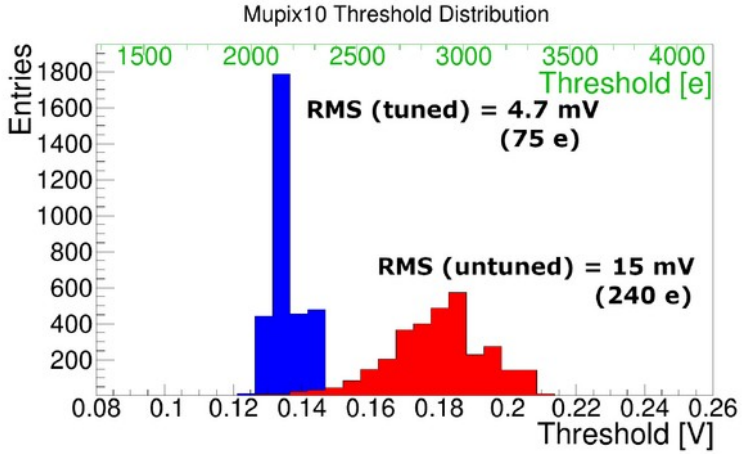
sensor dimensions [mm^2]	$\leq 21 \times 23$
sensor size (active) [mm^2]	$\approx 20 \times 20$
thickness [µm]	≤ 50
spatial resolution µm	≤ 30
time resolution [ns]	≤ 20
hit efficiency [%]	≥ 99
#LVDS links (inner layers)	1 (3)
bandwidth per link [Gbit/s]	≥ 1.25
power density of sensors [mW/cm^2]	≤ 350
operation temperature range [°C]	0 to 70

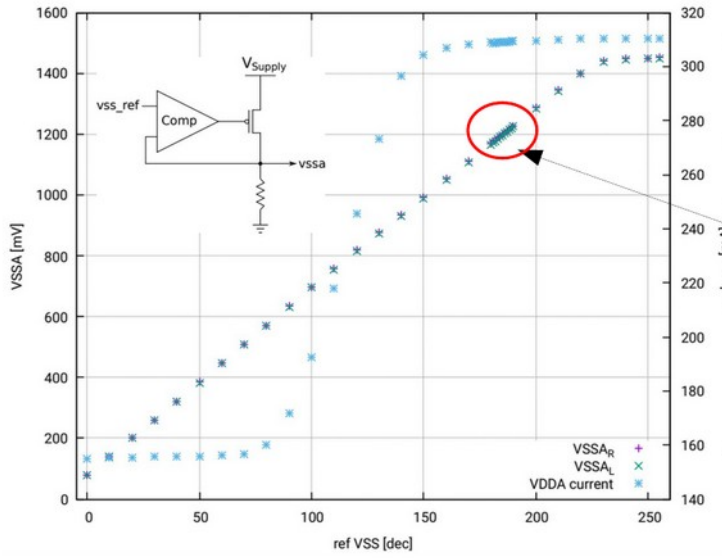
MuPix 10 Improvements wrt. MuPix8

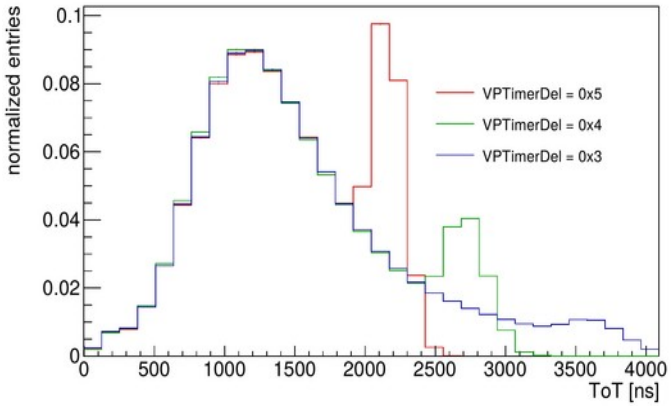
Main Optimisations and Improvements

- improved routing of analog signal lines to periphery
- improved speed of fast column readout (fast lanes)
- improved (fixed) pixel tuning
- delay circuit added (for readout)
- voltage regulator for VSSA (~1V)
- ...









All successful!

MuPix10 Main Issues

1) chip configuration problem → solved
2) speed of readout & state machine → probably solved
3) powering issues → solved
4) low signal → solved

Are we confident enough?

Need SNR plots!

Chip Configuration (severe impact!)

Issue 1

Three ways of configuration

1) legacy “all external” (slow protocol and many configuration lines)

2) standard SPI (4 configuration lines: CSB, MISO, MOSI, SCK)

3) Costumised Mu3e protocol (differential: SIN_p, SIN_n) → **baseline**

- motivated by routing problems on HDI (only one differential pair)
- first implemented in MuPix9 and successfully tested

ADD SCHEMATICS?!

Problem:

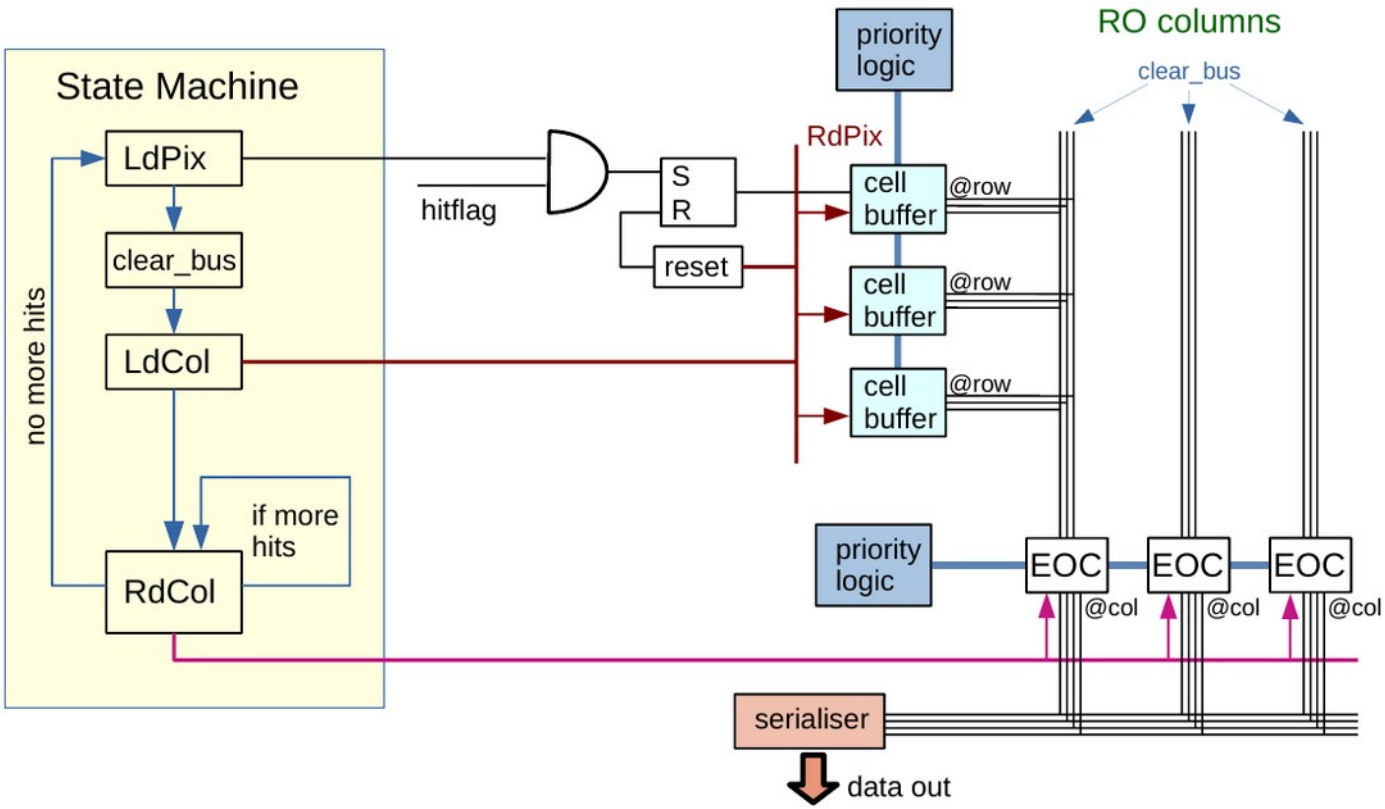
- loading of config registers triggers an auto-reset which is generated too early (probably tsu problem which is not seen in standard simulation)
- All three configuration schemes are affected but SPI configuration scheme is still operational “enough” to configure most functions of the chip.
- a possible issue with timing closure was found in the software library

Implemented fixes:

- implemented configuration registers as simple registers (not triple redundant)
- split *load* and *reset* signal (very simple fix)
- re-synthesize of VERILOG code with new library (→ see also later)

Readout & State Machine

Issue 2



maximum hit rate
~ 5 MHz / sensor

Readout & State Machine is supposed to run with a clock frequency of **62.5 MHz** (corresponding to ~30 Mhits per second)

Problem:

- readout errors at 62.5 MHz; but working at ~50 MHz
- for Mu3e only 31.25 MHz would be possible as alternative to 62.5 MHz (baseline)

Fixes

- use new synthesis framework optimised for TSI process, see next slide
- speed up state machine & machine and design (e.g. more power bus drivers, ...)

WHAT IS DONE HERE?

Note on Synthesis Framework

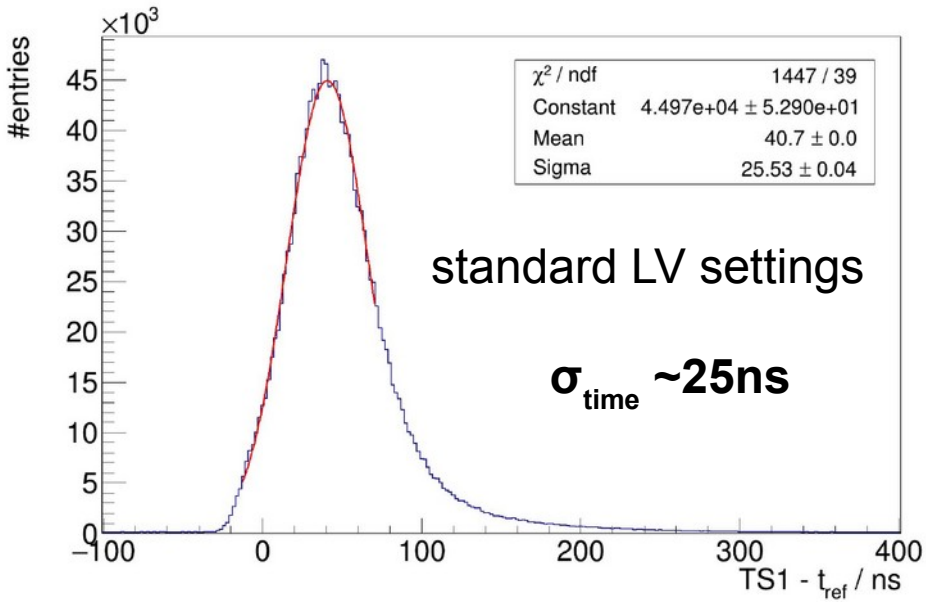
Issue 2

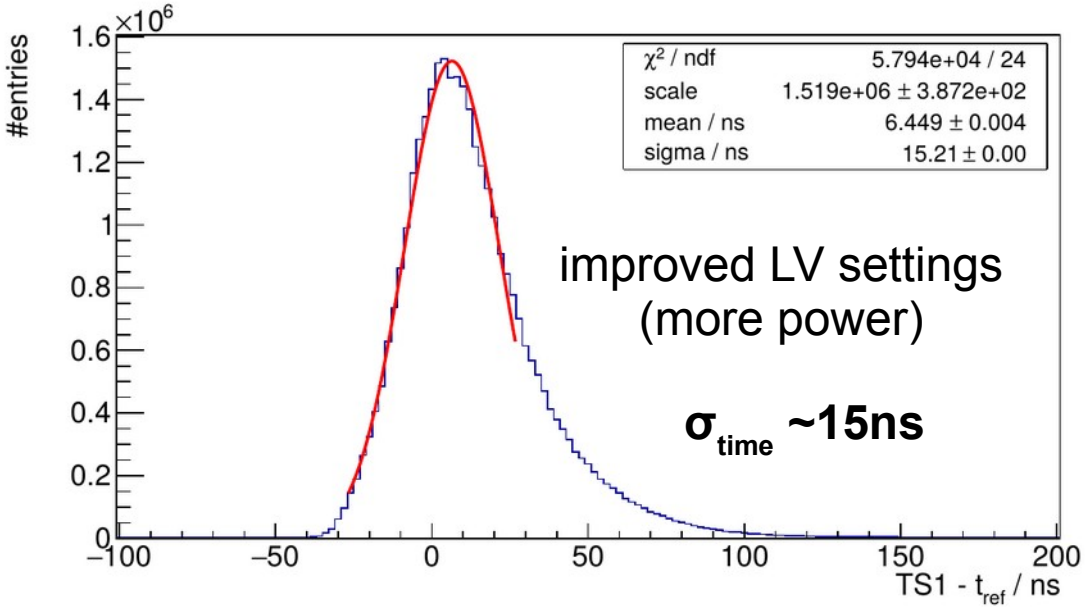
- All MuPix prototypes up to MuPix9 have been produced at **AMS** with a dedicated synthesis framework
- **MuPix10** (and MuPix7_B) produced at **TSI** foundry synthesised with the very same **"old"** framework since both processes (AMS & TSI) are very similar
- However, TSI has **7** metal layers (AMS has **6**) and capacities are slightly different (larger), thus slightly changing the properties of the circuits
- Larger (parasitic) **capacities** might cause problems for high **speed** and and other **critical** signals if old software framework is used
- A **new synthesis framework** with updated parameters was successfully created, and validated in the "Run2020" engineering run (16 test chips, other projects)

MuPix10 Powering

Issue 3

Uncorrected time resolution as measured with ^{90}Sr (bachelor F. Frauen):





MuPix10 allows to measure back (analog) the voltage inside the chip:

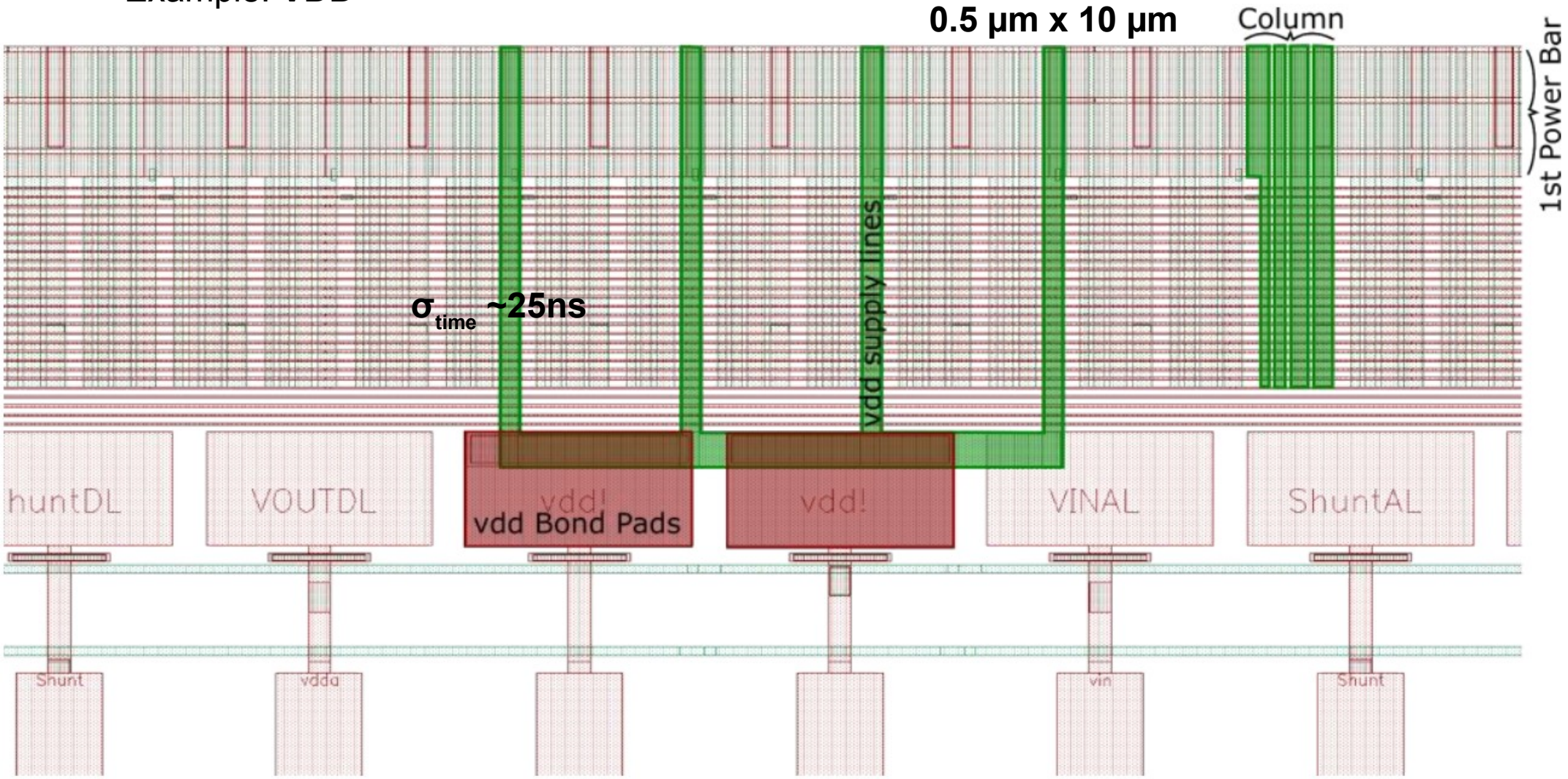
nominal		Number of Connections	With add. Connections	Measured Resistance	Calculated Resistance	Resistance with add. lines	Measured voltage drop	Expected voltage drop
1.8V	**vdd**	8	8+8	0.3Ω	0.26Ω	~0.13Ω	50mV	~25mV
0V	**gnd**	4	4+8	0.4Ω	0.33Ω	~0.11Ω	60mV	~20mV
1.8V	**vdda**	10	10+16	0.9Ω	0.75Ω	~0.37Ω	160mV	~60mV
0V	**gnda**	11	11+10	0.6Ω	0.36Ω	~0.19Ω	170mV	~90mV
1.2V	**vssa**	8	8+6	1.0Ω	0.76Ω	~0.44Ω	130mV	~75mV

Culprit: Pad to Power-Bar Connection

Issue 3

Example: **VDD**

cross section
0.5 µm x 10 µm

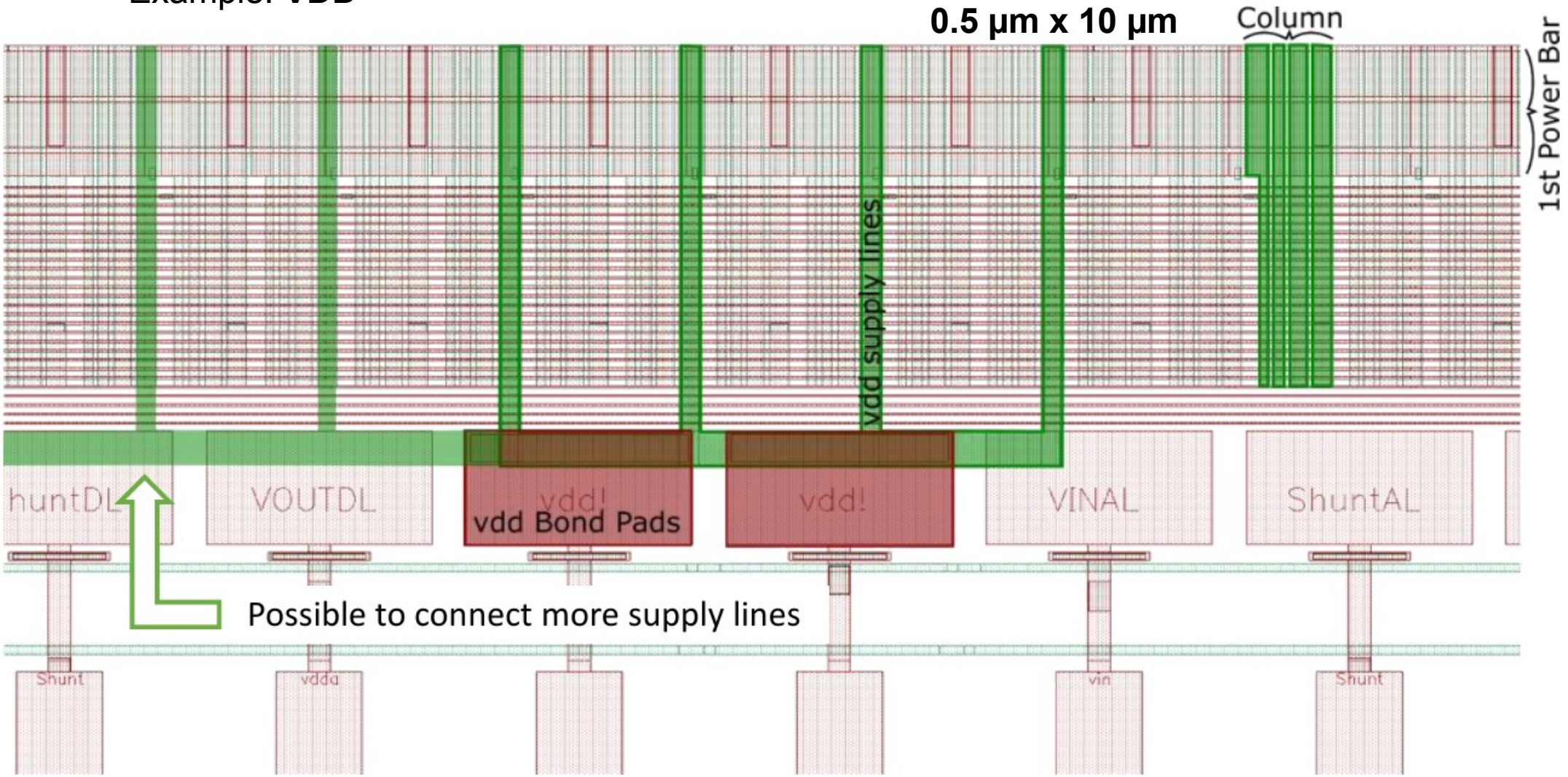


Fix: Increase Connections

Issue 3

Example: **VDD**

cross section
0.5 µm x 10 µm



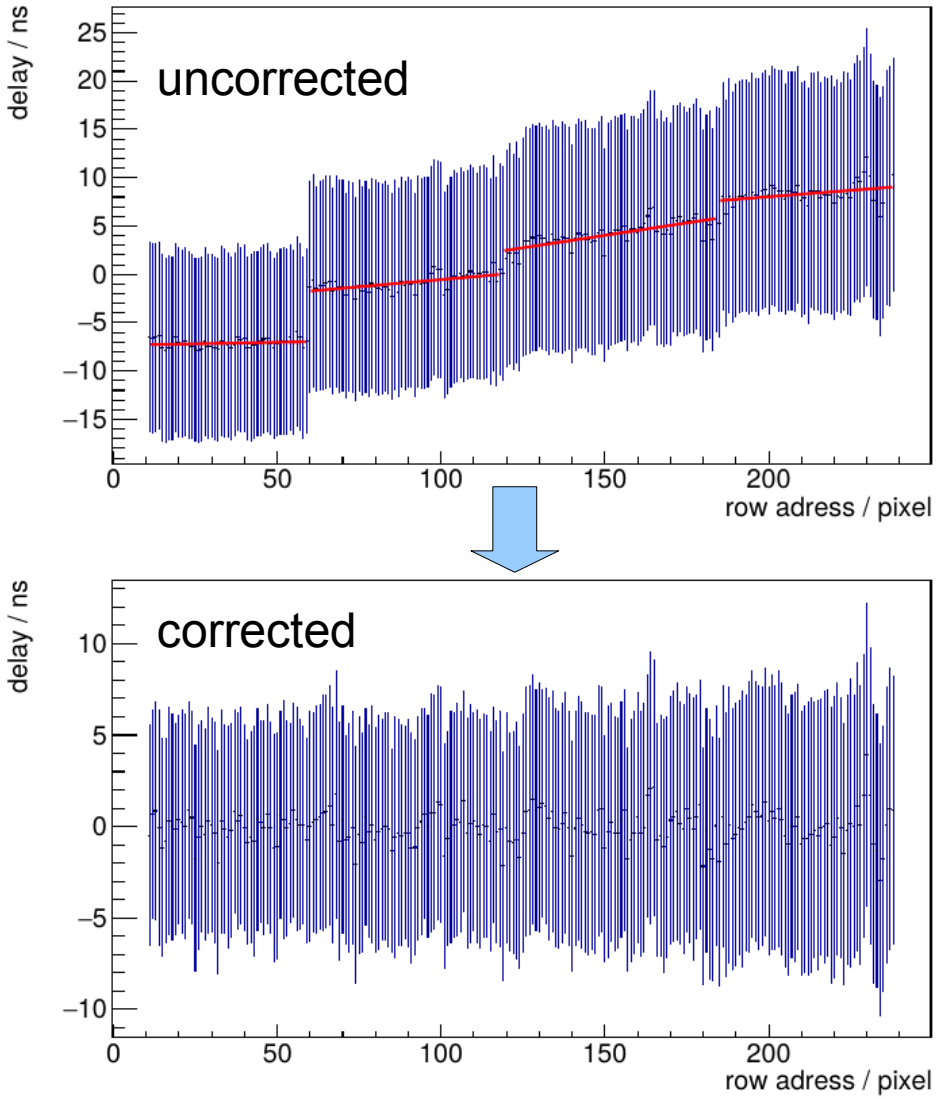
In addition, more metal layers are used

(similar for VDDA, VSSA, GND and GNDA)

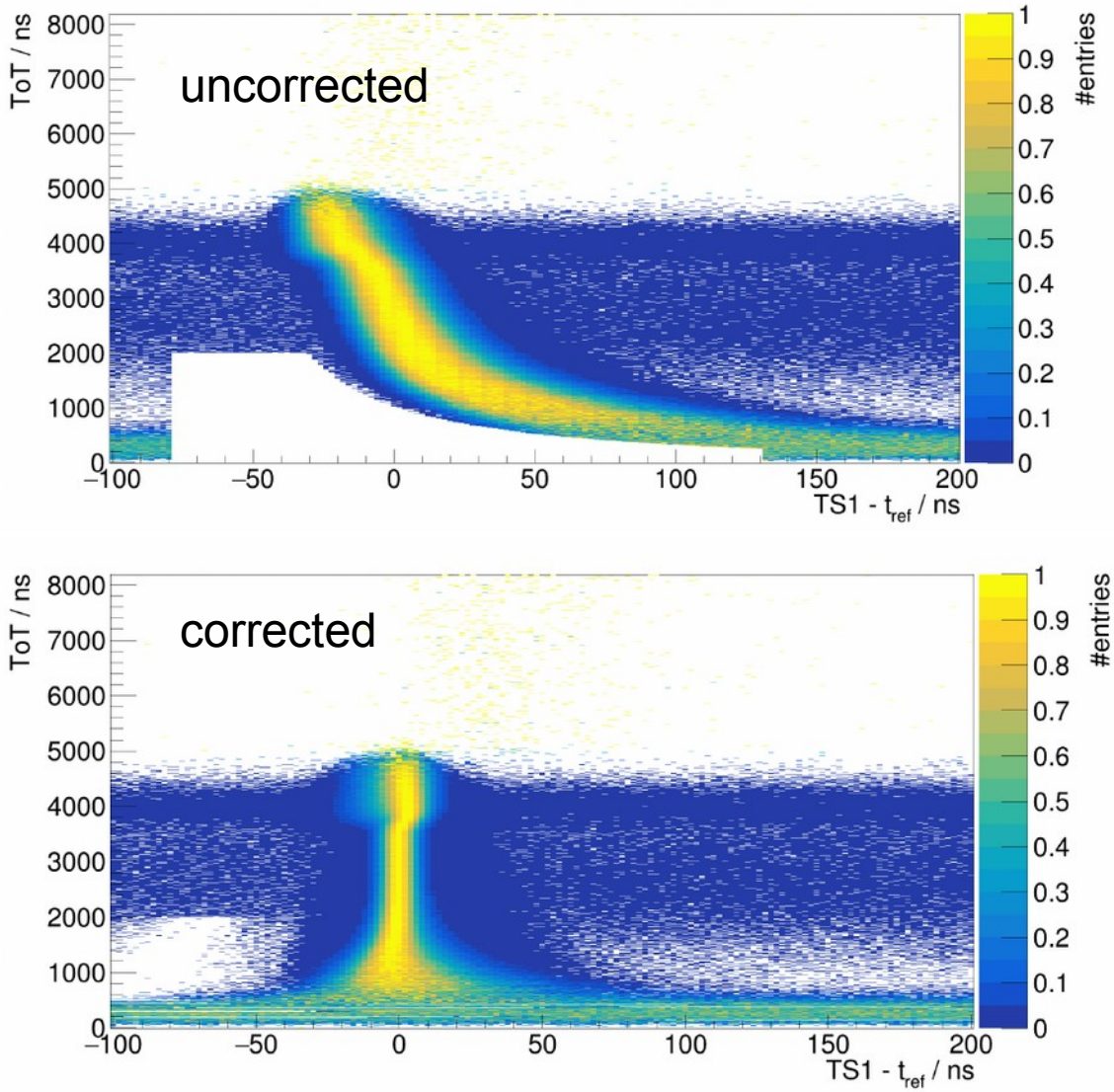
Time Resolution with Improved Powering

(bachelor F. Frauen) Issue 3

row dependent delay correction

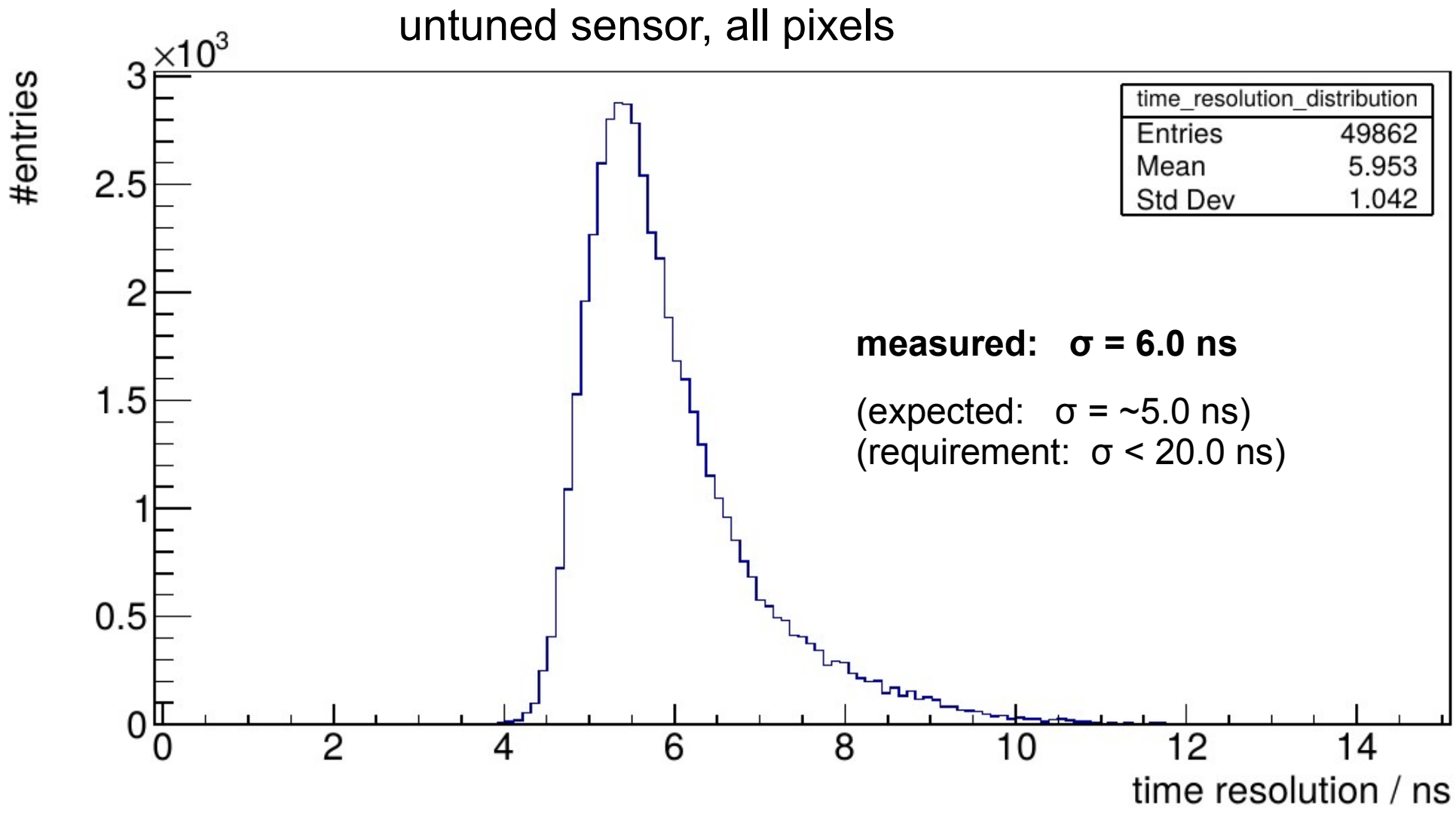


time-walk: ToT versus delay



Time Resolution with Improved Powering

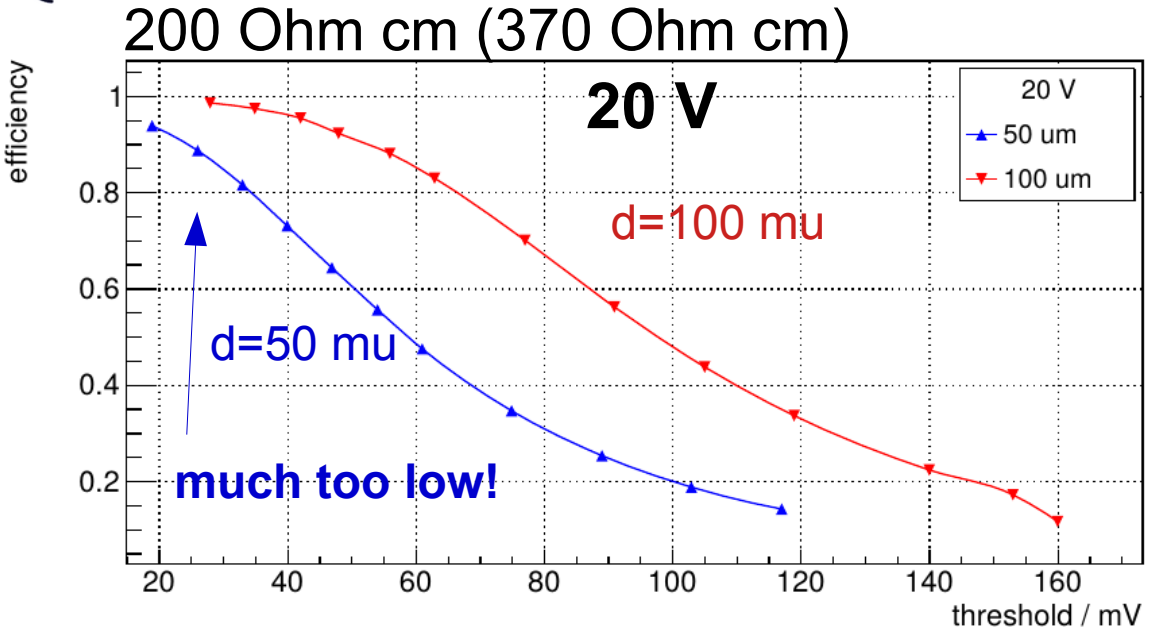
Issue 3



for comparison: ATLASpix3 (comparator in pixel) has a time resolution of about 4ns

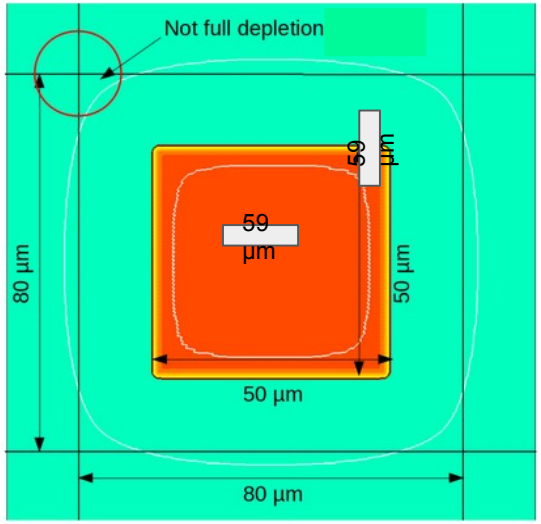
The Low Signal Problem I

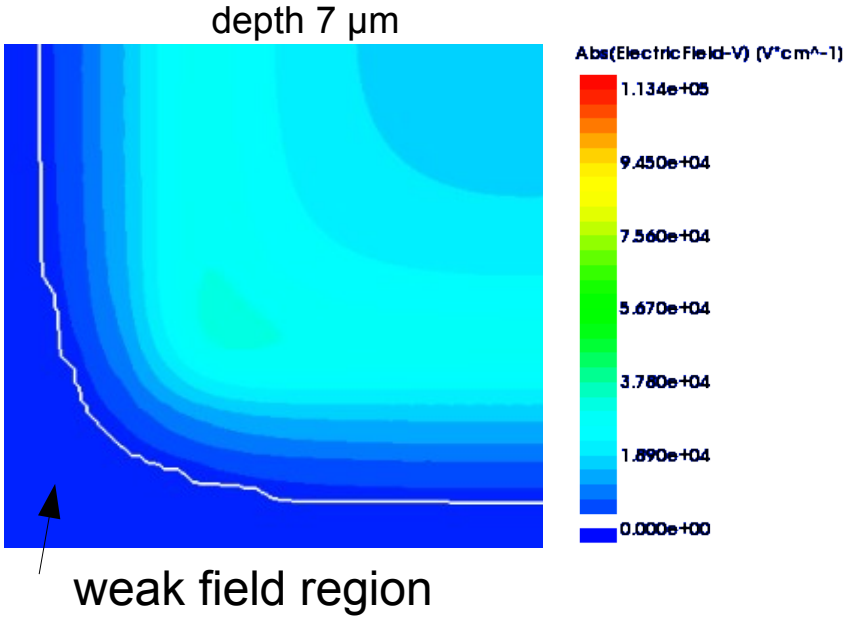
Issue 4



- Hit efficiency of **50 mu sensor** does not fulfill the specification
- inefficiencies originate from pixel edges and corners
- 100 mu sensor is more efficient due to contribution from diffusion

Results from TCAD simulations for
200 Ohm cm and -30V

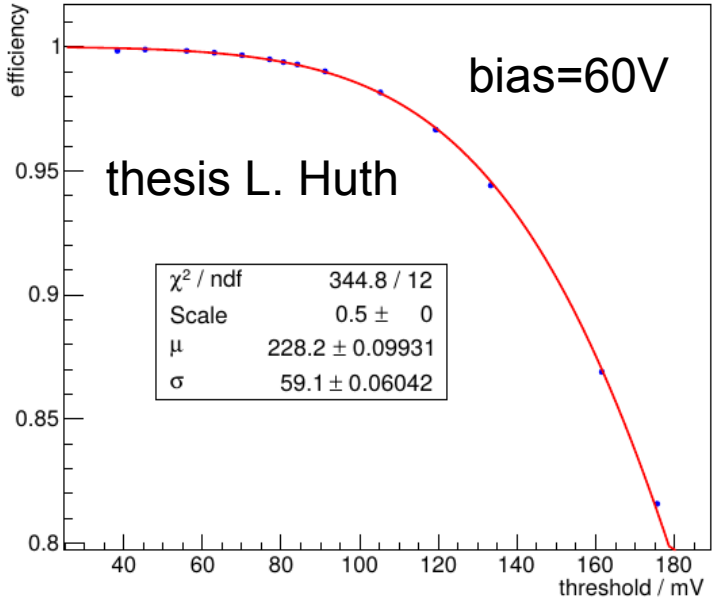




The Low Signal Problem II

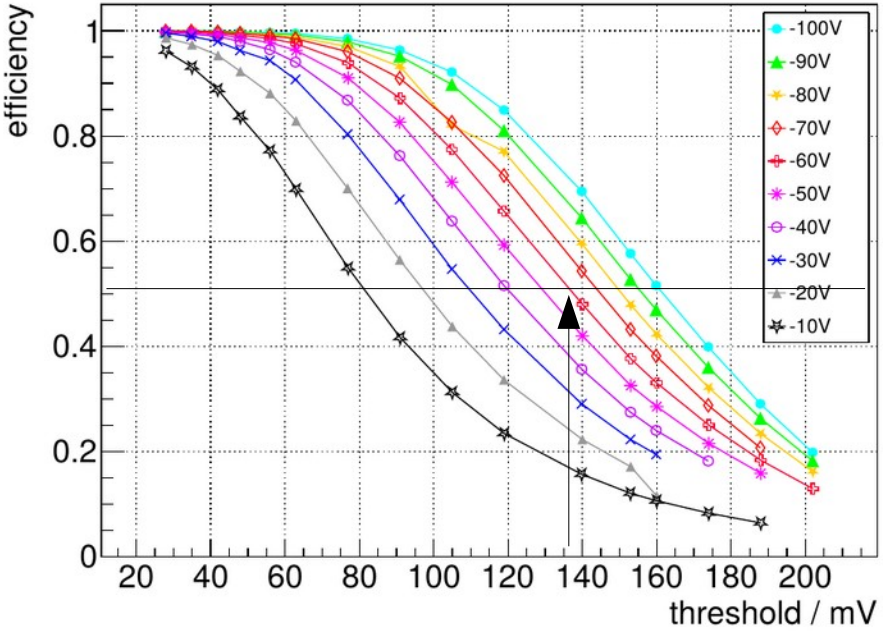
Issue 4

MuPix8 testbeam:
(100 um thickness, 200 Ohm cm



50% efficiency at **229mV**

MuPix10 testbeam:
100 um thickness, 200 Ohm cm)



50% efficiency at **137 mV** (56%)

Signal is much smaller (56%) than expected from Mupix8

Amplifier and comparator basically unchanged from MuPix:

- AC coupling between source follower and comparator was slightly changed (50%)
- Capacity of baseline restoration transistor was changed

(both changes are expected to have minimal effects on performance)

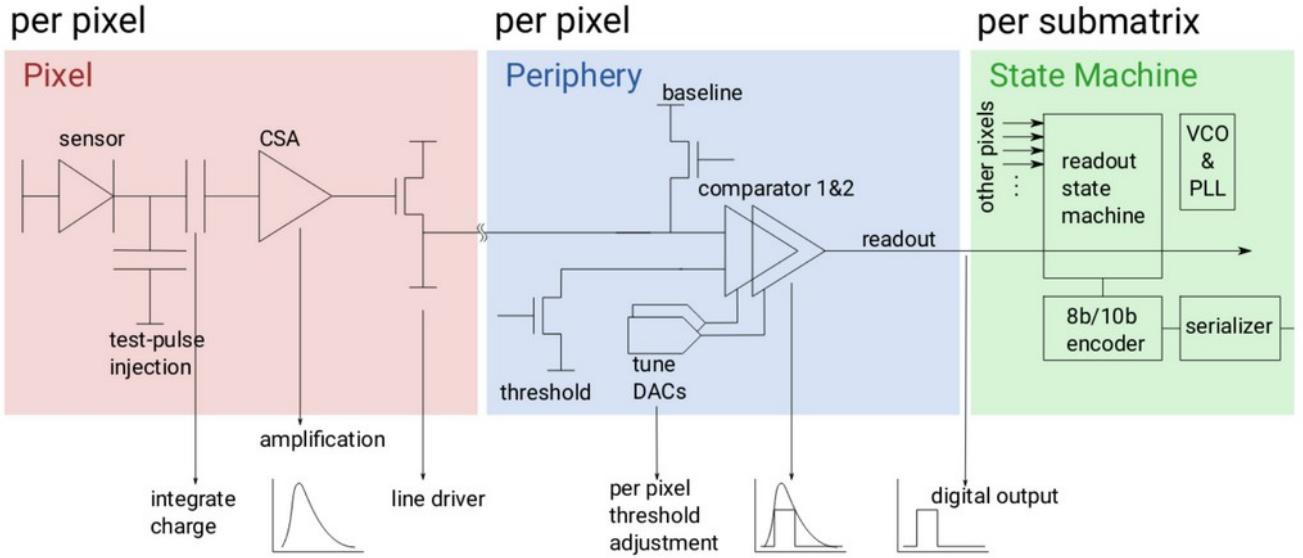
Correct TDAC Settings?

Issue 4

History of Mupix10 optimisation:

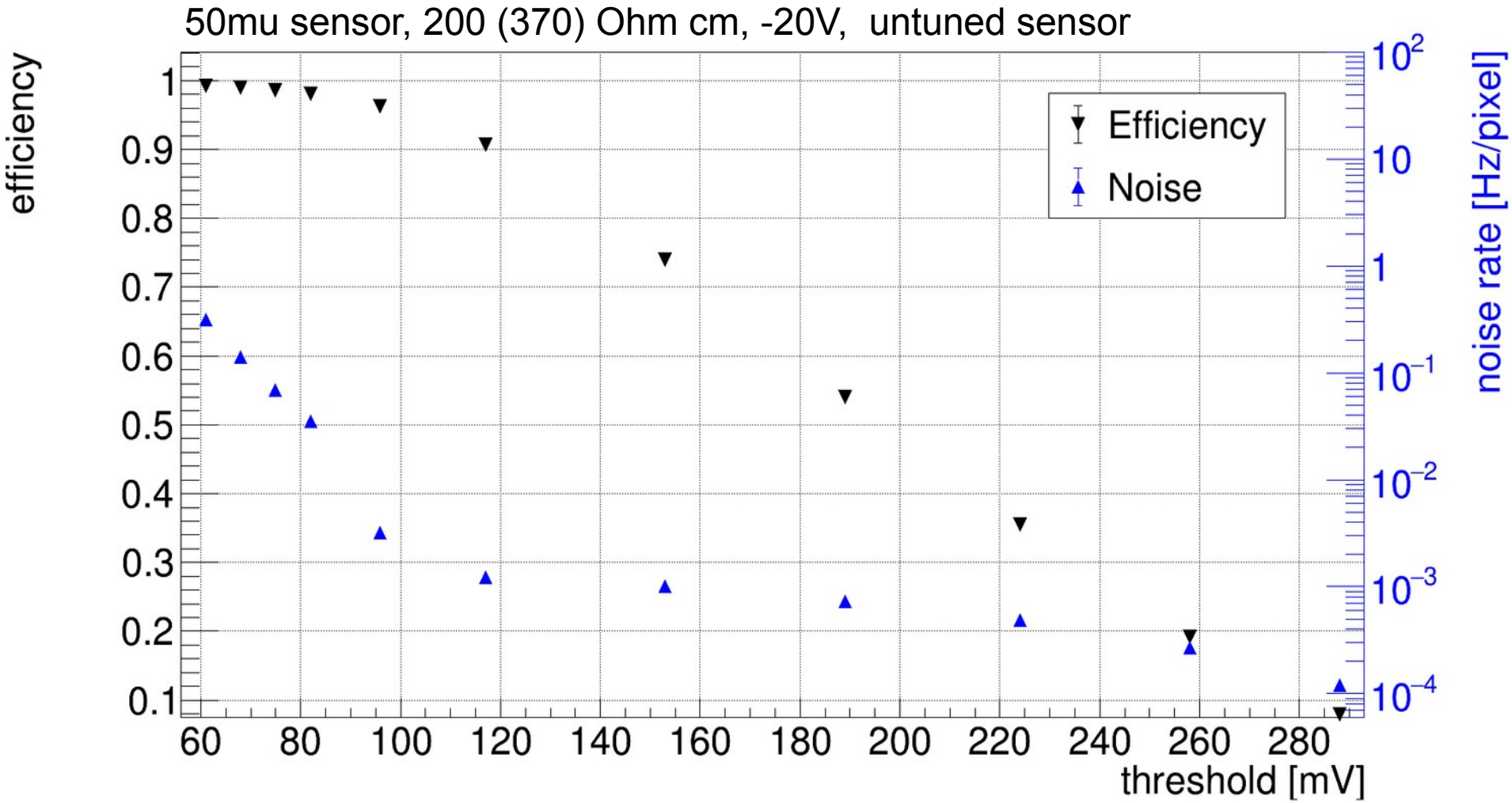
- TDAC settings were optimised for time resolution with ^{90}Sr source
- then in-chip voltage drops (issue3) were found and fixed
- TDAC re-optimisation done with ^{90}Sr yielding improved but still unsatisfactory results
- further investigations brought more findings:
  - low voltage level of comparator baseline should be avoided
  - employed timing optimisation had a bias
    (integrated time resolution improves when cutting out small signals)
- settings were optimised again by checking directly the rising edge

Note: the charge is collected by drift within <1ns. The steeper the rising edge of the comparator input, the higher the signal efficiency.



New Result from Nov. Testbeam (DESY)

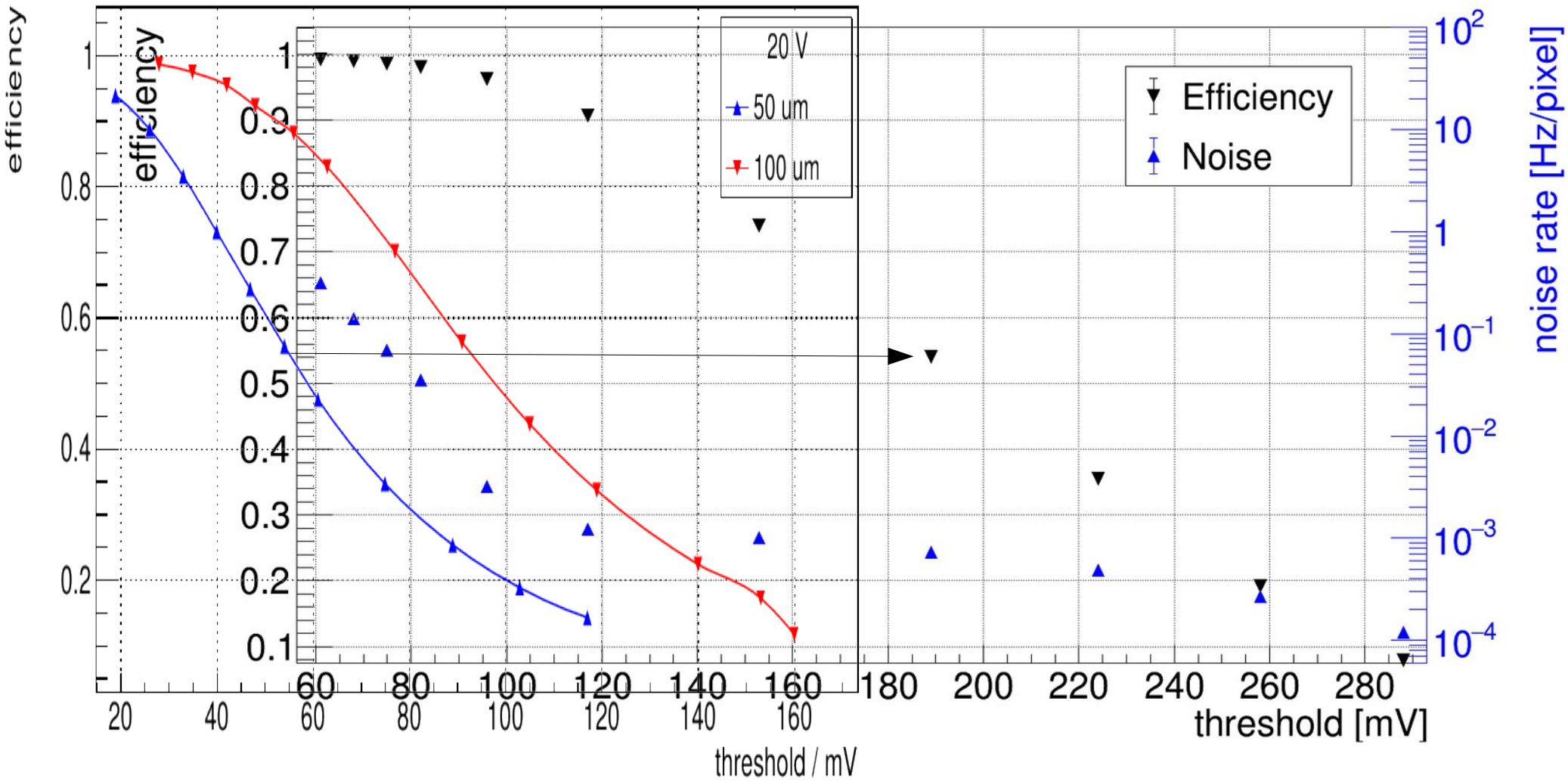
Issue 4



- hit efficiency >99%
- noise from a few hot pixels (untuned) increases at low threshold
- noise rate is small (<< 20 Hz/pixel)

Comparison Old vs. New Settings

Issue 4



- the signal is substantially larger with the new settings!
- issue is solved and understood!

COULD WE HAVE CONSISTENT PLOTS?

Other Minor Changes for MuPix11

1) Removal of dedicated R&D columns to improve homogeneity of sensor → uncritical
2) Removal of 1.8 voltage regulators (not needed) → uncritical
3) Shift HV pad by 50 um to improve handling and operation → uncritical
4) adjust dynamical range of VPDAQ (pixel tuning) → uncritical
5) adjust dynamical range of delay circuitry → uncritical
6) implement faster baseline restauration → uncritical
7)

WHAT ELSE ?

Dedicated R&O columns

Minor 1

add TEXT

1.8 Voltage Regulators

Minor 2

- For test purposes and for a serial powering study 1.8V regulators were added to MuPix10
- They are not needed for Mu3e phase I and not foreseen in baseline design which is based on external regulators
  - decision to remove!
  - frees some pads which can be better used for GND/powering!

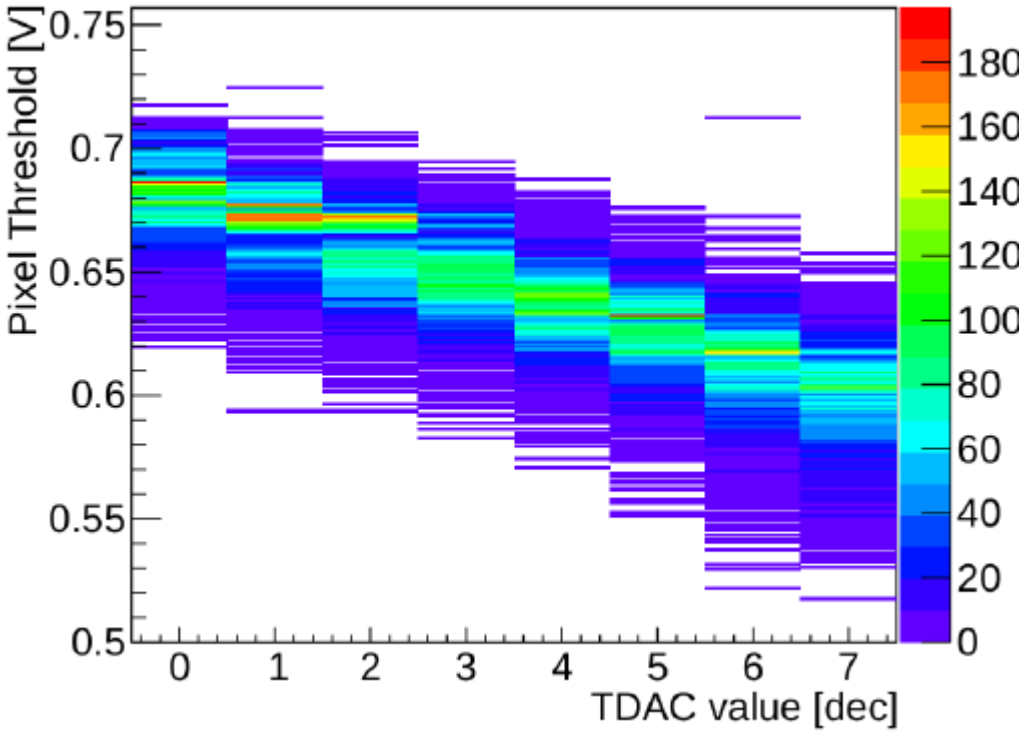
Shift HV pad by 50 um to improve handling and operation

Minor 3

ADD PICTURE FROM HEIKO

Dynamical range of VPDAC (pixel tuning)

Minor 4

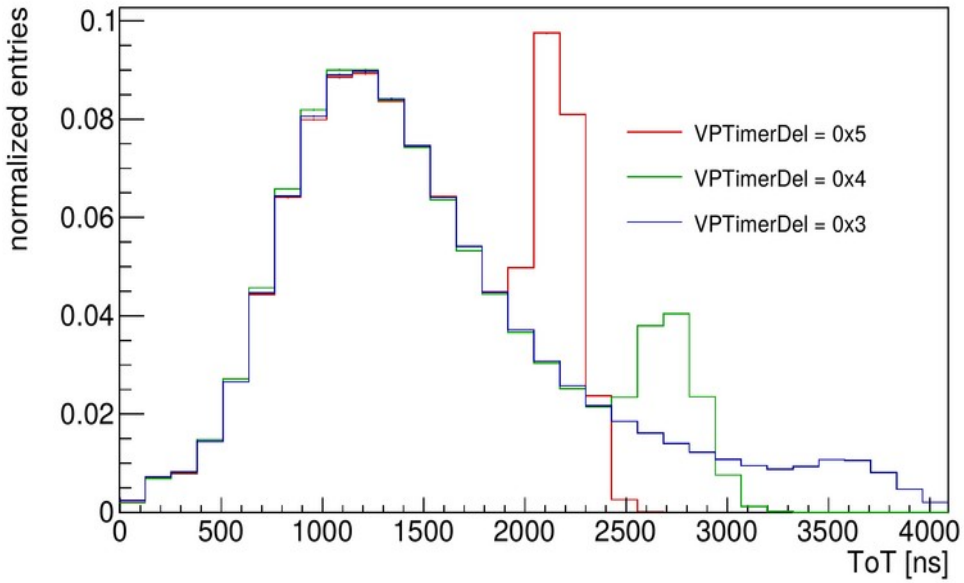


The adjustable range is a bit too narrow

HEIKO, ADD COMMENT

Dynamical range of delay circuitry

Minor 5



The delay point is given by:

delay = 10 mus / TDAC(4 bit)

correct?

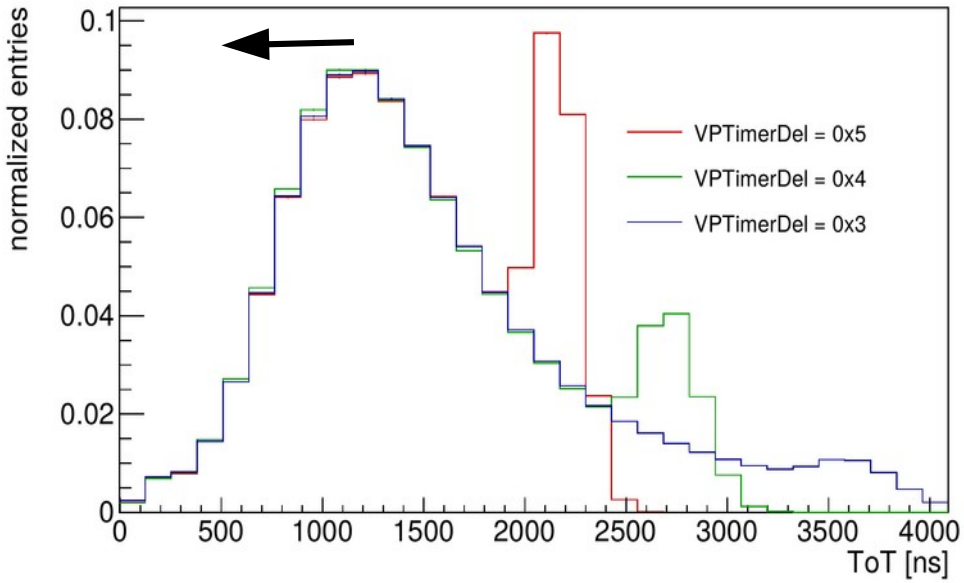
The full range (MSB) can essentially not be used

AS: I think the real problem is that the pulses are to long!

Baseline Restoration

Minor 6

0.5 mus



1 mus

See previous point!

Baseline restoration should be speed up by a factor 2-4

COMMENTS!

ADD SCHEMATICS

Validation of MuPix10 Specifications

	specification	measured	
sensor dimensions [mm^2]	$\leq 21 \times 23$	OK	
sensor size (active) [mm^2]	$\approx 20 \times 20$	OK	
thickness [µm]	≤ 50	OK	
spatial resolution µm	≤ 30	OK	
time resolution [ns]	≤ 20	OK	plots for 100mu
hit efficiency [%]	≥ 99	OK	
#LVDS links (inner layers)	1 (3)	OK	
bandwidth per link [Gbit/s]	≥ 1.25	OK	
power density of sensors [mW/cm^2]	≤ 350	~ 200, OK	
operation temperature range [°C]	0 to 70	plan to operate as cold as possible	

List of Implemented Changes (Status)

- A
- B
- C

END

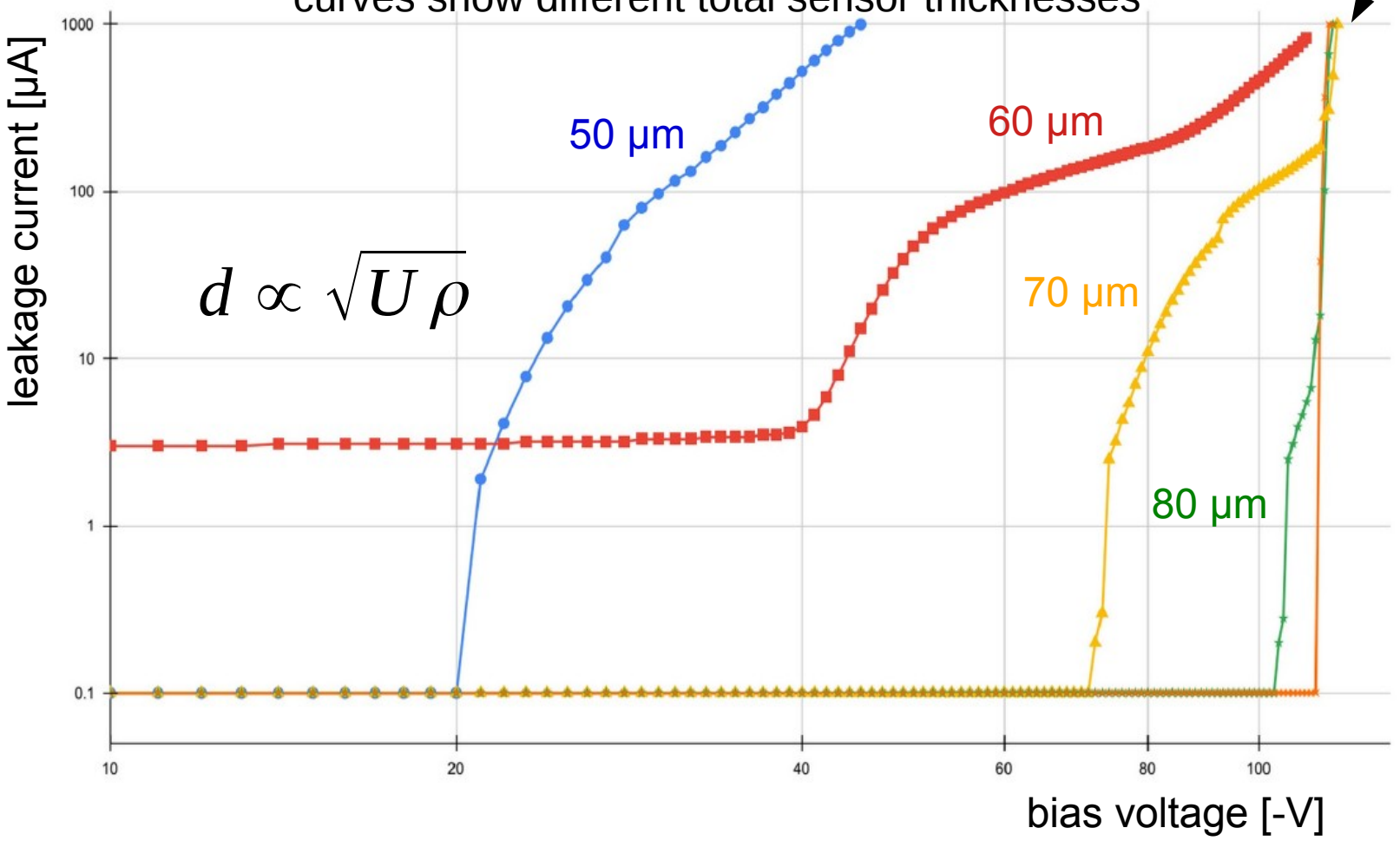
Backup

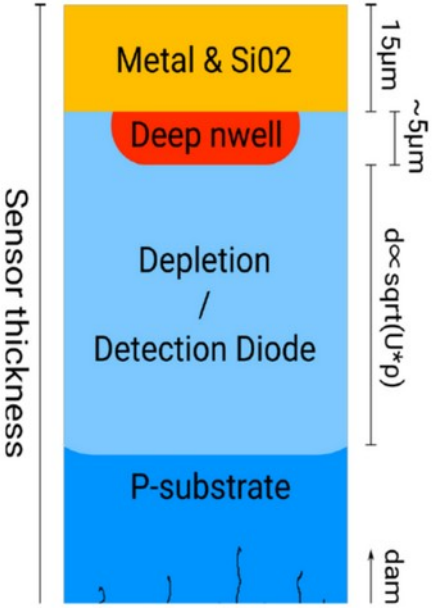
Depletion and Sensor Thickness

I-V curves

curves show different total sensor thicknesses

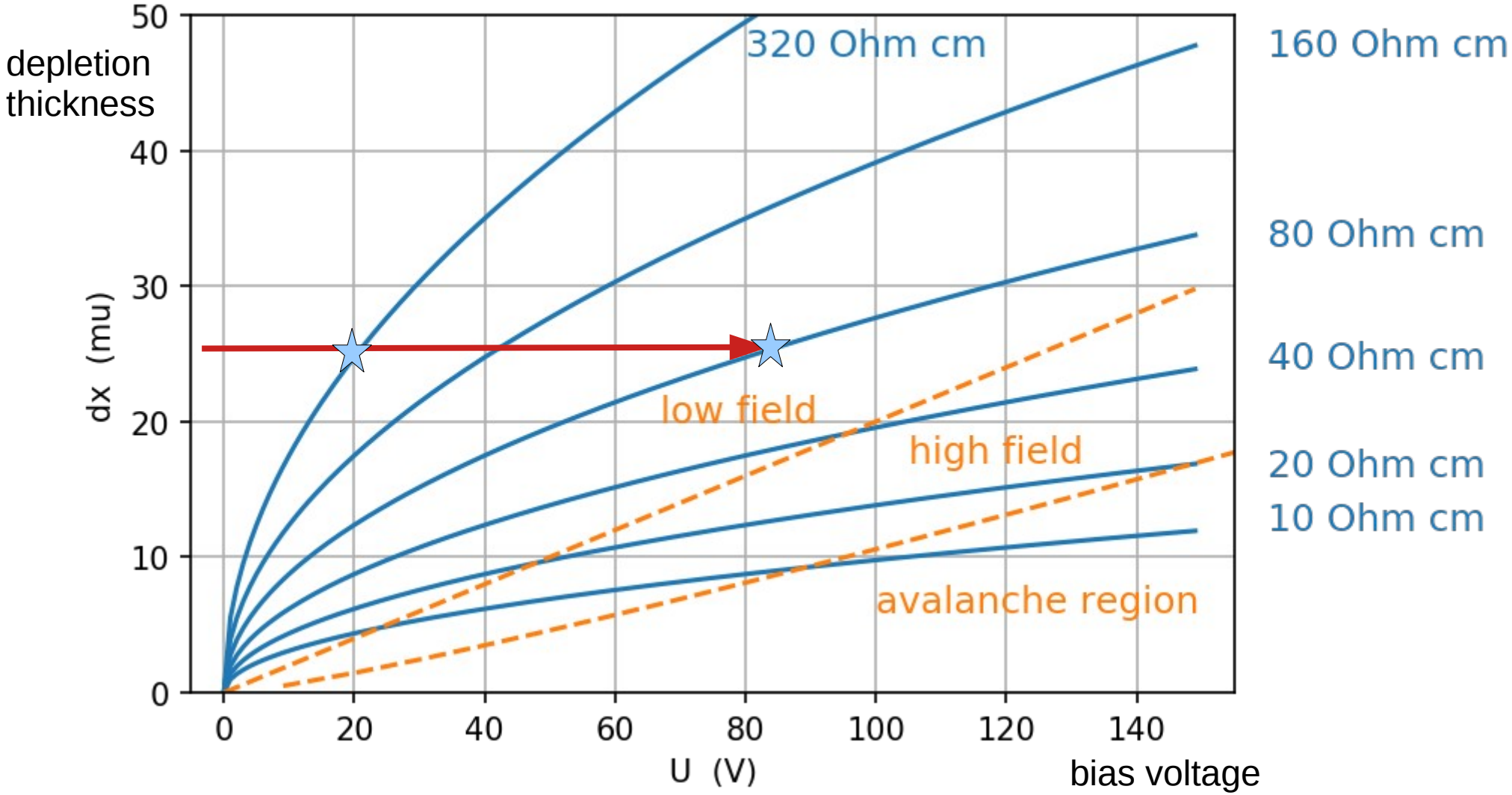
breakdown is at ~110V





- Sensors **thinned to 50 um** allow for only **20-25 V depletion**
- Data are well compatible with a substrate resistivity of **~370 Ohm cm** (nominal 200) assuming that the depletion **touches the back-side**

Depletion and Bias Voltage Relation



- **50 um sensor allows only 25-30 mu depletion**
- **Optimal resistivity is ≥ 80 Ohm cm → full depletion possible @100V**

Mupix10 Optimisations & New Features

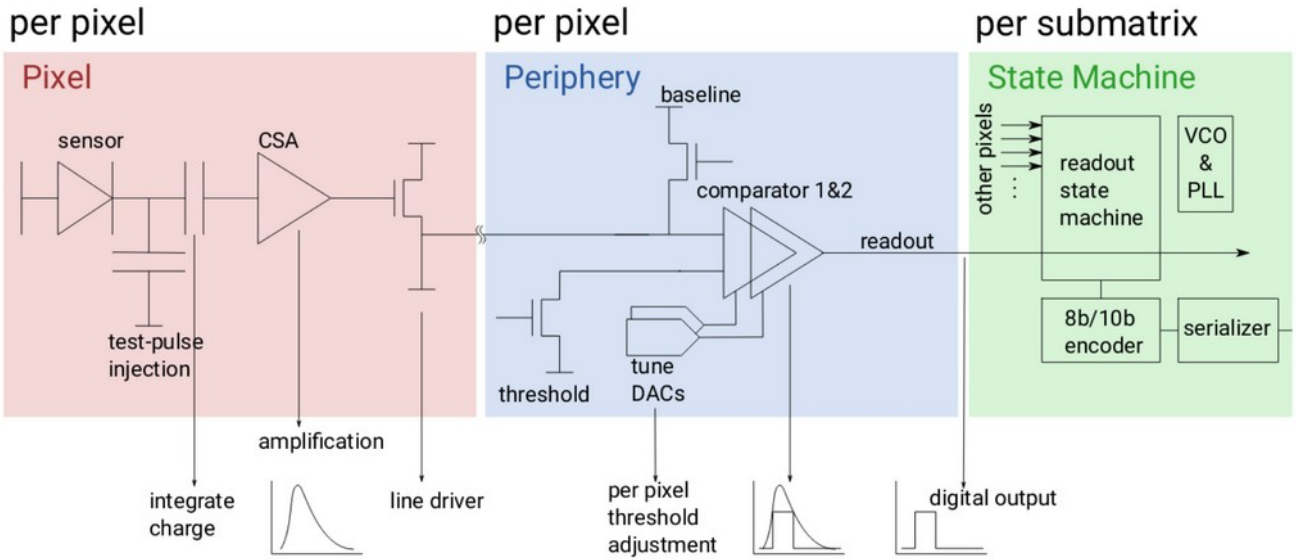
Optimisations wrt. Mupix8

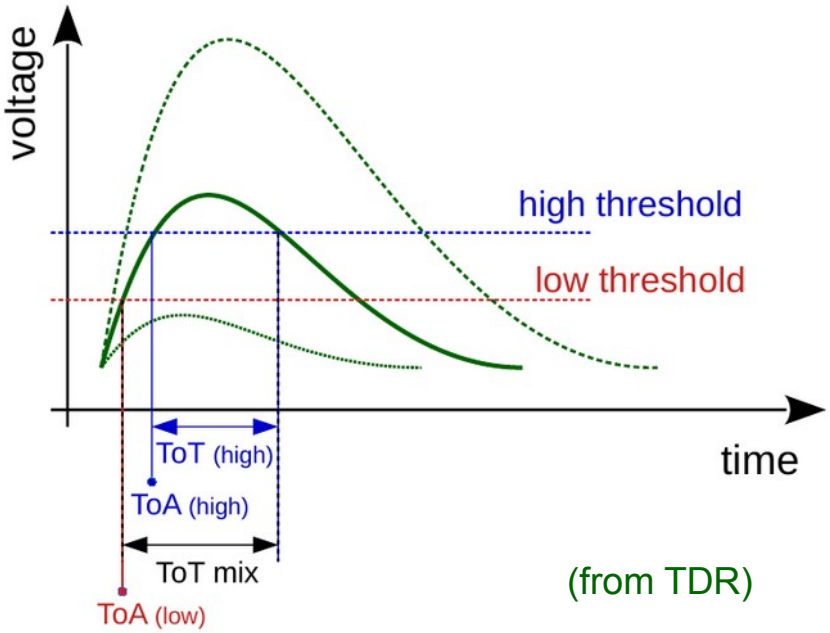
- RO architecture → only NMOS-Amplifier & source follower)
- power net improved
- bonding pads (SpTAB & wire)
- pixel tuning improved
- improved routing of analog signal lines to periphery
- time stamp 10 → 11 bits (ToT bits 6 → 5)
- substrate resistance → 200 Ωcm
- improved two comparator circuit (time-of-arrival & time-over-threshold)
- further improved speed of fast column readout (fast lanes)

New Features

- delay circuit added (for readout)
- voltage regulator for 1.0V (VSSA)
- larger sensor!

2-Comparators





(from TDR)

Motivation of 2-comparator design

- use lower threshold for reducing time walk (ToA)
- use higher threshold for hit validation
- use higher threshold for measuring falling edge more precisely → better ToT

Two methods to measure ToT:

➔ rising and falling edge from high threshold

➔ rising lower edge and falling higher threshold

is it working???

MuPix10 Delay Circuit

Issue:

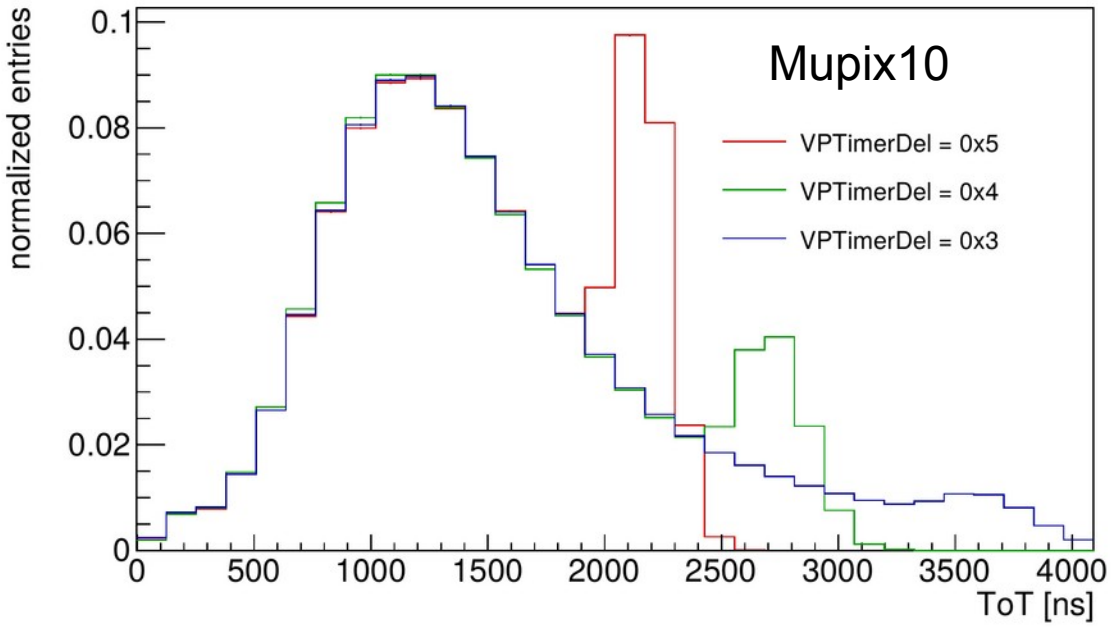
- Hits should be read out after completing of ToT measurement
- ToT measurement depends on pulse height → disturbs chronological order of hits
- solution: read hits after adjustable fixed delay

Challenges:

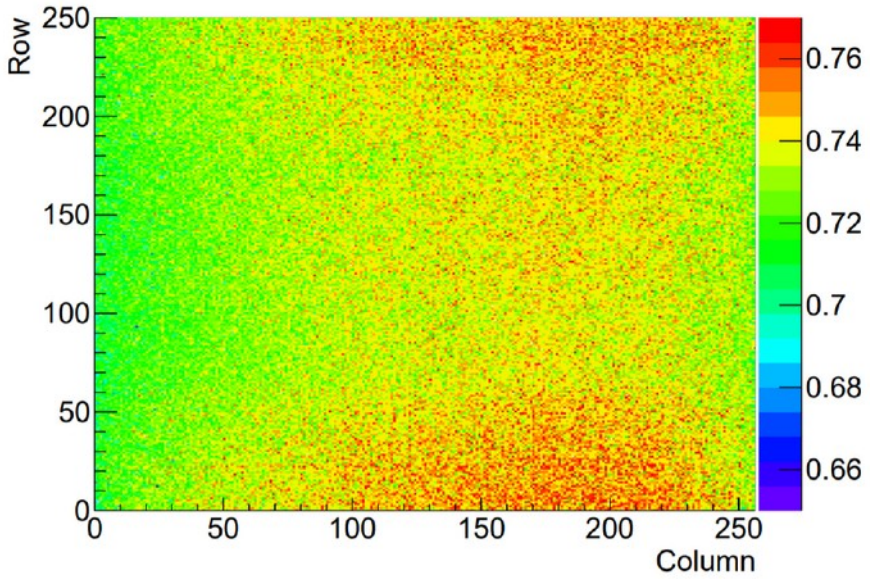
➔ handling of overflows (huge pulses) is required (counter stops)

➔ delay dispersion of pixels should be small

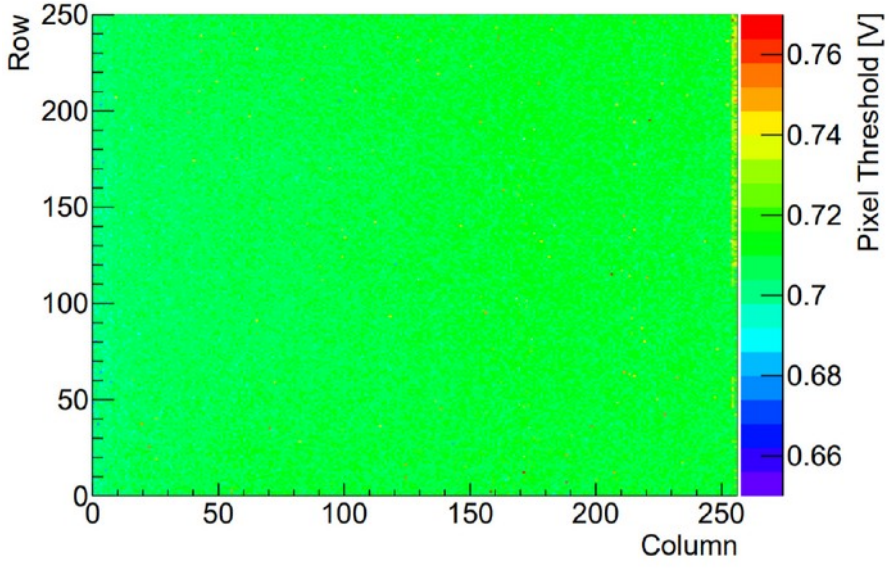
time-over-threshold



Mupix10: Pixel Tuning

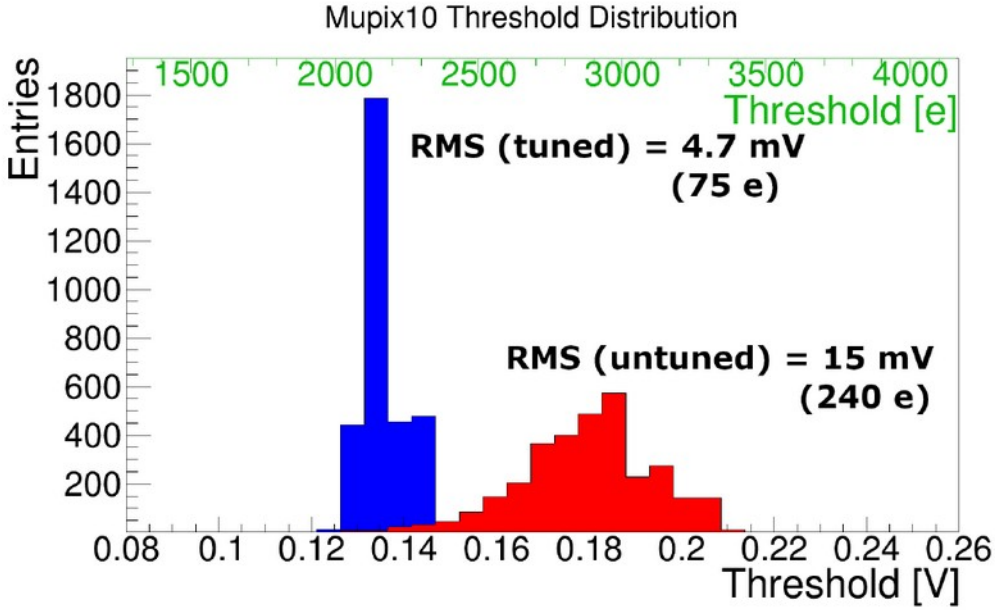


(a) Untuned pixel threshold distribution.



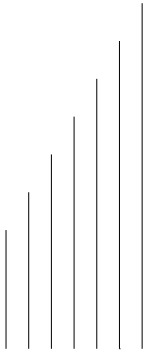
(b) Tuned pixel threshold distribution.

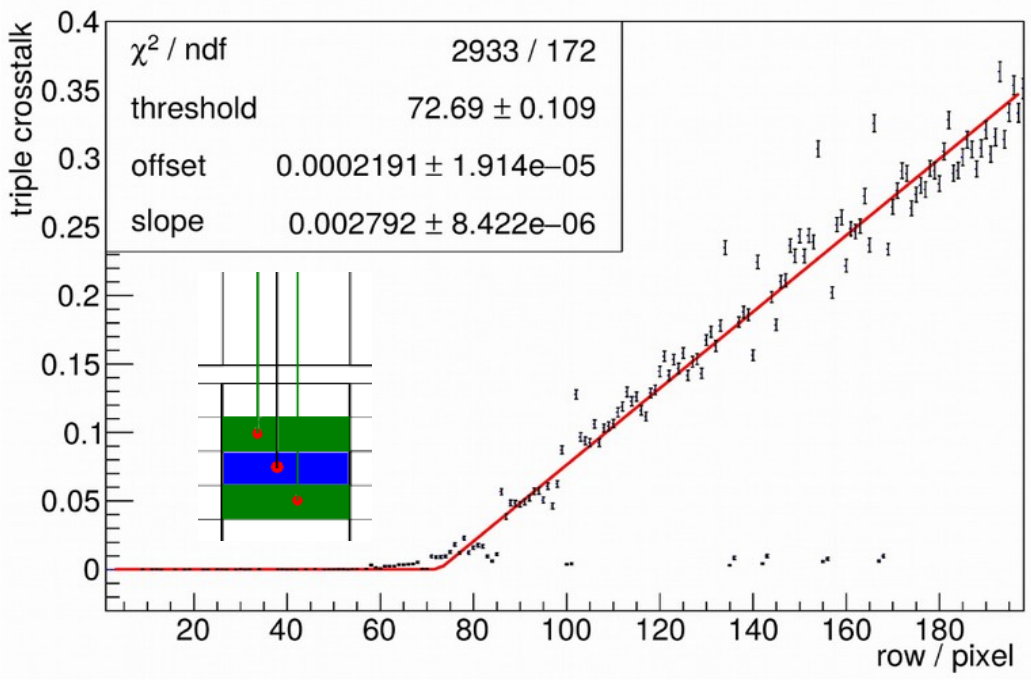
- 3 bit tune dac (TDAC) per pixel
- tune with charge injection
- significant dispersion reduction measured



Mupix10: New Routing of Analog Signal Lines

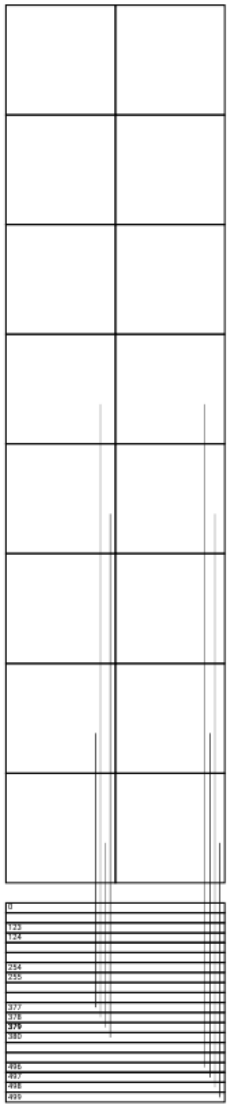
Mupix8 Layout



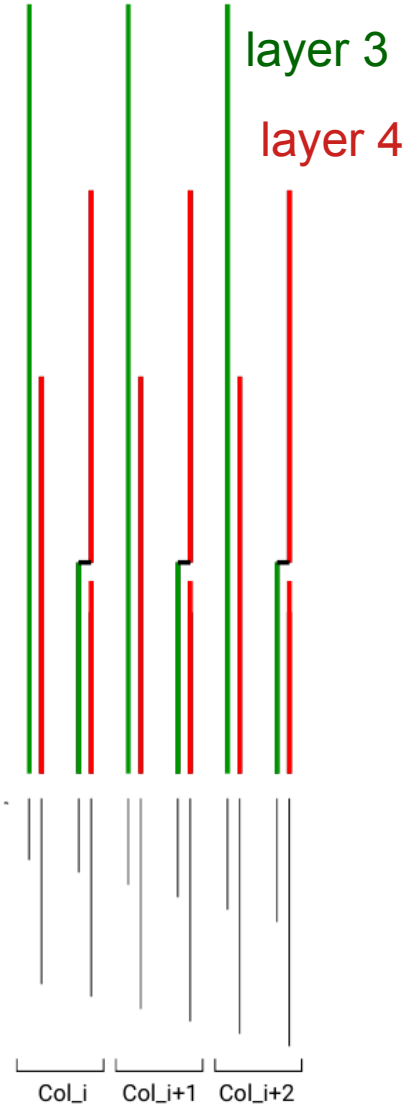


Triple cross talk probability

New Mupix10 Layout



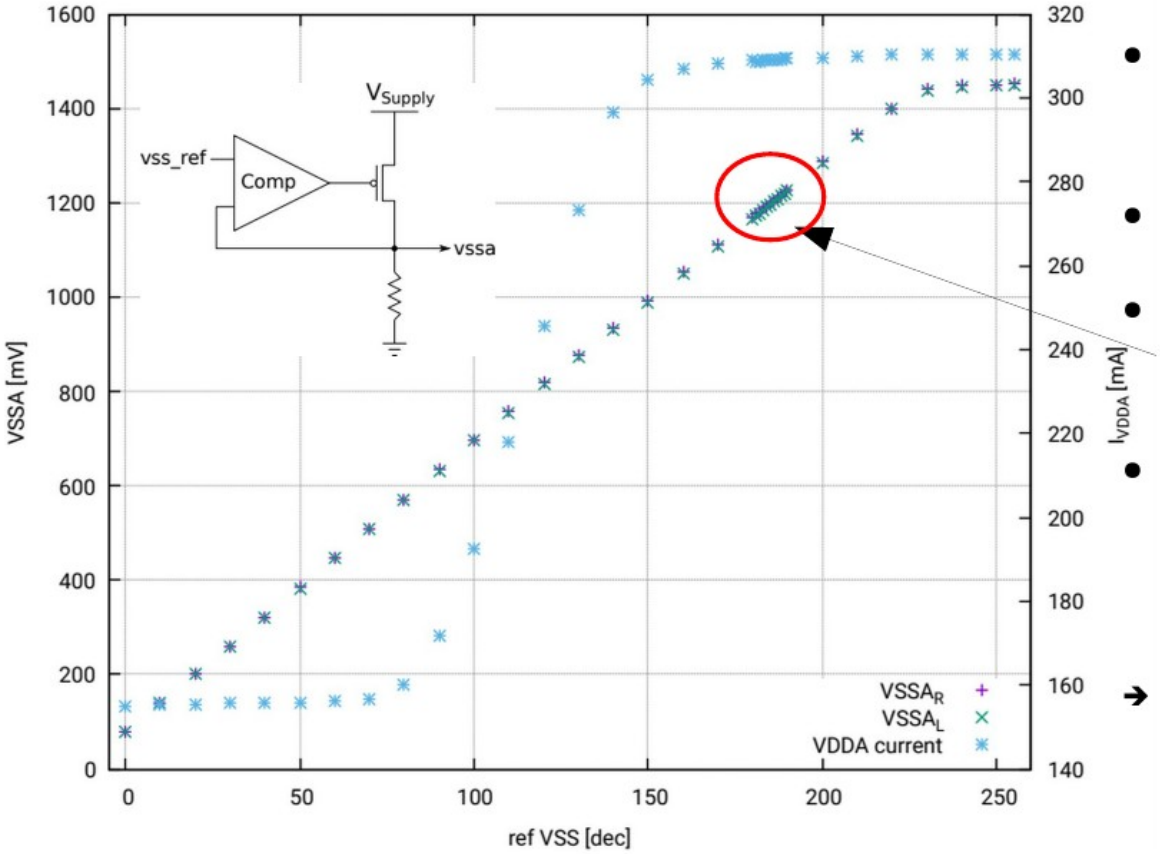
double column



2-metal layers

VSSA Regulator

Vssa-Regulator



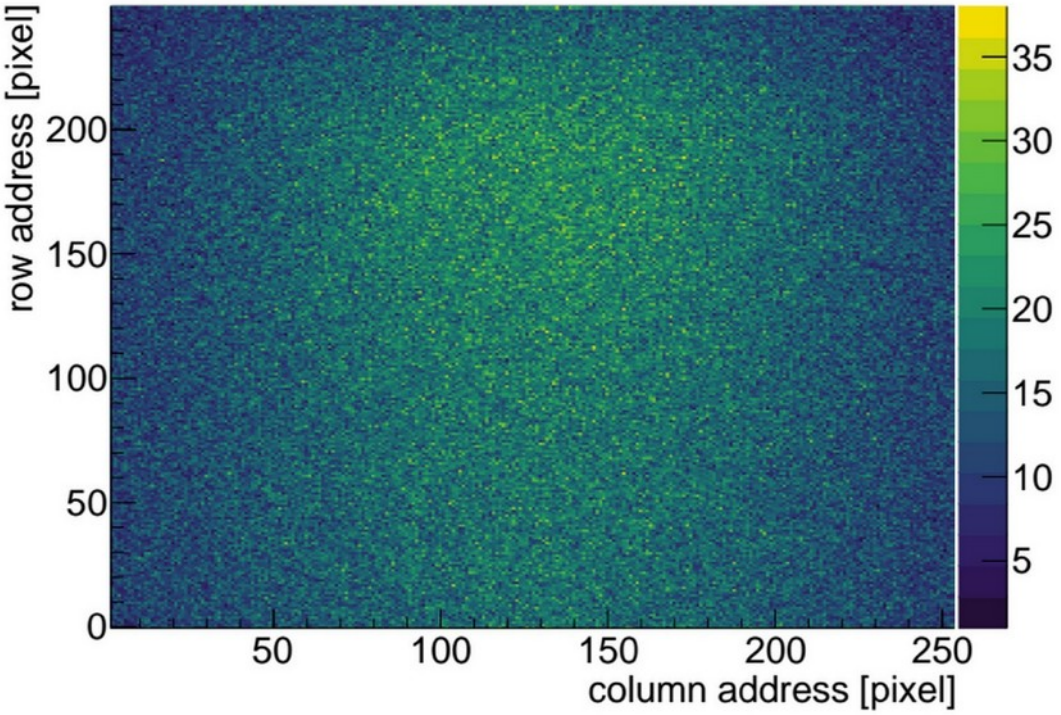
- Integral for module functionality with a single supply voltage
- No detailed study yet
- Dive into the cold water: the regulator works nicely
- Even colder water: MuPix10 was operated successfully with a single supply voltage

➔ Power consumption: ~ 220mW/cm²

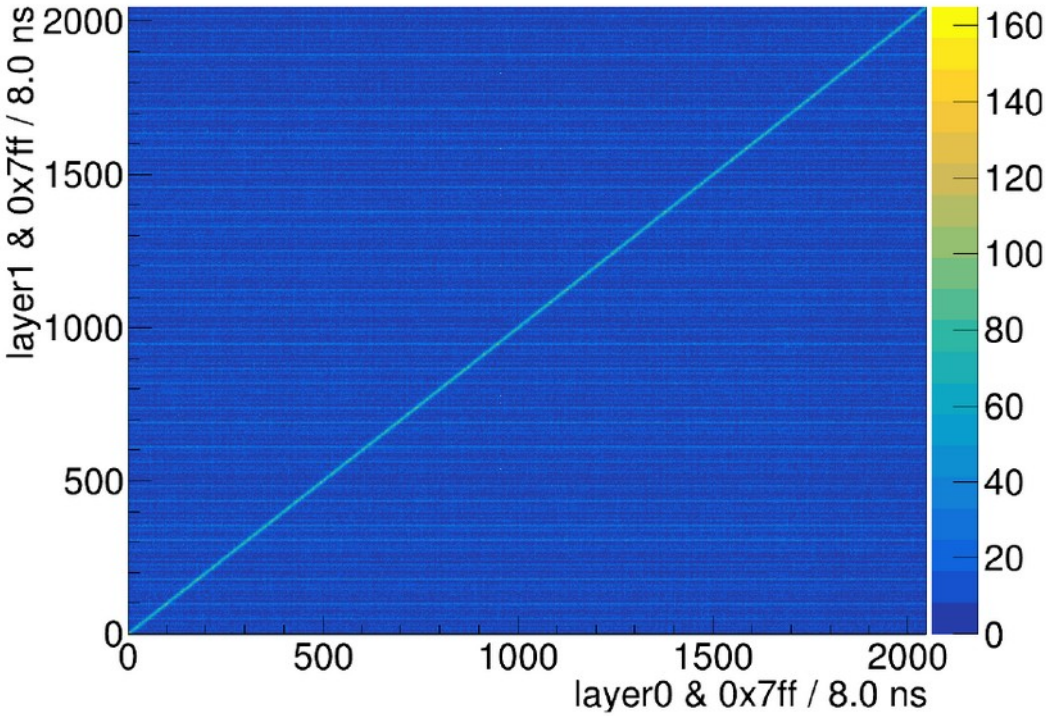
→ slide from Heiko; to be redone

Beam Test Results and Mupix10 Telescope

- telescope: 3+1 (DUT) layers
- DESY & PSI testbeams (despite Corona)
- MuPix works fine in general!



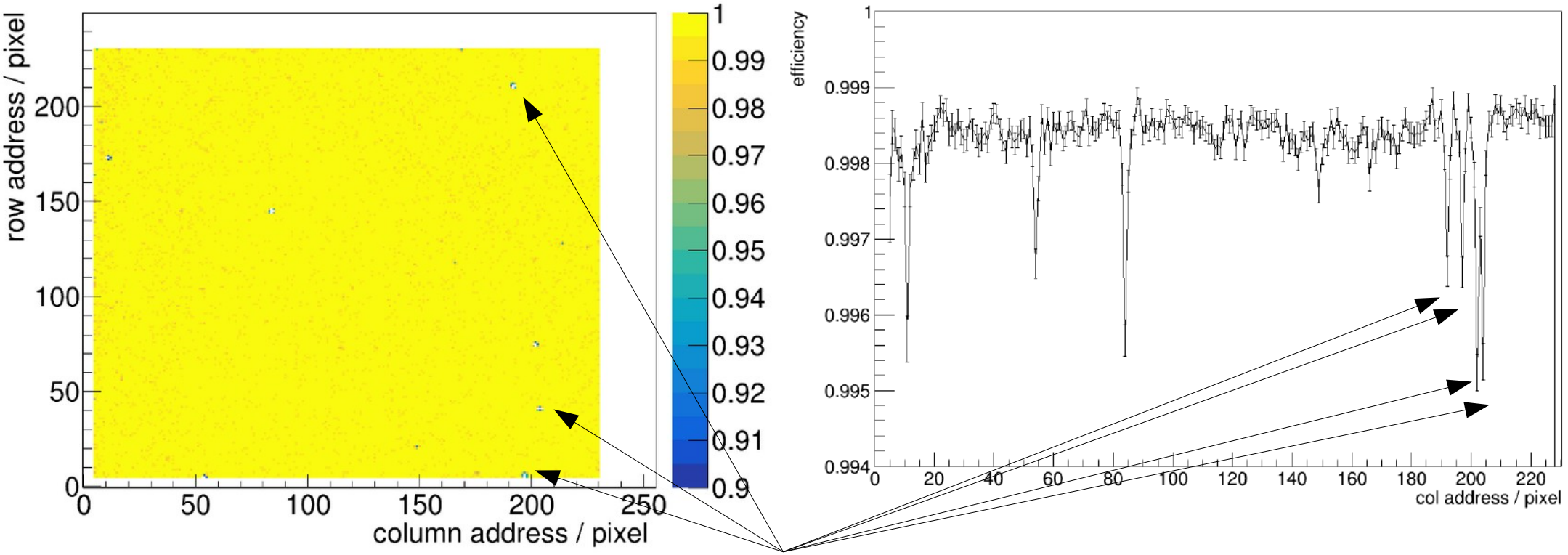
Hit map (electrons @DESY)



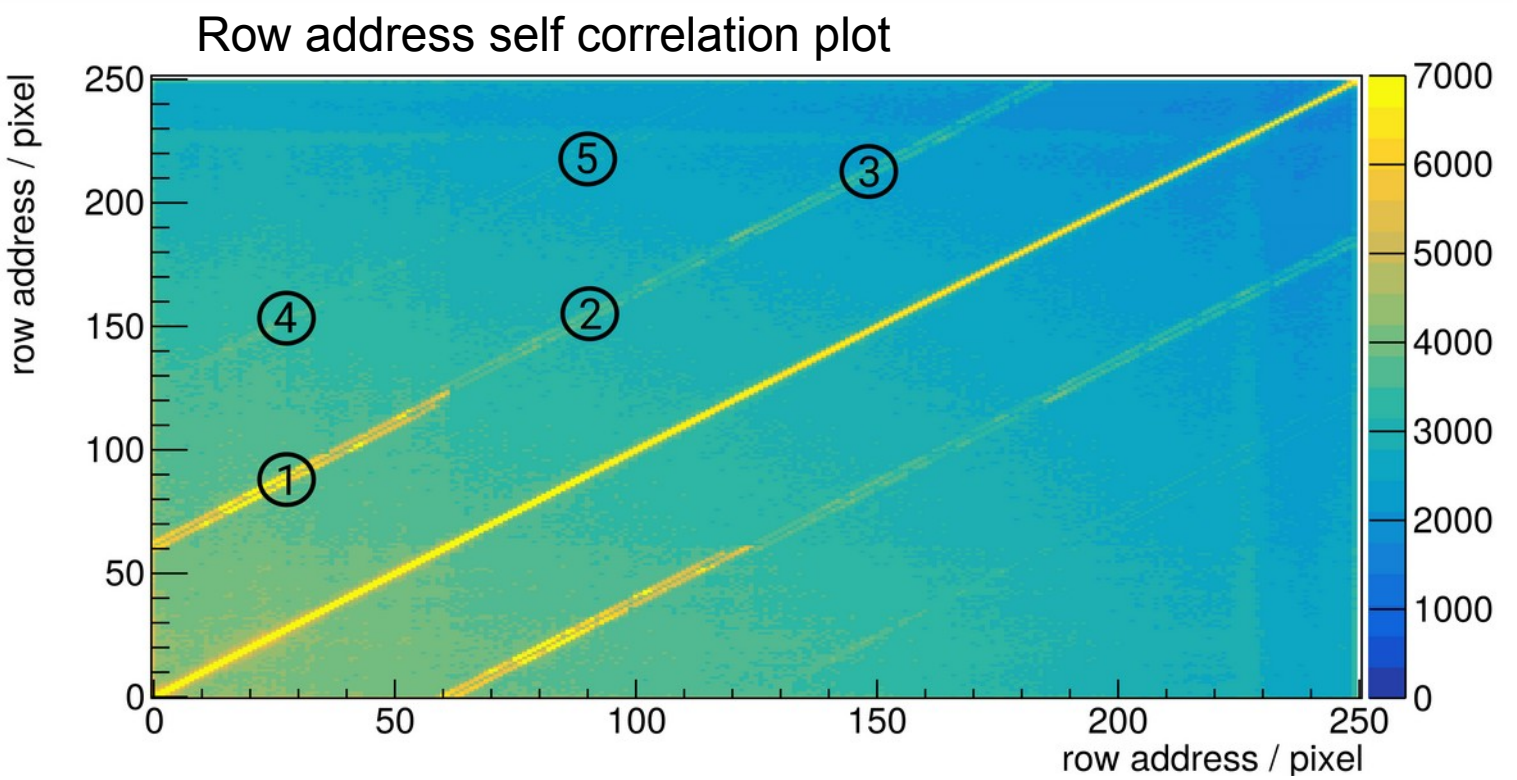
Time correlation between layers (PSI)

Mupix10 Efficiency (PSI)

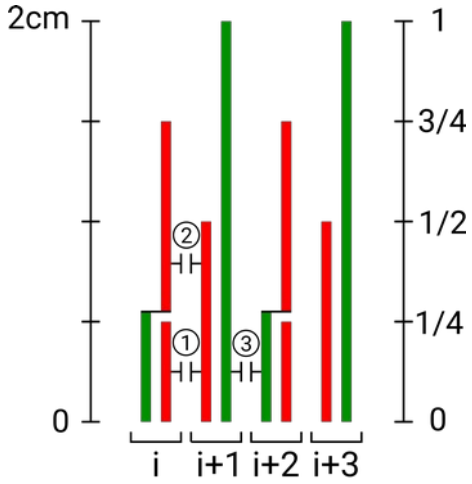
- threshold 42mV (~670 e^-)
- average efficiency ~ 99.85% (noise & rate dependent → dead time)
- no pixels masked!
- no TDAC tuning of individual pixels
- O(10) noisy pixel out of 64000 → lead to deadtime losses



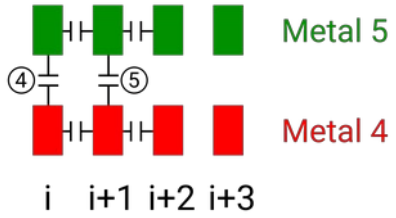
Cross Talk between Analog RO Lines



MuPix10 routing pattern



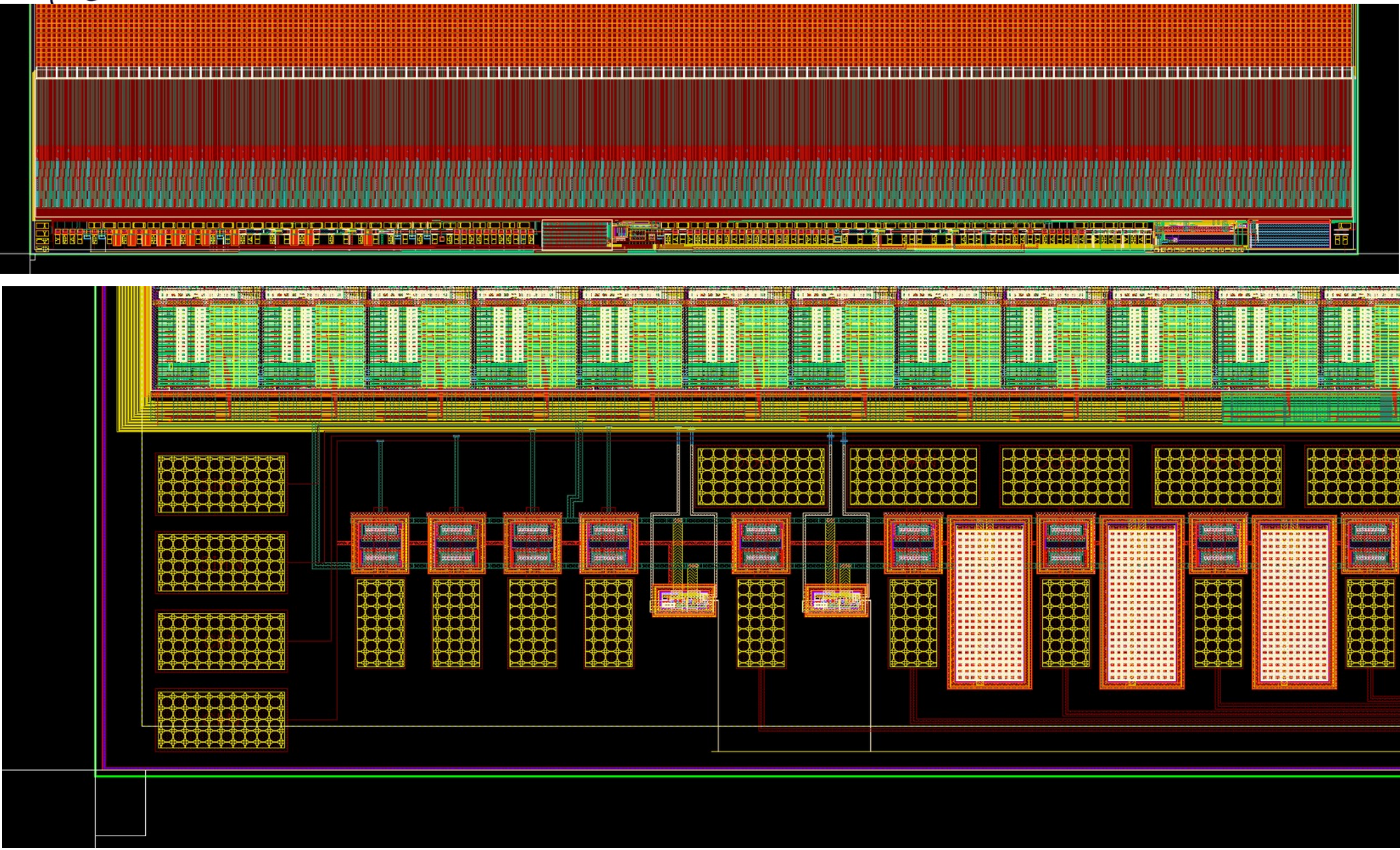
Top view



Cross section

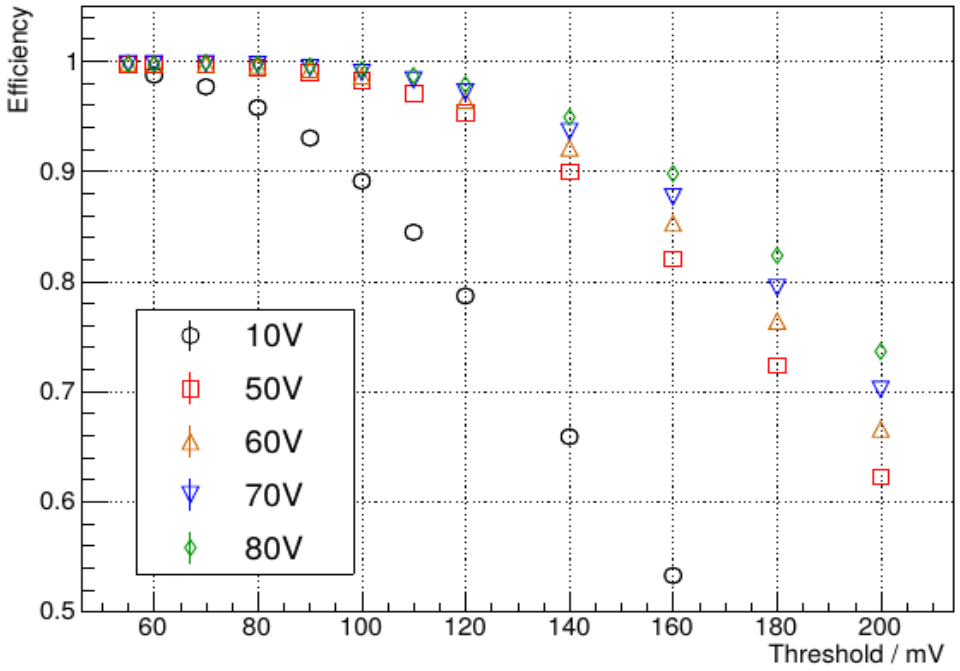
Mupix10 integrated cross talk probability less than 1.5 % (Mupix8 ~12%)

Mupix10 Periphery + Pads

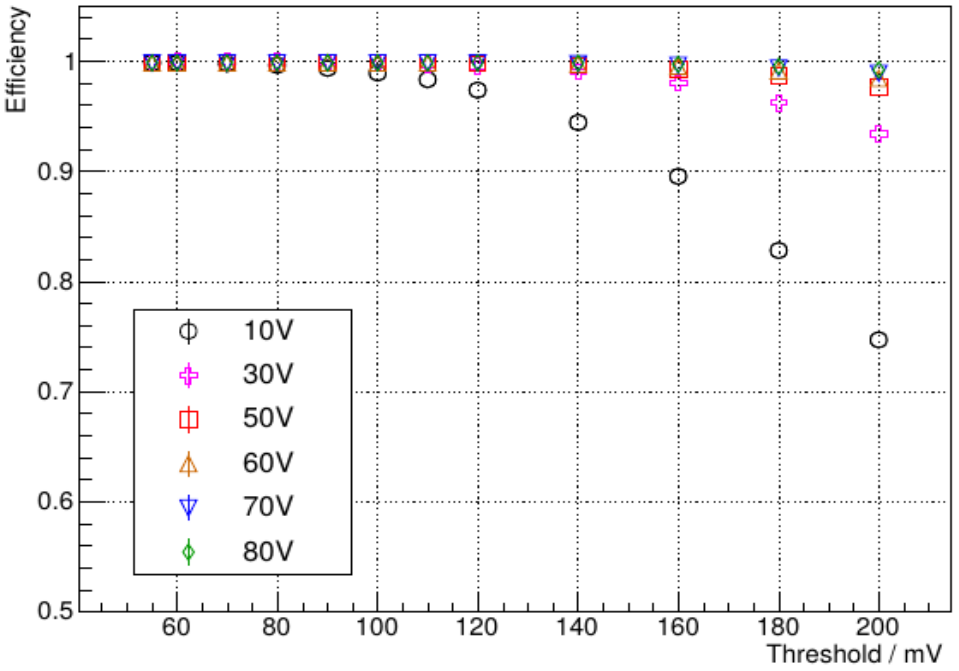


Substrate Resistivity Dependence ATLASpix1

80 Ω cm



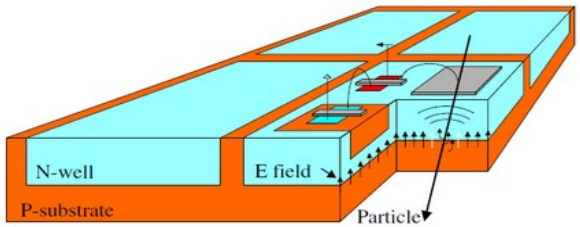
200 Ω cm

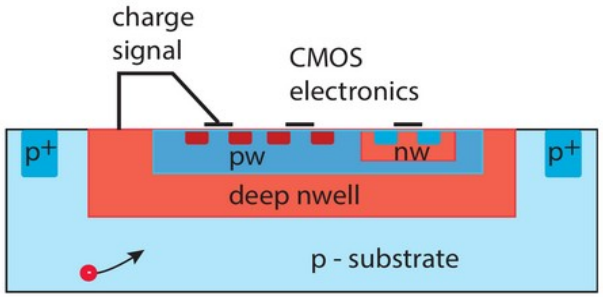


significant larger depletion with higher resistivity!

HV-MAPS Prototypes - History

I. Peric et al (2007)





Mupix7 was the first small scale prototype integrating all relevant features of a **fully monolithic chip** (VCO, PLL, state machine, ...)

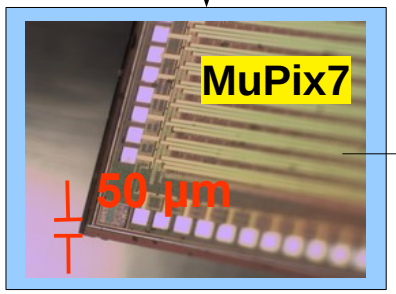
Mu3e-Experiment

MuPix1

MuPix2

.....

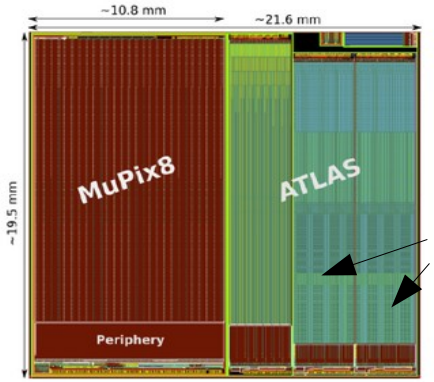
MuPix6



AMS H18 (IBM)

Mu3e & ATLAS (HL-LHC)

AMS AH18



Mupix9

ATLASpix2

TSI H18

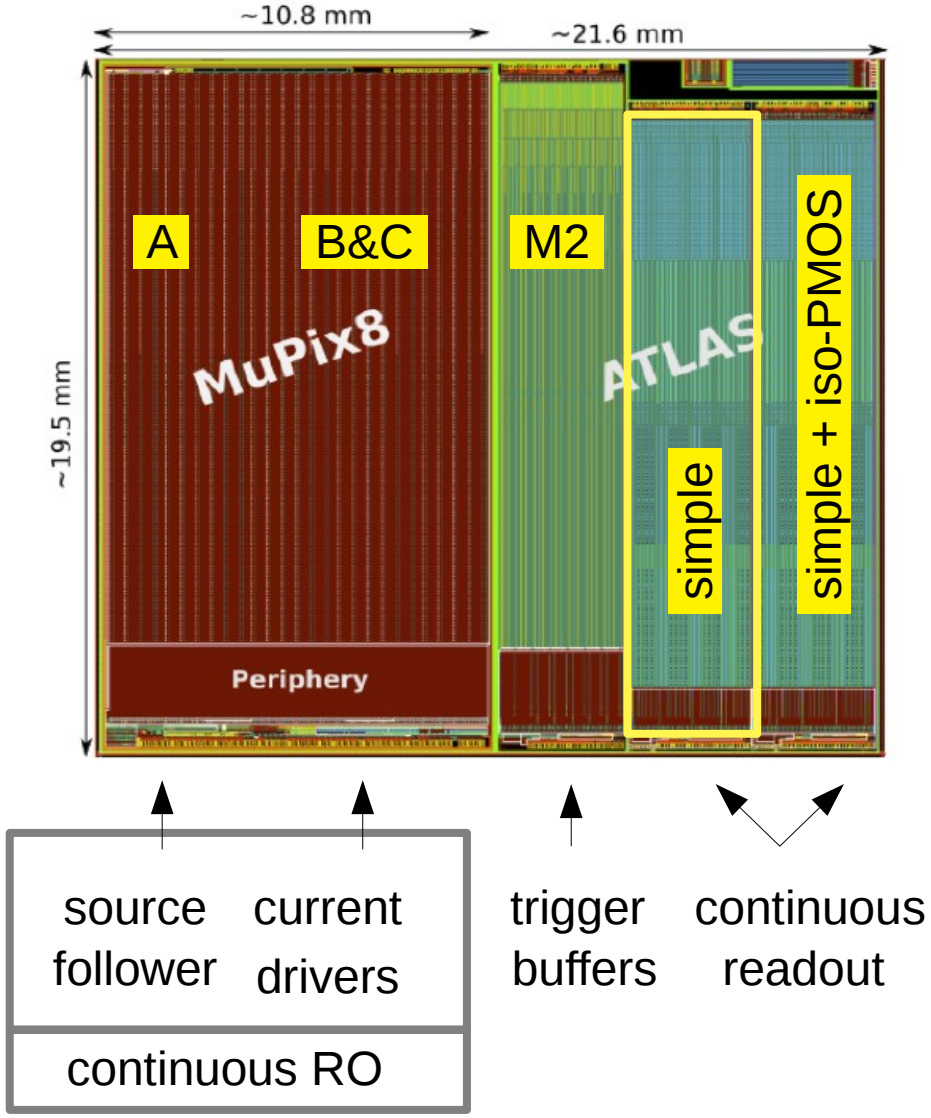
Mar 2020

Sep 2019

MuPix8 & ATLASpix1

Mupix8

- pixel: 80 x 81 µm²
- 200 rows x 48 cols
- amplifier in pixel cell
- **discriminators in periphery**
- 6 bit ToT
- state machine
- serial link up to 1.6 Gbit/s



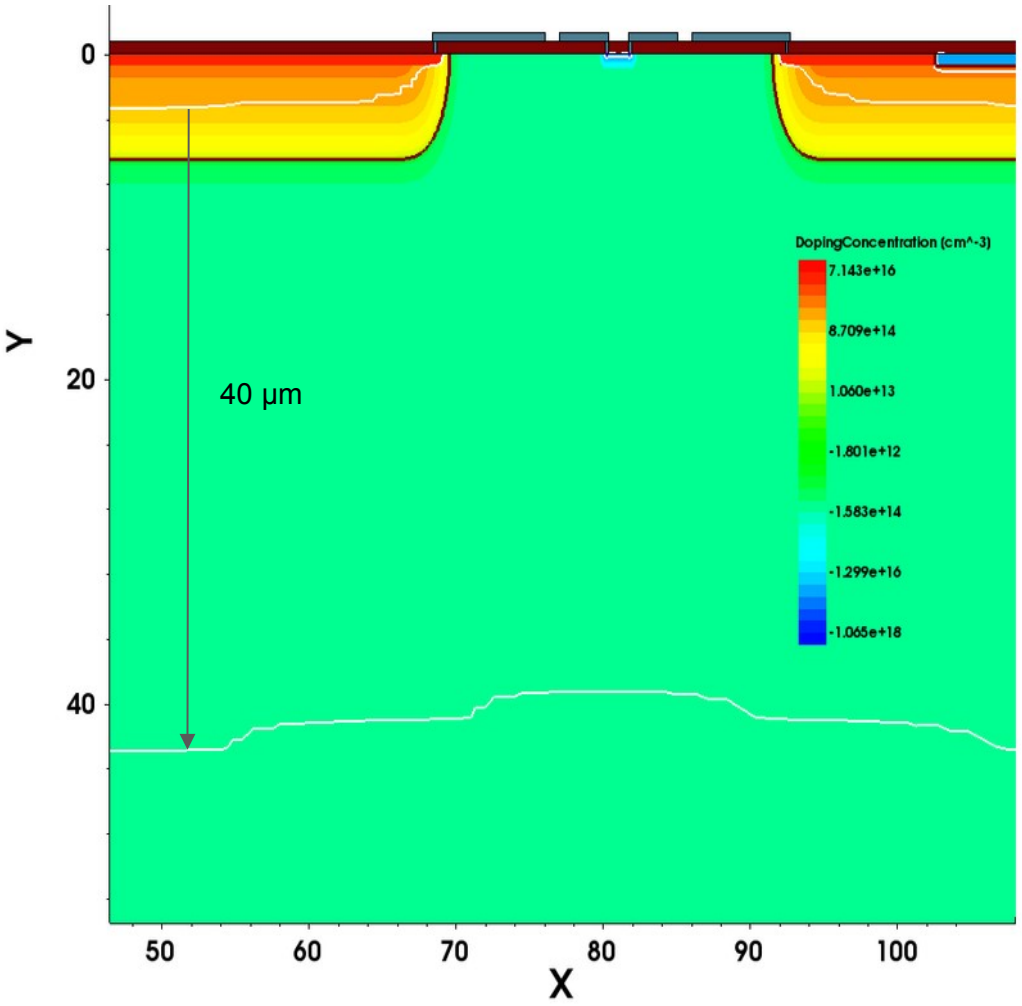
ATLASpix

- pixel: 40 x 130 µm²
- 400 rows x 25 cols
- amplifier in pixel cell
- **discriminators in active pixel cell**
- 6 bit ToT
- state machine
- serial link up to 1.6 Gbit/s

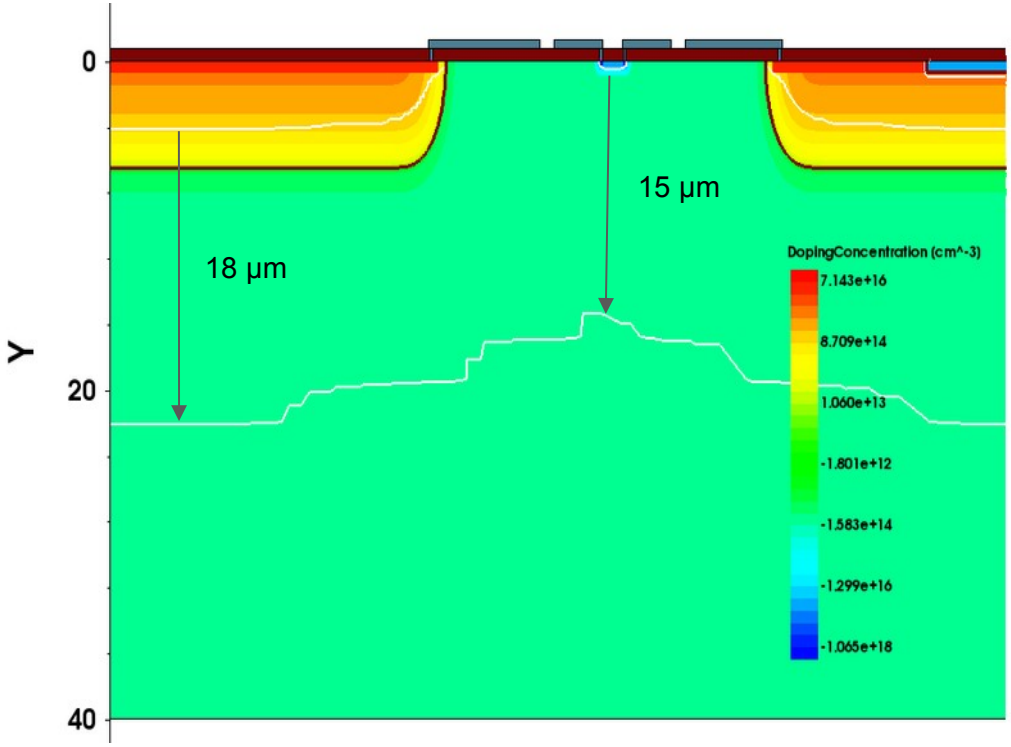
Both discriminator readout architectures are candidate for Mu3e!

TCAD simulations: Doping

HV =-100 V

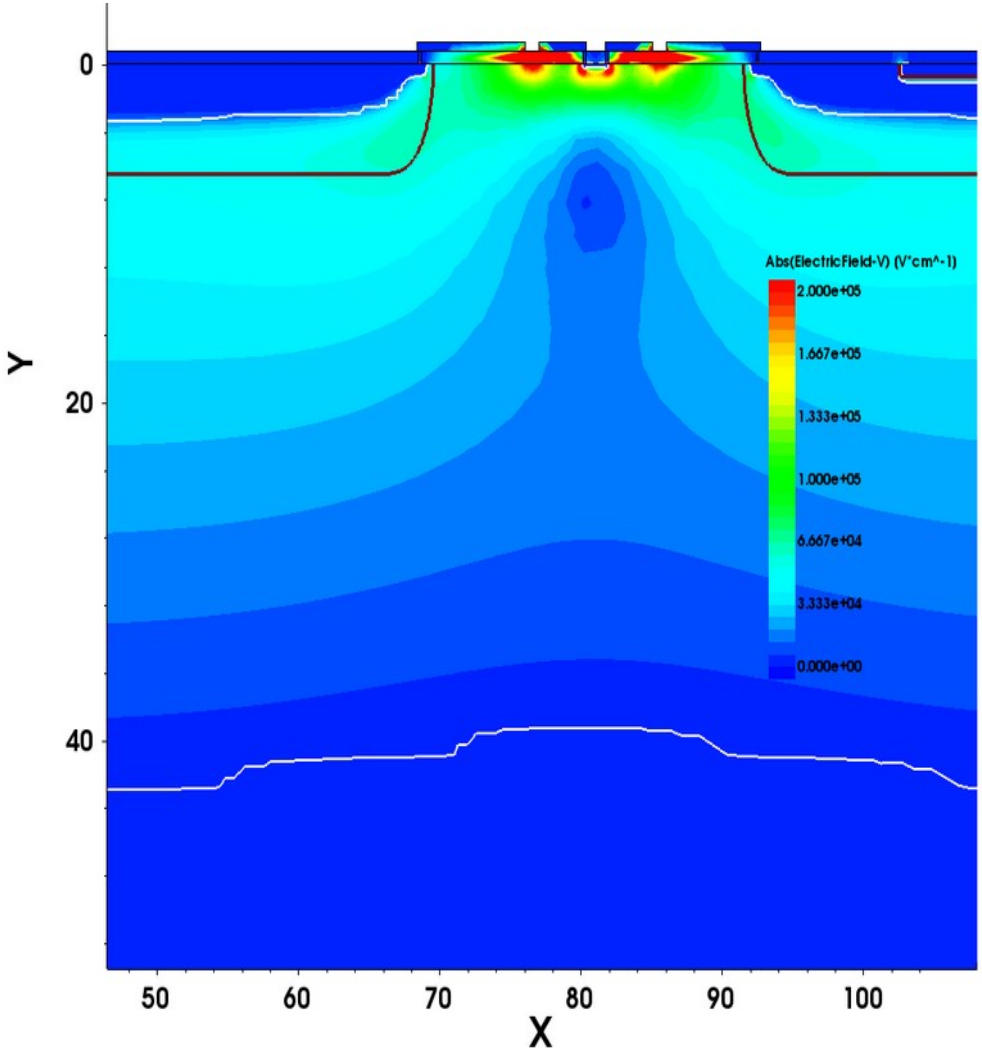


HV =20 V

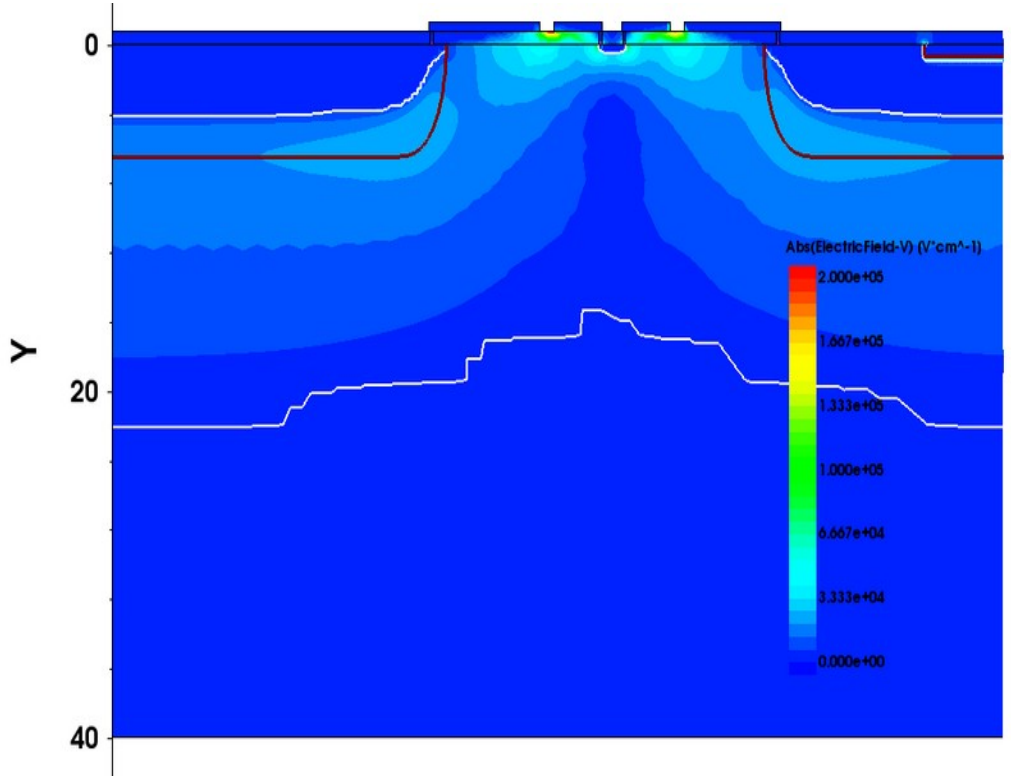


TCAD simulations: Field

HV =-100 V



HV =20 V



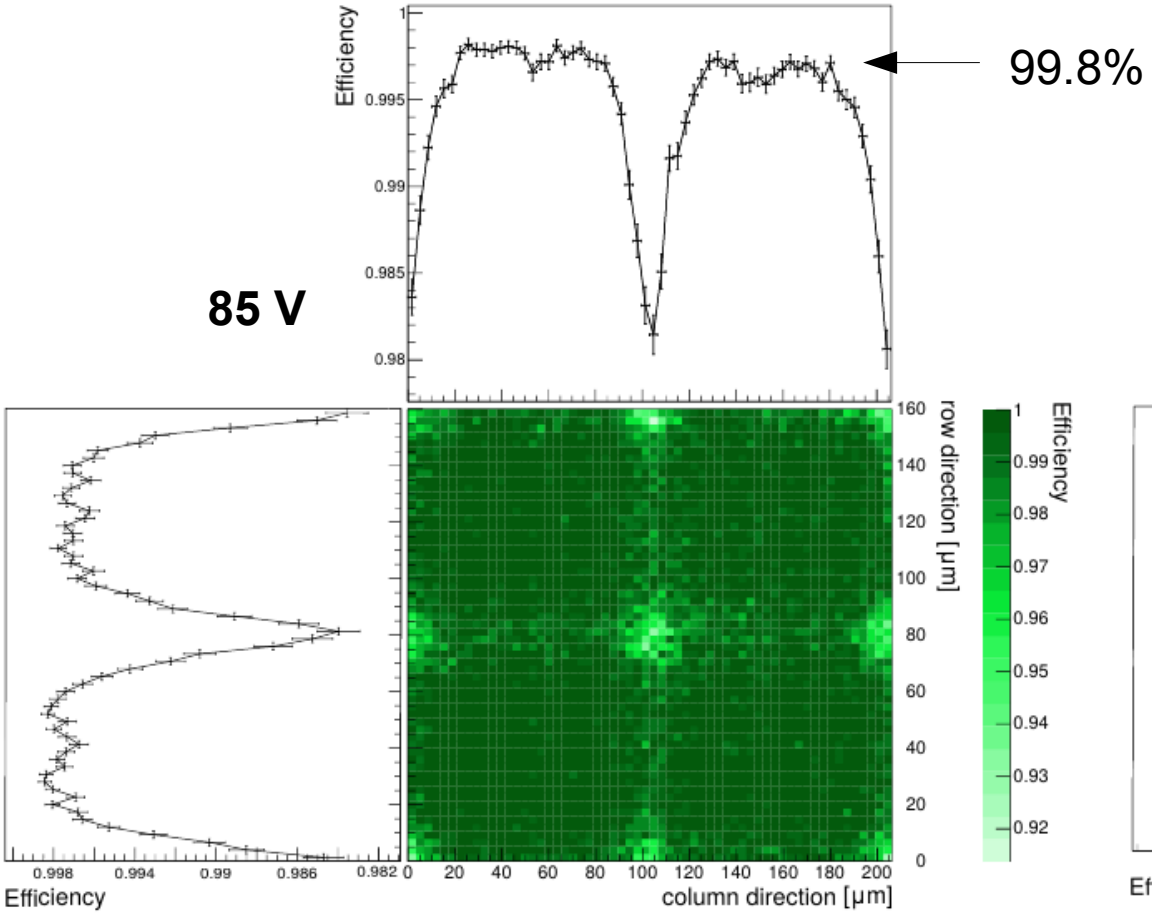
red=$2 \cdot 10^5$ V/cm

green=$1 \cdot 10^5$ V/cm

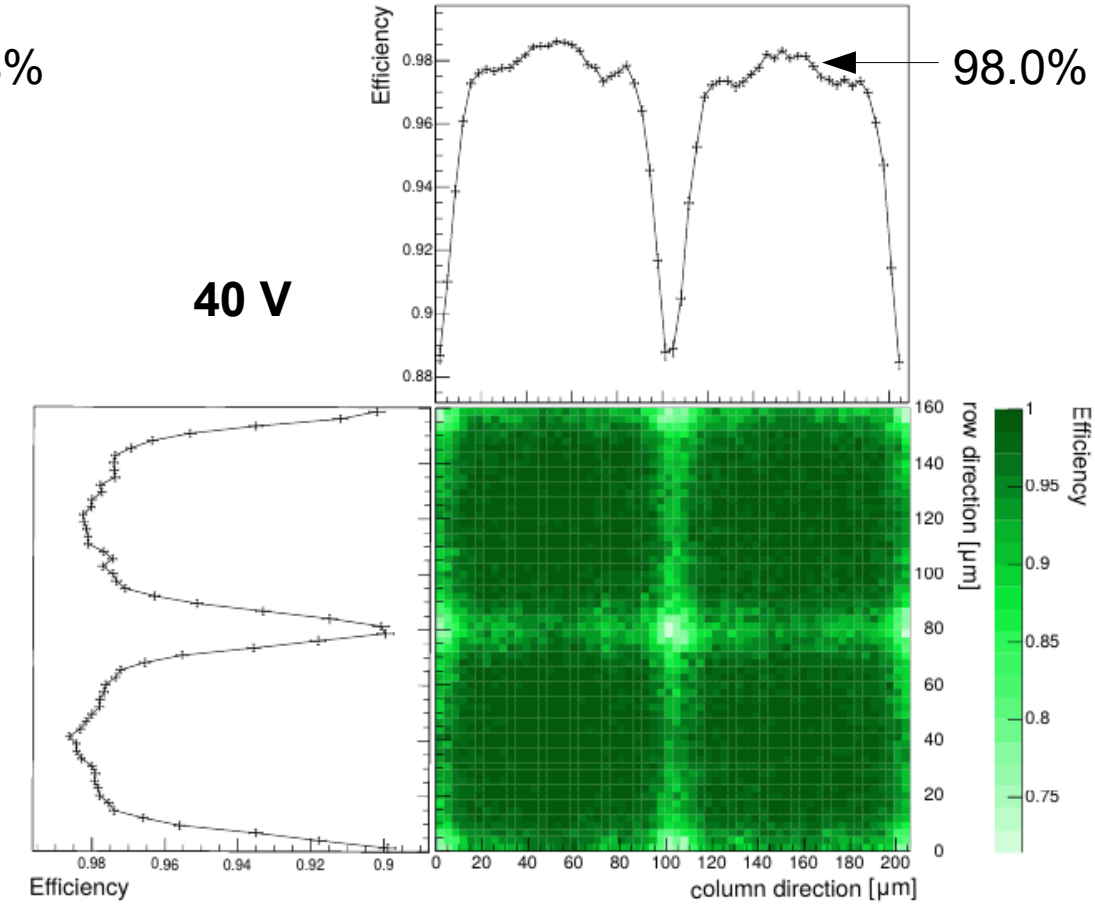
2x2 Subpixel Efficiency MuPix7

- 20 Ohm cm
- 64 um thickness

85 V



40 V



depletion depth ~ 13 um

depletion depth ~ 9 um