# On-detector electronic circuits

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#### Overview: lines per half-ladder

- LV power (1.8-2 V)
- GND
- HV (20-120 V)
- Data -> 9 LVDS lines
- Clock -> 1 LVDS line
- Sync Reset -> 1 LVDS line
- Serial Input ->1 LVDS line
  - Not needed in Mupix10
- SPI lines (single ended, Mupix10 only)
  - 1 Chip Select per chip
  - 1 SPI clock
  - 1 SPI MOSI

3 DC lines + 11 LVDS lines Baseline (Mupix11)

> 3 DC lines + 11 LVDS lines + 5 single ended lines Mupix10 6-chip ladders

Inner layer design



Inner layer design



Inner layer design (no SPI lines)

#### **Bottom layer**



Inner layer design (no SPI lines)



Inner layer design (with SPI lines)



Inner layer design (with SPI lines)



# Mupix10 HDI to interposer

Inner layer design (no SPI lines)





#### Interposer flex

Sense line routing towards the middle



#### **Intermediate layer**

#### Interposer flex



#### **Top layer**

#### Interposer flex

Sense line routing towards the middle



#### **Intermediate layer**



# Interposer flex: summary

- Routing of lines from HDI to End-ring flex
- 1 per half ladder
- Copper design
- SwissPCB production
- Multi-layered
- Design for inner layers to be finalized
  - The presented one is old, must be updated

# End-ring flex

- Routing from interposers to BoSSL
- 1 per DAQ module (-> half a mechanics module)

It should be wrapped around the End-rings

Design not started

Size and physical constraints need to be verified in in-person mechanics meeting of Nov. 24 in HD



# End-ring flex

- Routing from interposers to BoSSL
- 1 per DAQ module (-> half a mechanics module)

It should be wrapped around the End-rings

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# End-ring flex

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- 1 per DAQ module (-> half a mechanics module)

It should be wrapped around the End-rings

Design not started

Size and physical constraints need to be verified in in-person mechanics meeting of Nov. 24 in HD



# BoSSL

- From End-ring flex through interposer to external cables
- Produced
- Must be verified
  - Tests with micro-twisted pair cables foreseen
  - Placement verified at the in-person meeting on 24 Nov in HD

# Conclusions

- For the routing of the signals we need (custom design):
  - Ladder HDI
  - Interposer flex
  - End-ring flex
  - BoSSL board or similar
- Status for inner layers:
  - Ladder HDI:
    - Design finished for Mupix11
    - Produced for Mupix10, to be tested
  - Interposer flex
    - Design started
  - $\circ \quad \text{End-ring flex} \quad$ 
    - Design to start (verify space constraints)
  - BoSSL
    - Produced