Mini DAQ for Detector QA

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November 16th 2021

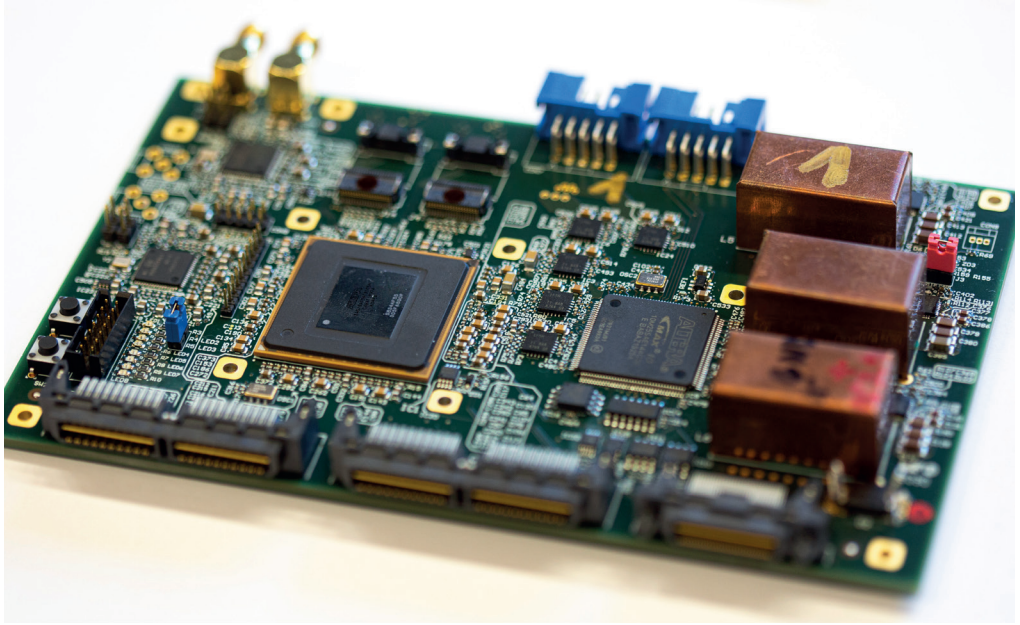
Idea for test systems

Use subsets of the final DAQ hard-, firm- and software

- Easy re-use of components
- Easy to profit from other developments, minimize duplications
- Quality control
- Portability

- Sometimes slightly steeper learning curve
- Will leave behind parts of the beloved, venerable and sometimes kludgy MuPix telescope history

Basic building blocks



Front-end board

- Electrical to optical transition
- Arria V FPGA
- ~20 boards available
- ~60 boards by Q3 2022
- More whenever we get the remaining FPGAs

Receiving board

- Optical to PCIe transition
- Arria X FPGA
- ~12 boards available, can be bought at Terasic (DDR3 and DDR4 variants)

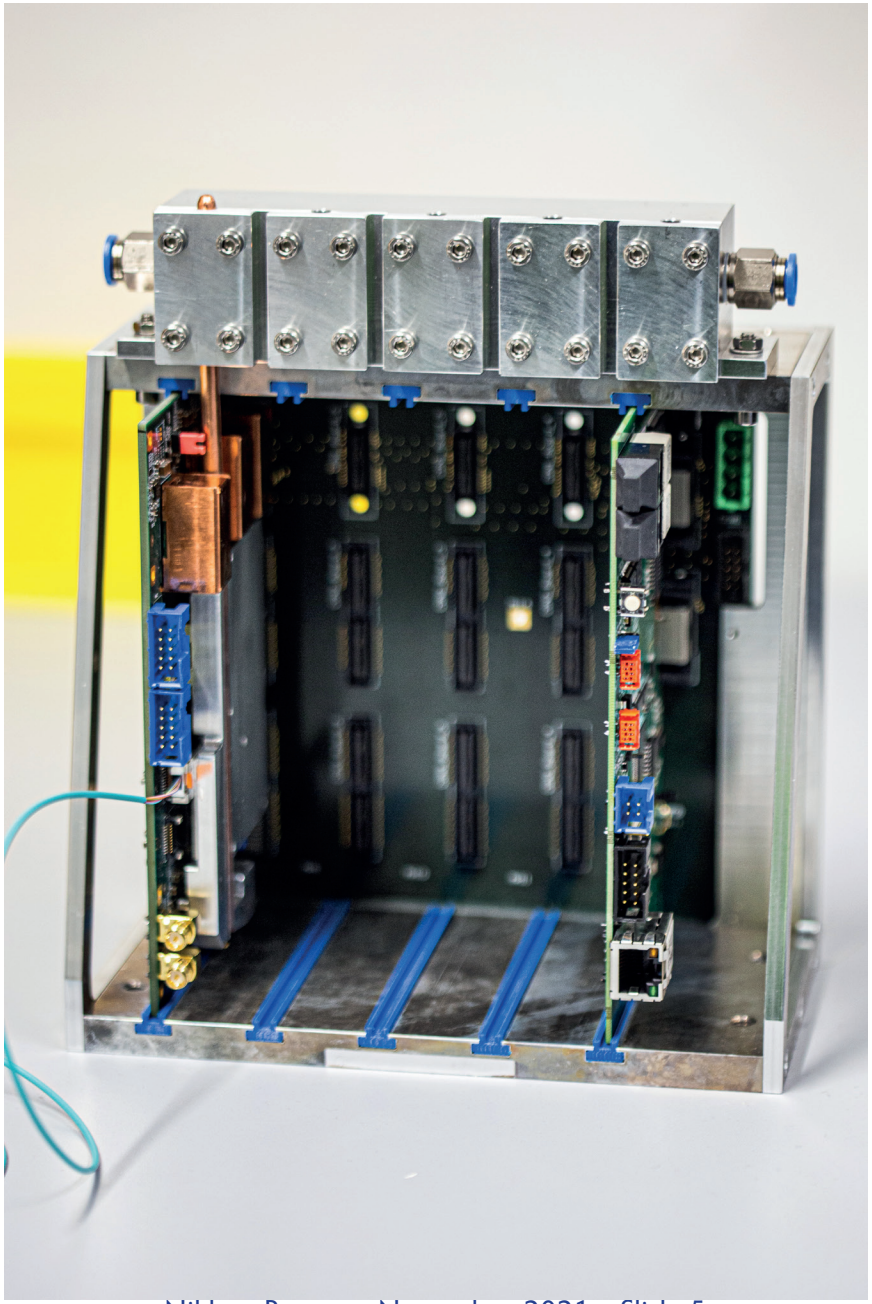
Other ingredients needed

- A Firefly transceiver (comes with the FEB) Either needs a fan or a cooling plate
- A QSFP+ transceiver for the receiving board
- A MTP cable and an MTP adapter. Types depending on Firely type - please inquire
- Si5433 eval board (others also possible) for clocking, plus 3 SMA cables, plus Windows PC for programming
  (we try to get rid of that)
- JTAG Programming cable for the FEB
- Linux PC with root access and a PCIe x8 slot for the receiving board
- Intel Quartus software, ideally with a license (FPGA programming is possible without)
- See also https://bitbucket.org/mu3e/online/wiki/Minimal%20slow%20control%20testing%20setup

Running FEBs

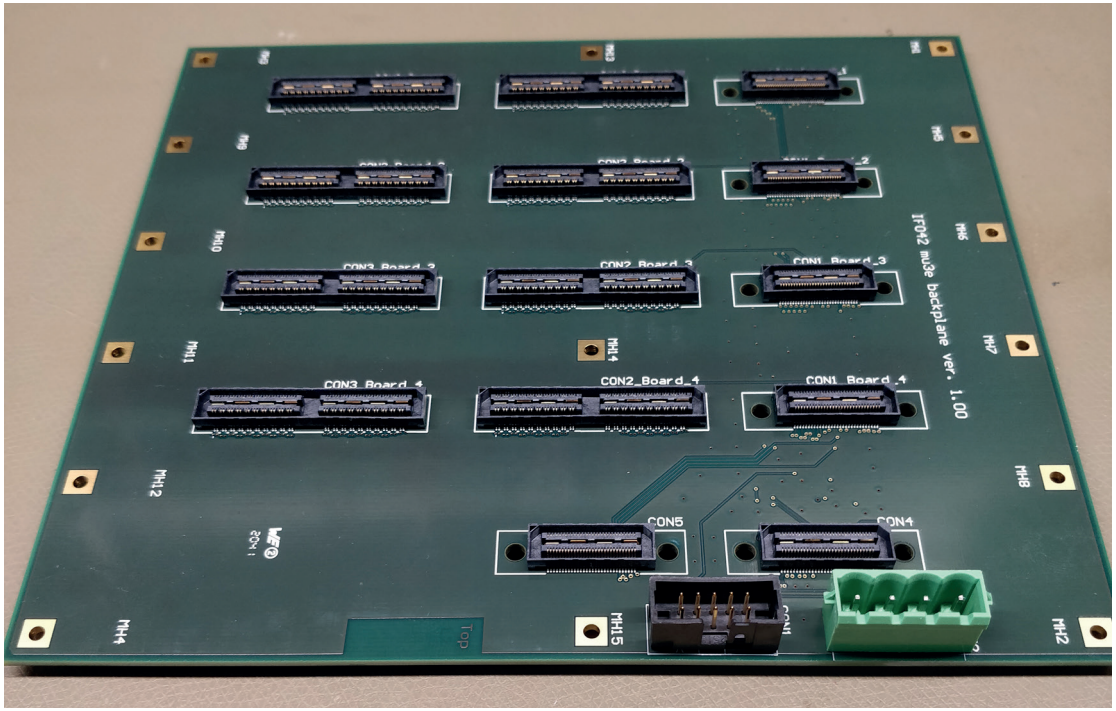
- Can run FEB and Firefly standalone on a table (heatsink on the FPGA and a fan)
- Power: 12-20 V from lab supply

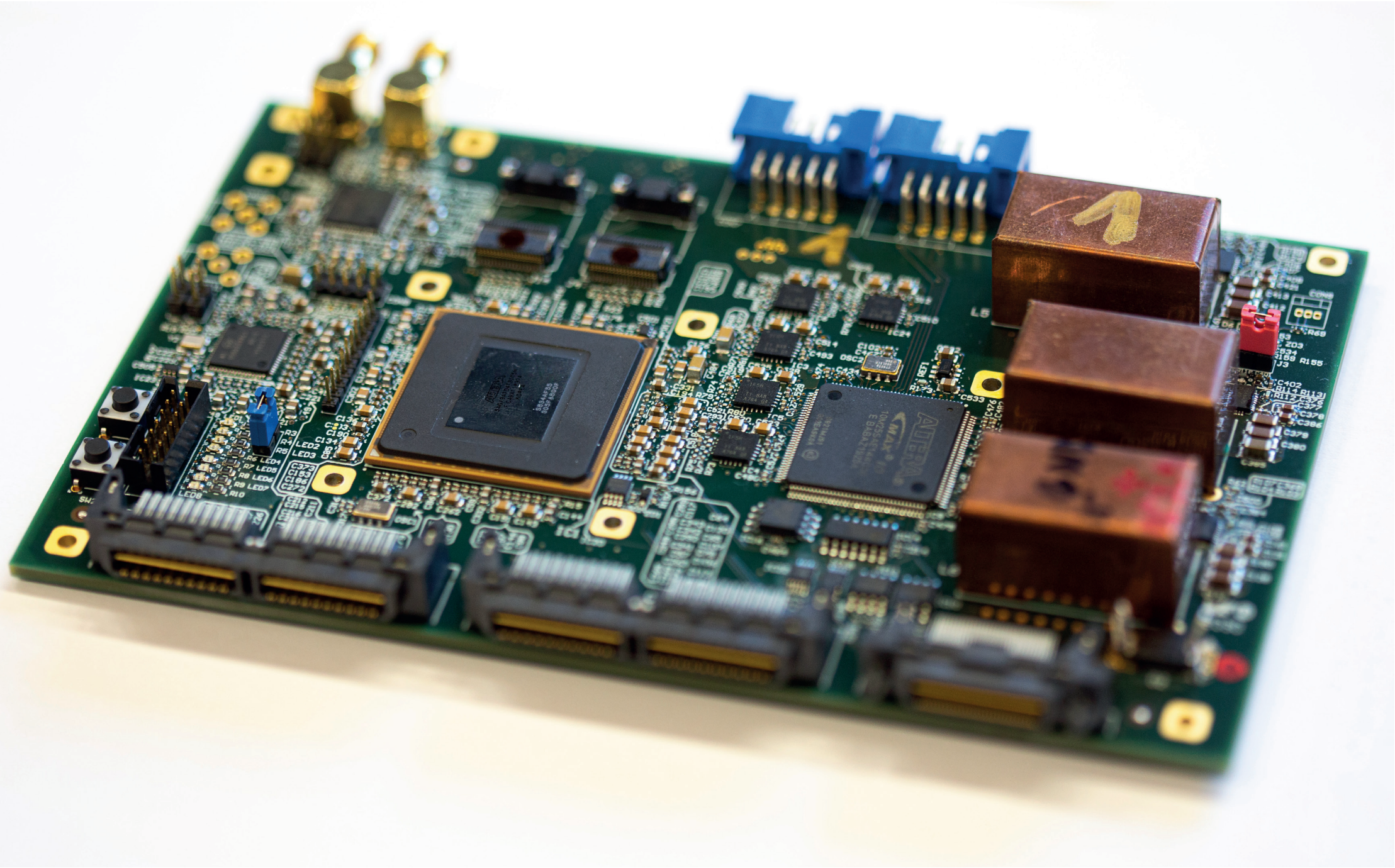
- Nicer: Use FEB with cooling plate and a mini-crate - for single FEB safe without water cooling
- Crate controller nice to have, but not needed (FEB can be jumpered on), power same.



Connection to Sensors

- Needs a detector adaptor board (DAB)
  DABs are a subsystem responsibility
  (Pixel: Heidelberg)
- Connects to the back of the backplane
- (can use two connectors soldered together if no backplane available)
- One connector serves up to 6 MuPix (inner layers, three links) or 18 MuPix (outer layers, one link)





Front-end board firmware

- MuPix configuration
  (Currently SPI version, MuPix11 protocol being added)
- Receiving and decoding MuPix data
- Link monitoring, protocol checks
- Time sorting of hits
- Transmission of hits to receiving board
- Board monitoring and programming

On the way:

- Tapping of data at various points in the process
- Receiving and processing MuPix slow control data

- Do the planned Q&A tests need additional FEB firmware?

Receiving board firmware

- Receive data from FEBs
- Optical link monitoring
- Protocol for FEB and ASIC configuration and monitoring
- MIDAS bank building for hit data
- PCIe DMA to PC

- Note that this mixes firmware from the receiving boards and switching boards in the final DAQ

- Do the planned Q&A tests need additional receiving board firmware?

Software

- Driver for PCIe
- C++ libraries for slow control and monitoring interface
- MIDAS code for hit readout, board monitoring
- MIDAS code for ASIC configuration (needs to be adapted for new configuration scheme)

- MIDAS analyzer for hit maps, easily extendable

Meetings

- DAQ developers meetings every Monday at 15:00 (Zoom)
  Agenda and minutes in online repository wiki
  - join the DAQ elog for announcements

- Regular discussions of set-ups, firmware and software developments

- We are happy to zoom you through setting up your first MiniDAQ

Summary

- Basic functionality available in hard-, firm- and software
- Many things still a bit rough around the edges - still implementing and testing fixes from the integration run
- Documentation growing, many helpful experts around

- Let us know what you need and give back your tools to main DAQ