Copper-only HDI Proposal for Layers 1/2

Luigi Vigani

The issue

- We would like to start production in spring 2022: first components this summer
- At the moment there is a very small chance we get the HDIs from LTU by then
- The fastest way to obtain HDIs is if we use commercial processes
- Market search: https://docs.google.com/spreadsheets/d/1fK8br_EWg2NFutqiv0k_RoxWn1UQ-HieV1m4q2HJvSE/edit?usp=sharing
- Commercial HDIs are mostly in copper
  - Changes to manufacturing process to be discussed later
- We looked for the process with the thinnest copper process which seemed reasonable

The issue

- Another key point is compatibility with the rest of the design
- The design of the other components is ongoing
- We do not want to redesign everything
- With copper, we only get rid of the interposer flex
- The pad pin-out at the interposer may change
- End-ring flex design not finalized, still chance to change it

One company replied positively

Beta-layout (UK):

“For flex PCBs we can offer 9 µm base copper, but since you mention it will be a 2 layer PCB, the finished copper thickness will be min. 18 µm because of required plating process for vias from top to bottom layer. If there are no plated holes for connecting top and bottom layer, then also finished copper thickness can be 9 µm.

Min. trace width will be 0.0762 mm (3 mil) and min. spacing 0.0889 mm (3.5 mil).

Please let me know if these specifications meet your requirements.

For quotation we will need the files in one of these file formats:

PCB File Formats | Beta LAYOUT Ltd.
Since you mention bond pads, please also give us information if you use aluminum or gold wires for bonding process, so that we can choose the matching surface finish type for these flex PCBs”

One company replied positively

Beta-layout (UK):

Is 18um only at the vias or everywhere?

“[if we use vias] It will be 18 micrometers finished copper thickness for each side (9 micrometer copper foil + 9 micrometer plating process). Copper wall thickness in vias will be approx. 10 micrometers. If 9 micrometers should be finished copper thickness for each side, it will be only 2-3 micrometer copper wall thickness in vias which is not good for conduction and easy to break this copper barrel.”

Is differential impedance 90-100 Ohm? (polyimide layer is 50 um)

“Yes, differential impedance will be around 95 Ohms with 0.0762 mm trace width and 0.0889 mm spacing. In case of order we can also do impedance simulation during file preparation before releasing to production. This impedance simulation is without any additional cost.”

Possible solution

- Go with Beta-layout without vias (next slides for how)
- It would be 9 um of copper instead of 12.5 um aluminum

Recalling previous calculations:

- At same thickness X/X_0 for copper is **6.2 times** higher than aluminum
- In that scenario, the radiation length increases by **1.37×10^{-3} X_0**

With 9um copper we could scale

- X/X_0 for copper is **4.5 times** higher than aluminum
- In that scenario, the radiation length increases by **1×10^{-3} X_0**

Is it worth trying?

Person-power in Heidelberg

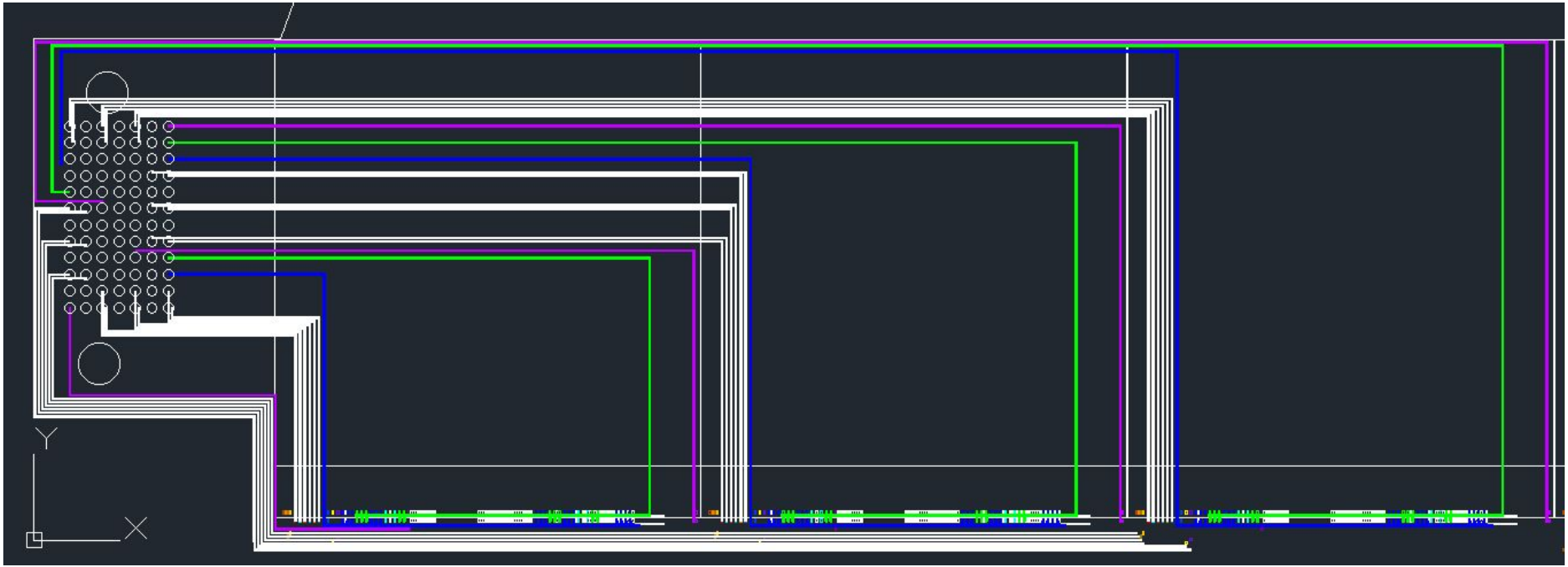
- One designer gave his availability
- He already designed crucial components of the integration run DAQ
- He is also looking around for aluminum alternatives in case
    - If we agree on this he will just focus on this project

No vias: how?

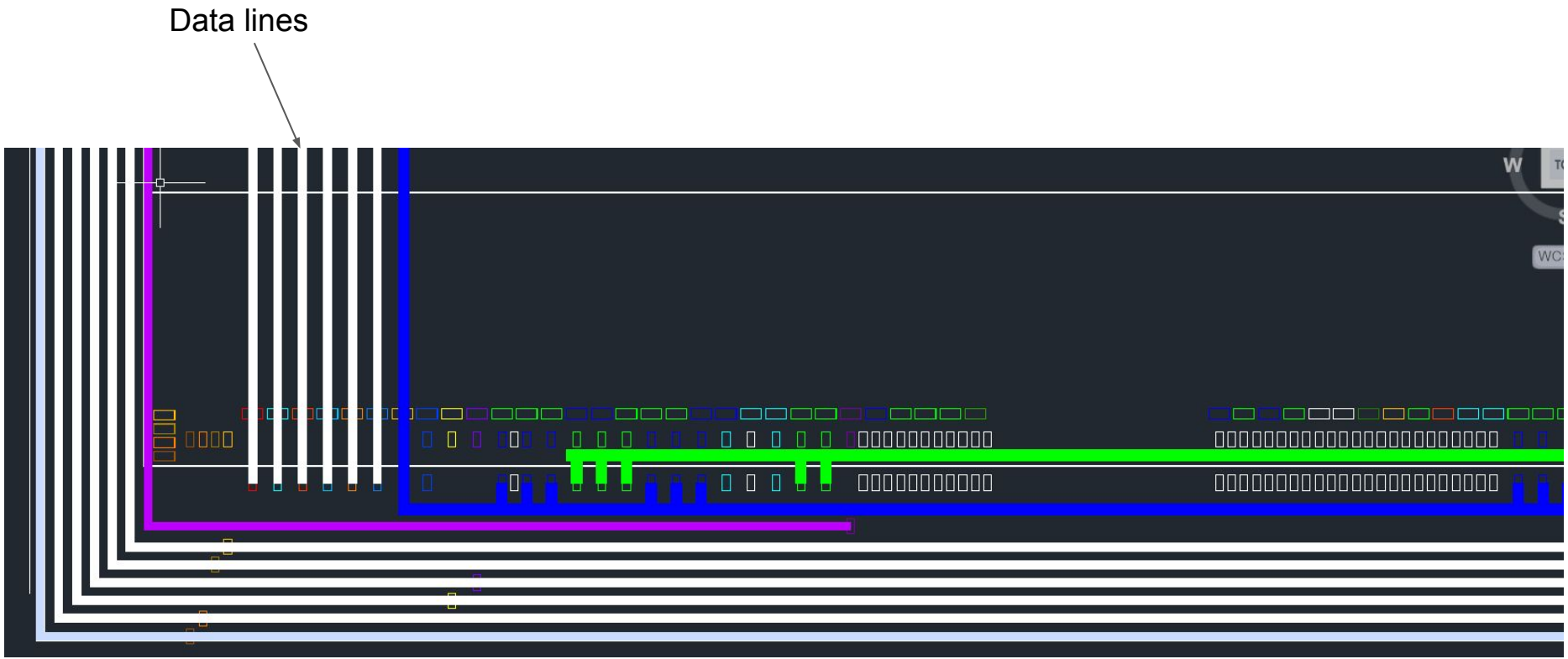
All relevant lines on top layer.

Interposer with same grid as Samtec interposer: routing at the interposer the crucial point.

Preliminary design (dxf):



At the chip pads



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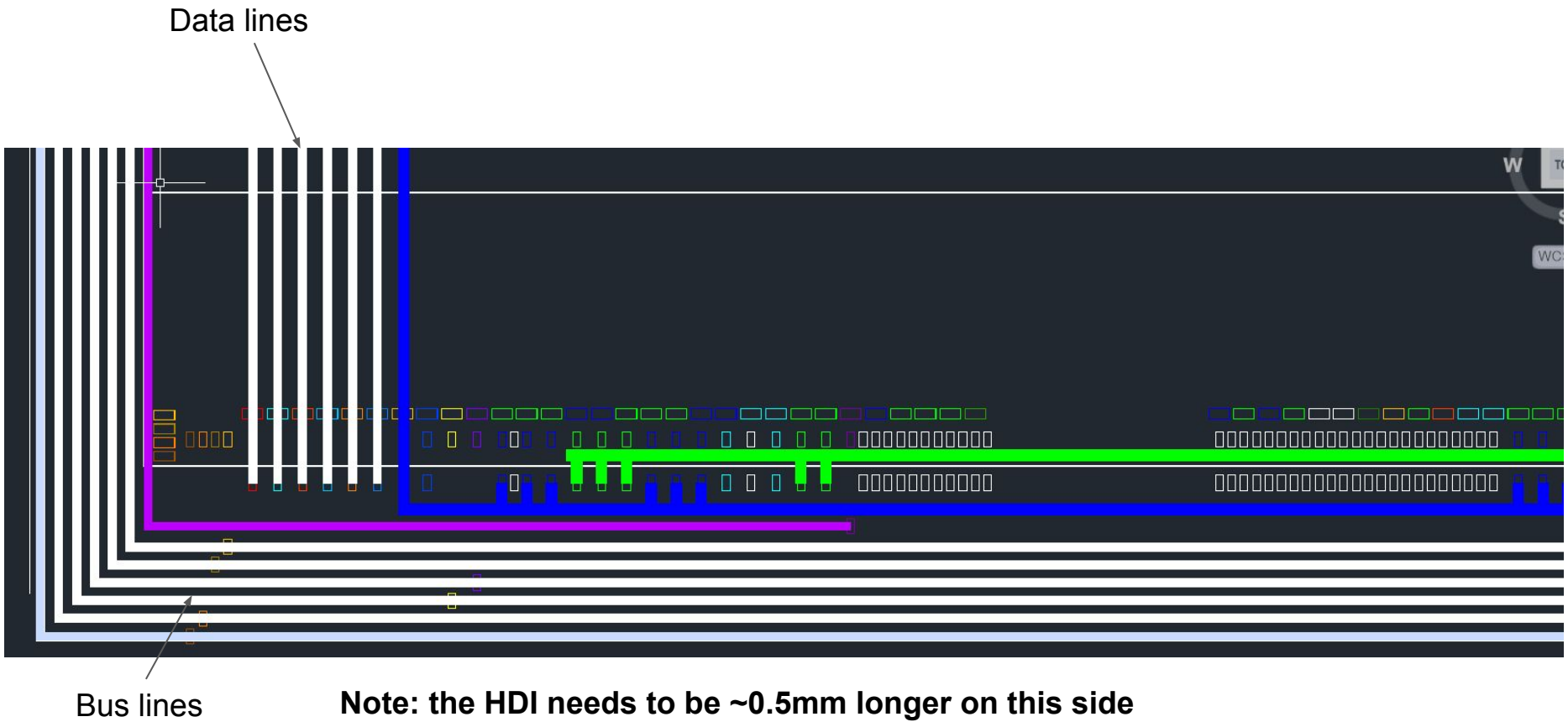
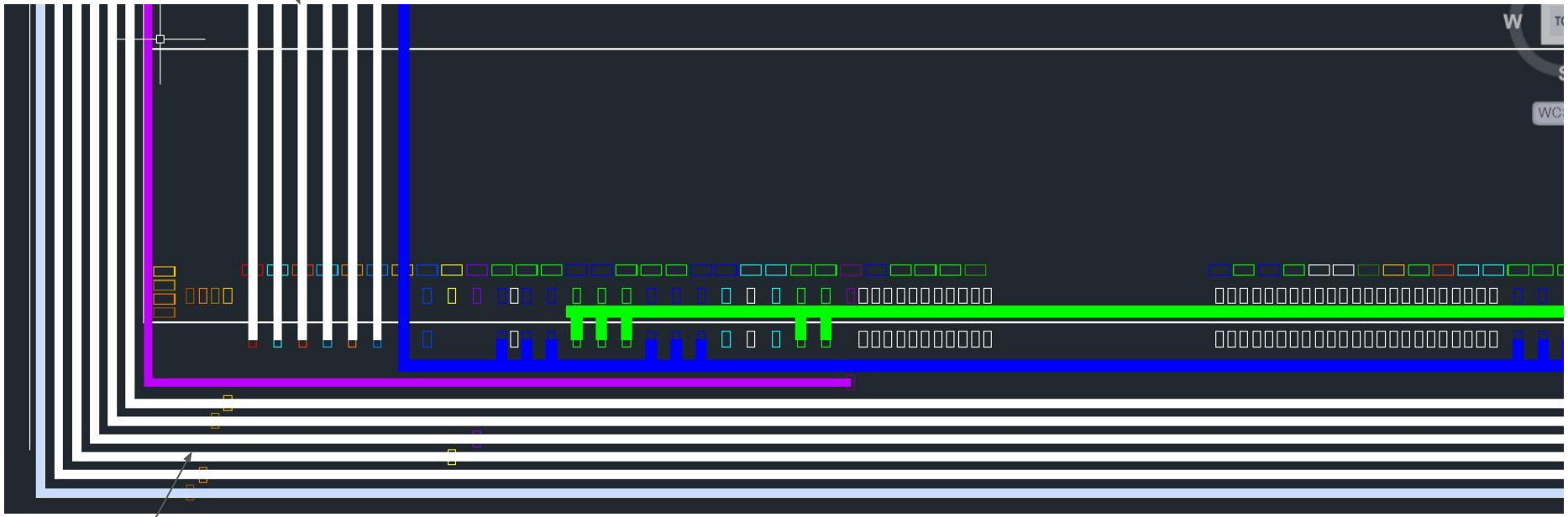


Note: the HDI needs to be ~0.5mm longer on this side

At the chip pads

Data lines

Green and blue are VDD bar and GND bar. One goes to the left and one to the right of the chip.



Bus lines

Note: the HDI needs to be ~0.5mm longer on this side

At the chip pads

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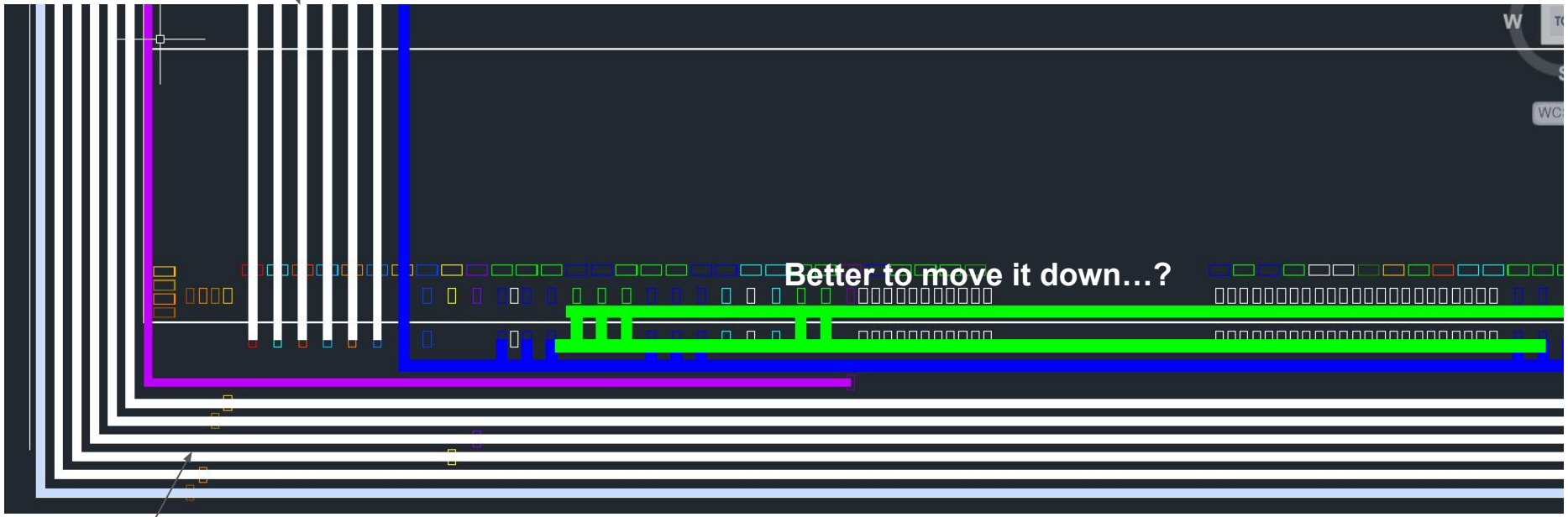
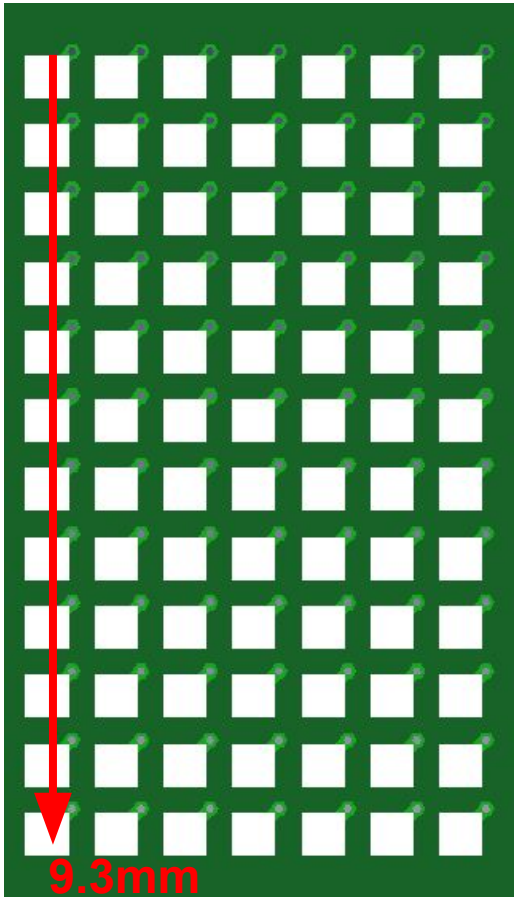


Bus lines

Note: the HDI needs to be ~0.5mm longer on this side

Line density calculation at interposer

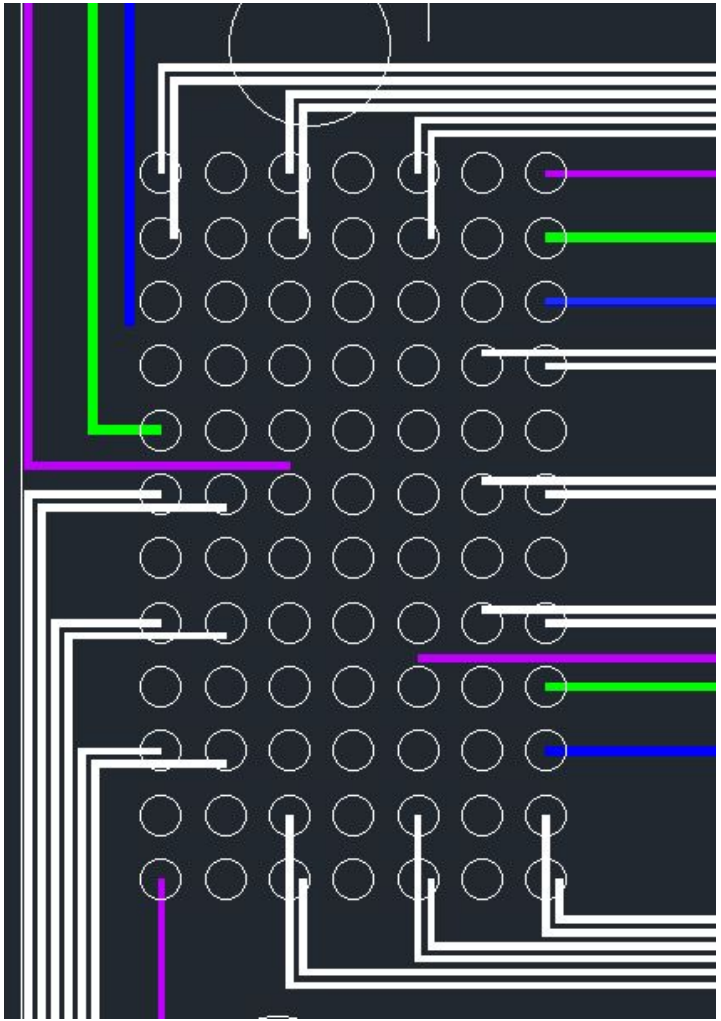


Min. trace width will be 0.0762 mm (3 mil) and min. spacing 0.0889 mm (3.5 mil)

Space between interposer pads: 3 mm

One differential pair (with spacing from the next):
0.0762*2 + 0.0889*3 = 0.4191
-> differential pairs can not go between interposer pads

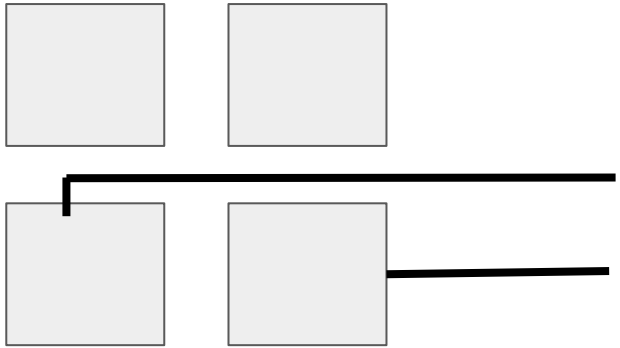
one line can:
0.0762 + 0.0889*2 = 0.254

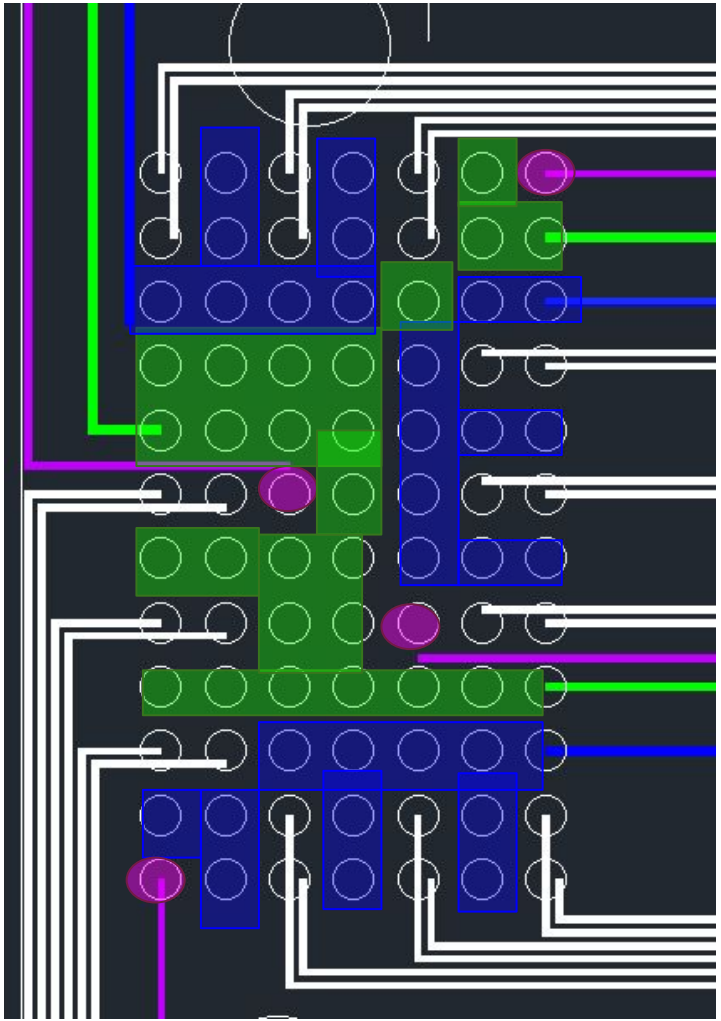


More detailed

Note: the line directions are simplified, the designer will make them properly.

The constraints make it possible if the differential lines are routed to the external 2 interposer pads:





Pad distribution

White: LVDS

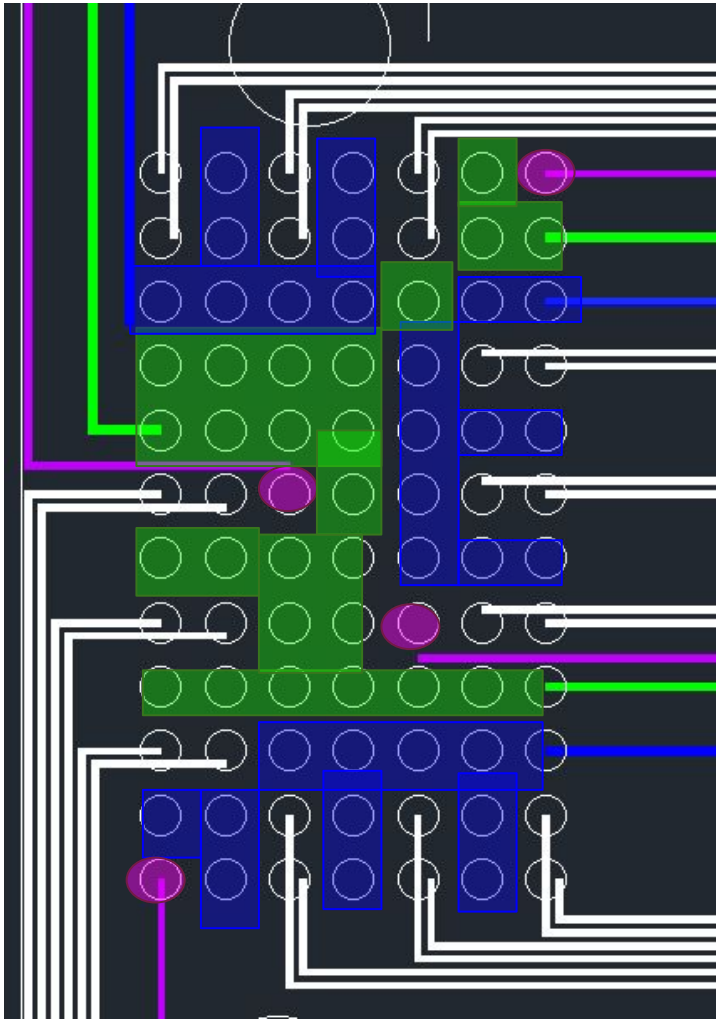
Blue/Green: VDD/GND

Purple: HV

Purple (bottom left): Temperature diode

VDD and GND sense can be added as lines following side-by-side one of the chip's VDD and GND lines

Note: only green here is shorted among chips, but blue can be shorted on power lines below the chips (see later)



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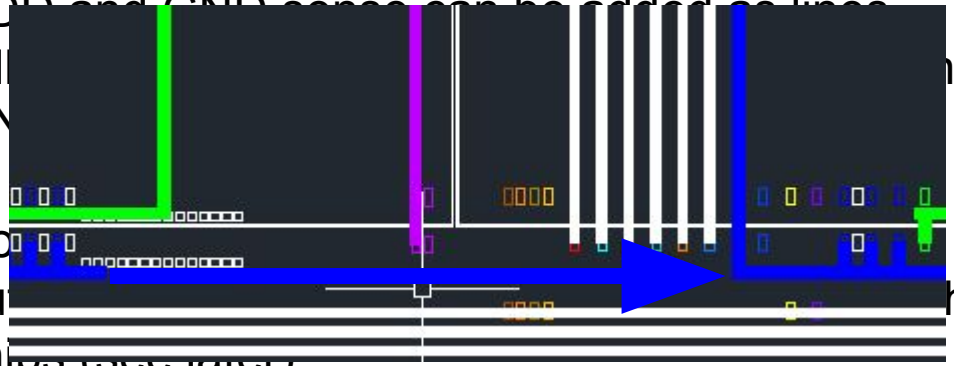

No
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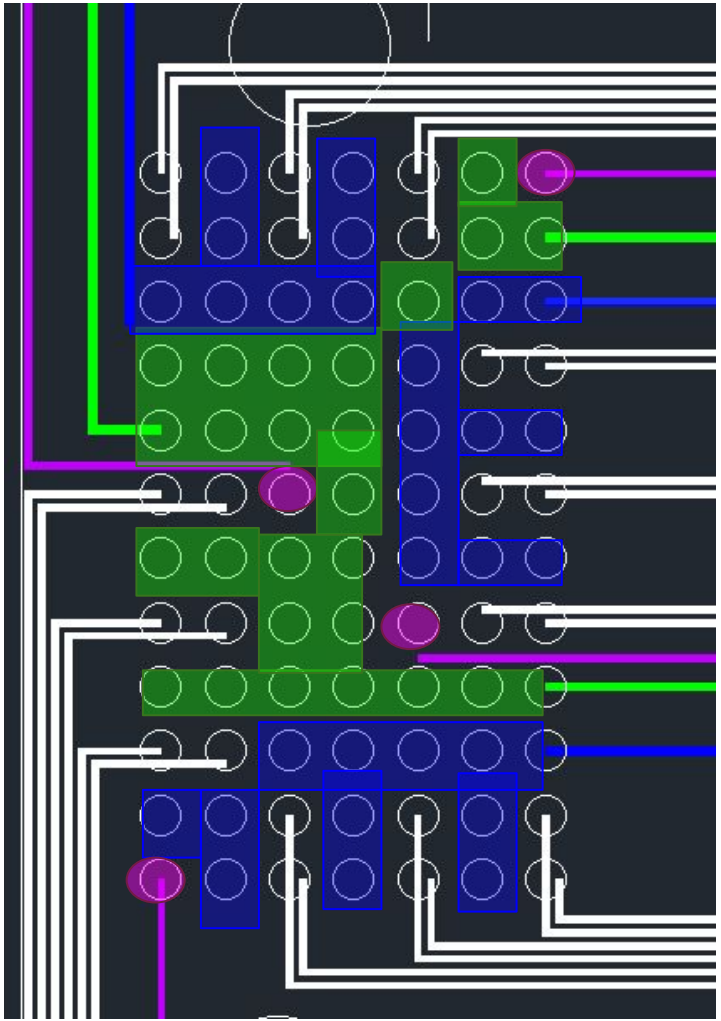
chips (see later)



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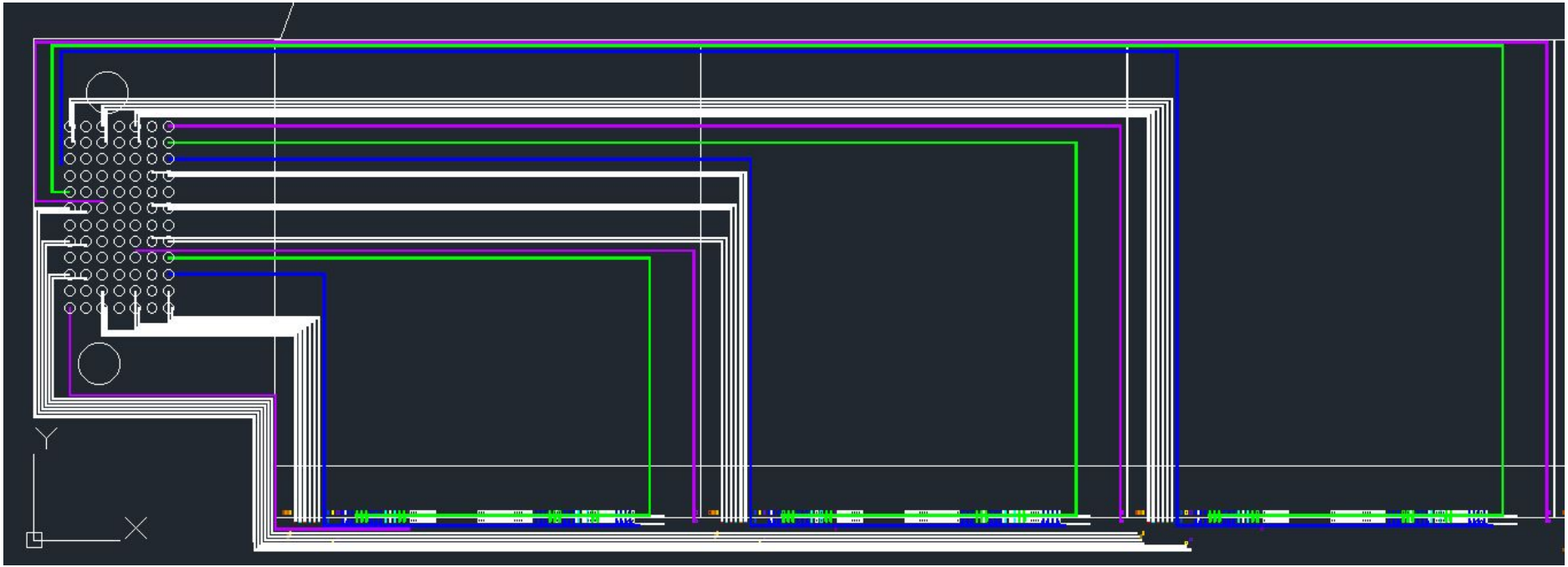
VDD and GND sense can be added as lines following side-by-side one of the chip's VDD and GND lines

Note: they are shorted anyway on the end-ring flex, but ground loops?

LVDS impedance

Bottom layer should have only ground bars covering the LVDS lines



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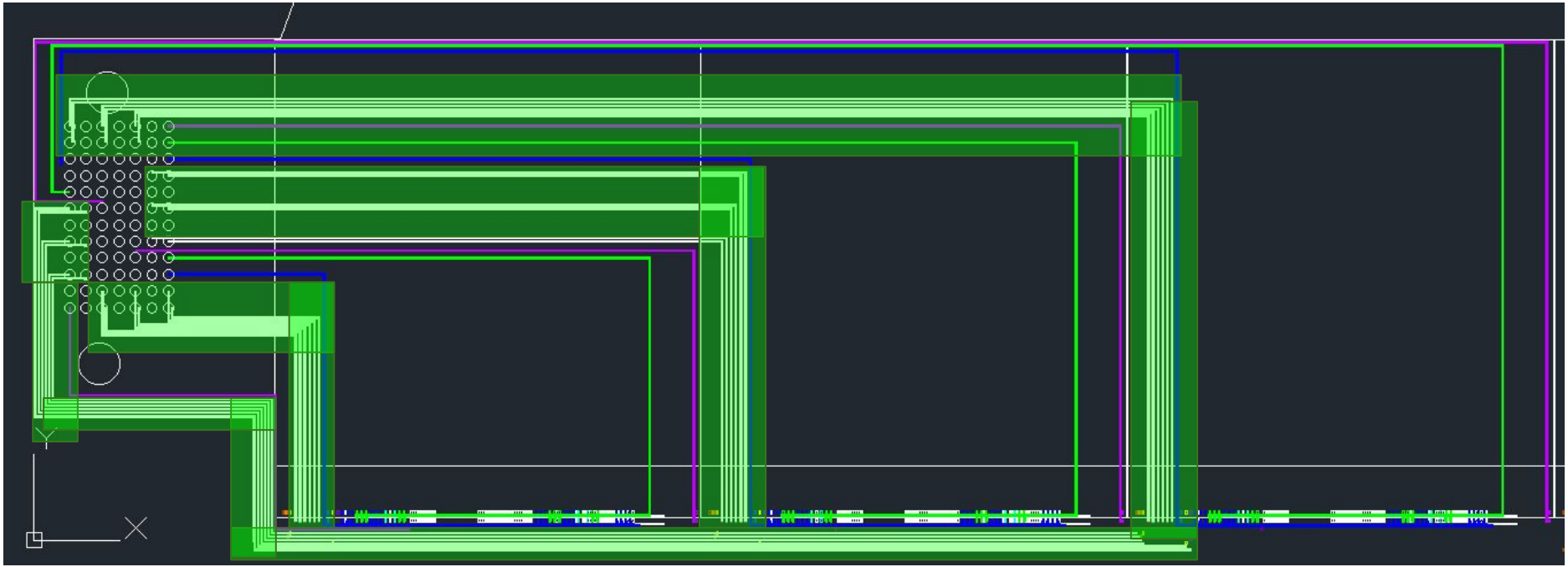
How to connect without vias?



LVDS impedance

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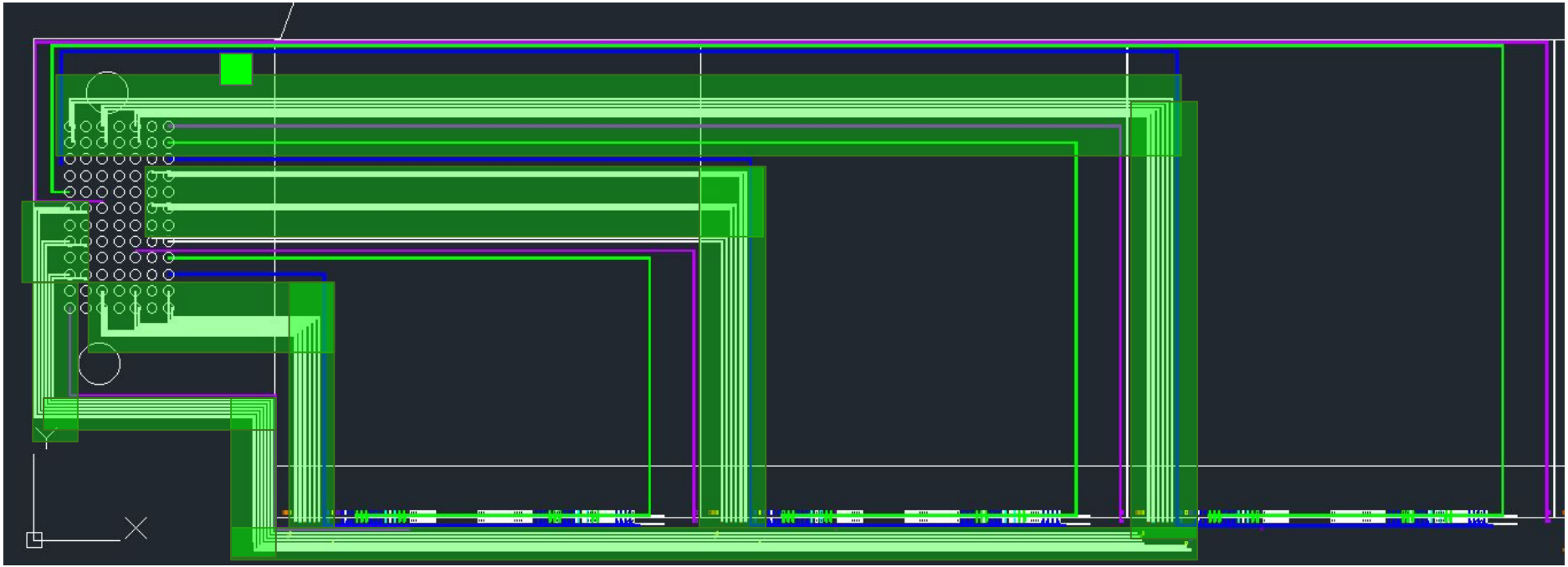
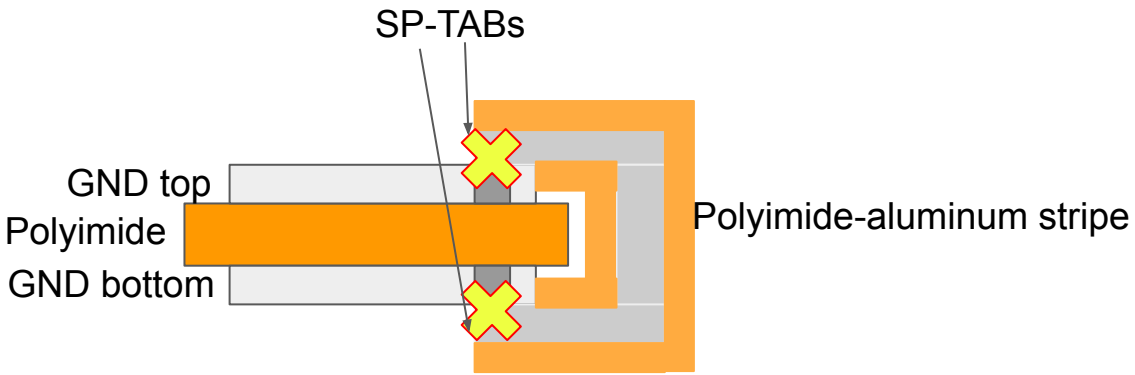
How to connect without vias: add TAB pads on either layer

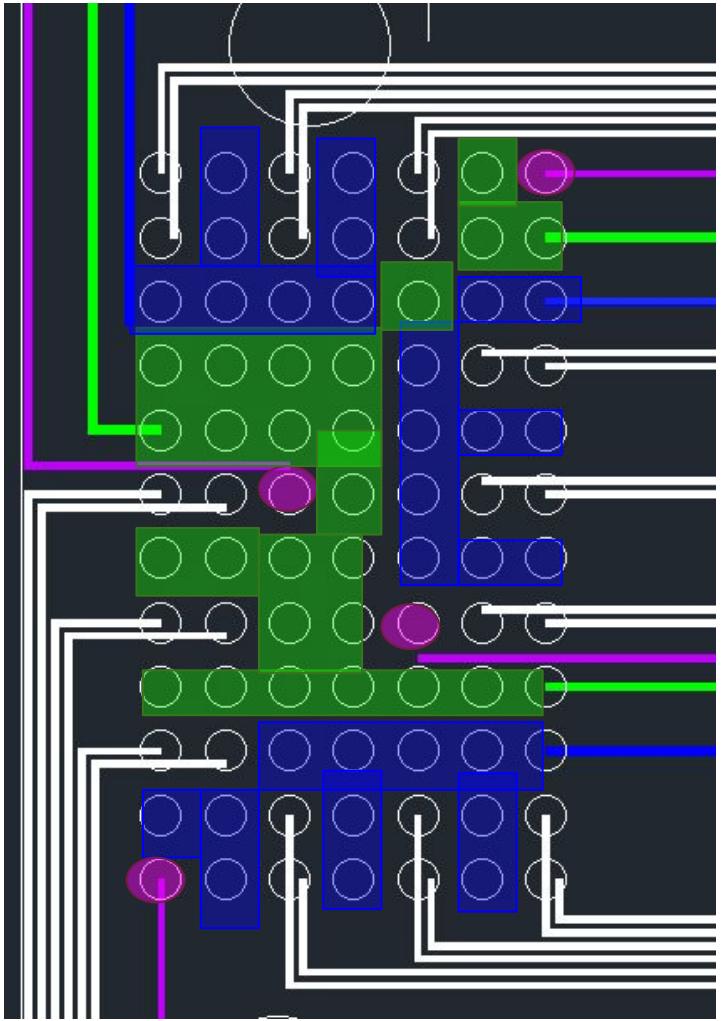


LVDS impedance

Bottom layer should have only ground bars covering the LVDS lines

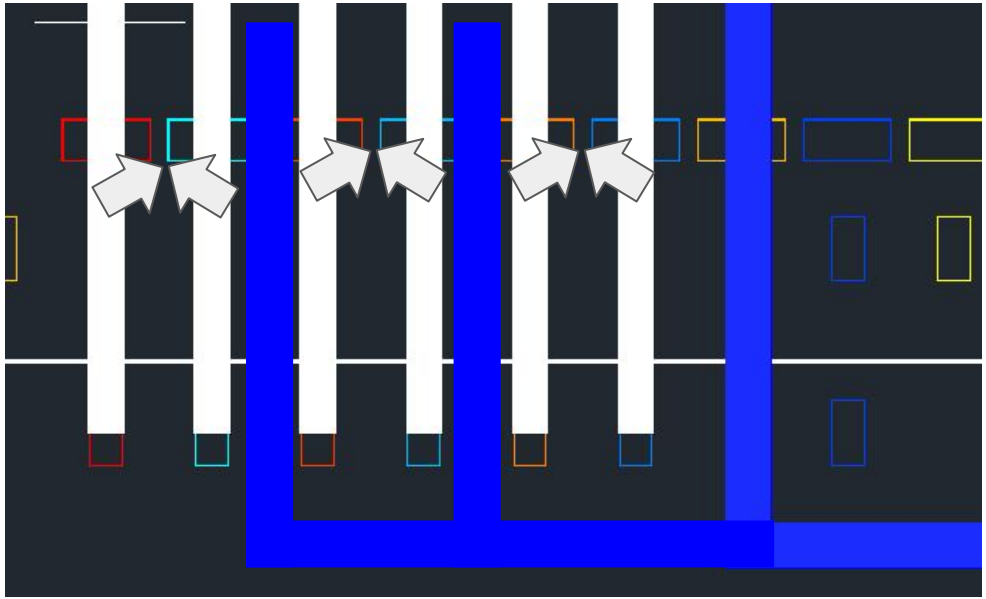
How to connect without vias: add TAB pads on either side





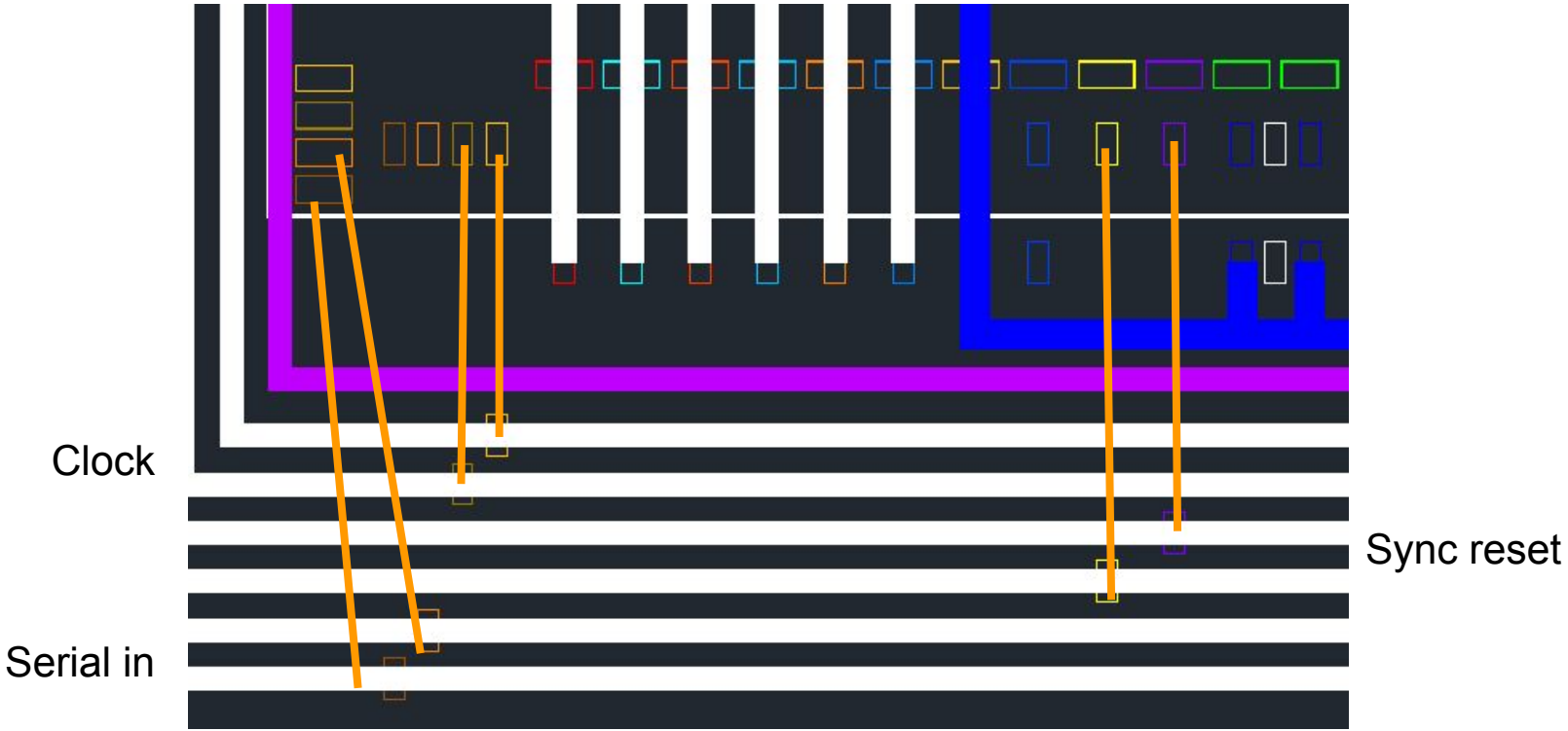
LVDS insulation (cross-talk reduction)

Data lines:
VDD/GND are already in between data pairs at interposer
Can be done also from the other side:



LVDS insulation (cross-talk reduction)

Bus lines: no GND possible in-between. One note: sync_res sends one bit every now and then: should it be in the middle…?



Possible issues

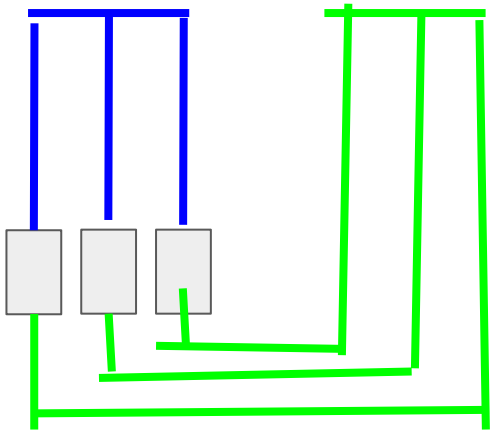
- Wire bonding:
  - More fragile
- Chips oriented upwards, on top of flex
  - Less possibility for alignment during assembly phase
- Extra TA-bonds
- ~0.5 mm larger
  - Likely not a problem -> to be verified
- Others…?

Should we try and go for it?

Backup

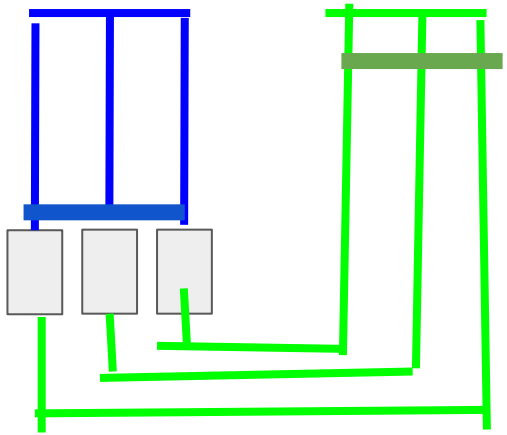
Ground loops

End-ring flex



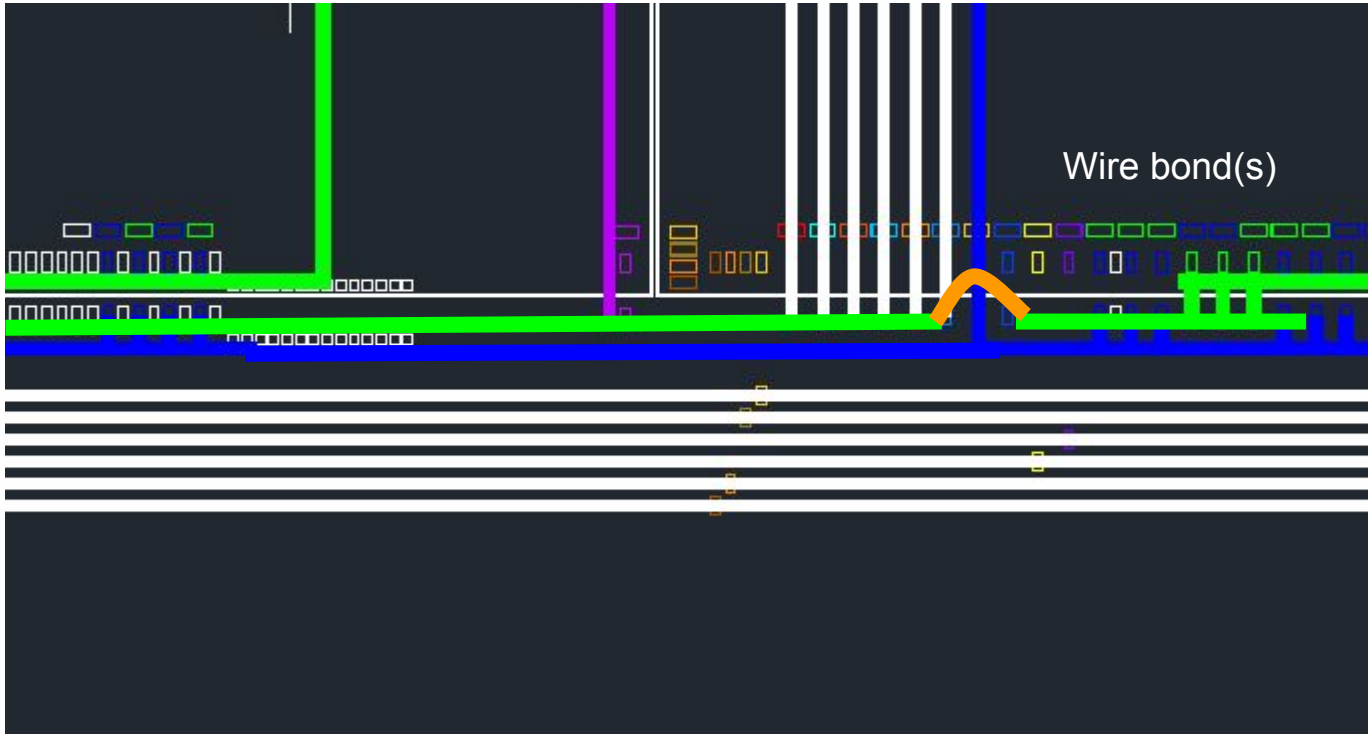
With no shorts on HDI

End-ring flex



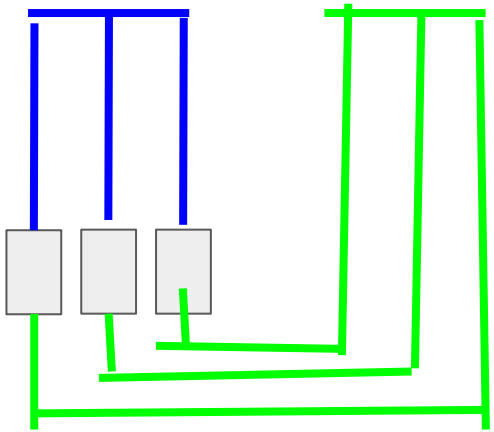
Possible shorts

Another short on green line



Ground loops

End-ring flex



With no shorts on HDI

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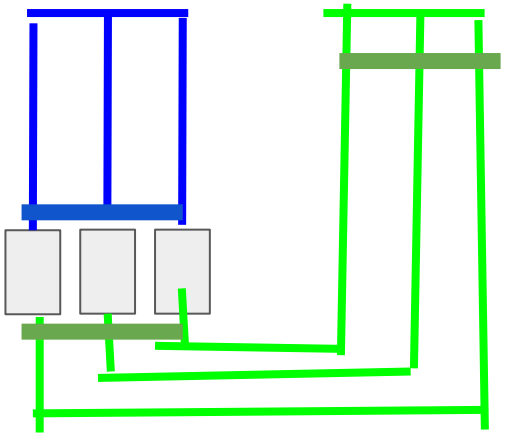
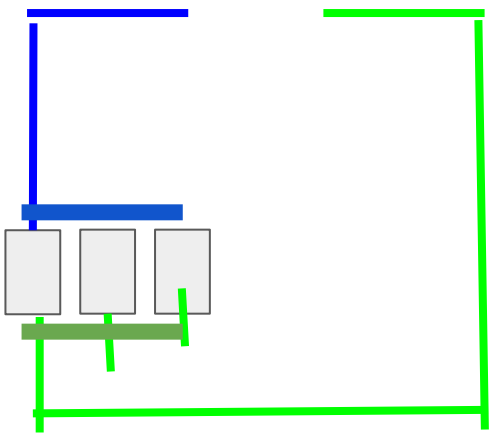


Possible shorts with internal wire-bonds

End-ring flex



Possible shorts with internal wire-bonds and no loops