

# Low Level RF Workshop 2022



9-13 Oct 2022, Brugg-Windisch, Switzerland



Contribution ID: 5

Type: **Oral**

## FPGA-based hardware acceleration of machine learning algorithms for particle accelerators

*Monday, October 10, 2022 2:35 PM (20 minutes)*

Diagnosis and supervision of particle accelerators is mostly a manual task, requiring deep insight by human operators. The usage of machine learning and data analysis has the potential to enhance the controllability and the diagnosis capability.

However, applications like longitudinal phase-space estimation, automatic control optimization, or anomaly detection can be used only when the hardware acceleration enables them to cope with the huge amount of data and stringent latency in response times required.

This work discusses how to trade off latency and throughput in FPGA-based hardware acceleration for machine learning algorithms. Specifically, current off-the-shelf tools focus on throughput, while latency is the main optimization goal in our setting.

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**Session Classification:** Machine Learning

**Track Classification:** Low Level RF Workshop 2022