PAUL SCHERRER INSTITUT

Low Level RF Workshop 2022 -Poster #9

RF Performance Characterization of the SLS-2 500 MHz LLRF Prototype in the Lab

R. Kalt <roger.kalt@psi.ch>[1], A. Dietrich[1], L. Moser[1], R. Rybaniec[1], B. Stef[1]

[1] Paul Scherrer Institut (PSI), Dept. Large Research Facilities (GFA), CH-5232 Villigen PSI, Switzerland

Abstract

For the SLS-2 project and the 500 MHz RF upgrades, the LLRF will be renewed and the previously analog system is going to be replaced by a digital one. The new system is built into two separated chassis, an analog frontend and a CompactPCI Serial based digital backend interconnected with coaxial cables. The custom design analog frontend implements two up- and eight down-conversion channels 50 to 500 MHz and vice versa. The digital backend consists of low latency high speed ADCs and DACs connected to the same FPGA/MPSoC that processes the signals in the digital domain.

This poster focus on several generic- and RF-type performance charac-terization measurements of the actuator- and the DAQ-paths of the LLRF system, done in the lab environment.

CPCI-Serial Crate:

- 1x UFC (FPGA FMC Carrier)
- 1x ADC3110 FMC (8ch)
- 1x rear module DAC (2ch)

RF Frontend Crate:

- 8ch downconverter
- 2ch upconverter
- 1x clocks generation
- 1x slow control interface

Fig. 1: Measurement setup in electronics lab

RF Actuator

RF Station Requirements

	RF Tolerance (rms)	Cavity BW's
Phase	0.020 deg	±13, 33, 44 kHz (BO, SPB, SR cavity)
Amplitude	0.001 rel.	

Table 1: RF field tolerance requirements for the various RF cavities

Hardware

- CPCI-Serial: I/Q Modulator in FPGA, clocked with 500 MHz and generating a 50 MHz IF signal using the DAC AD9783 (16-bit, 500 MHz, LVDS data interface). Output circuit: AC-coupled single-ended output path with reconstruction filter.
- RF frontend: Image Reject Mixer and filtering for up-conversion from 50 MHz IF to 500 MHz RF including fast RF switches for interlocking purpose and monitoring ports.

Phase noise measurement

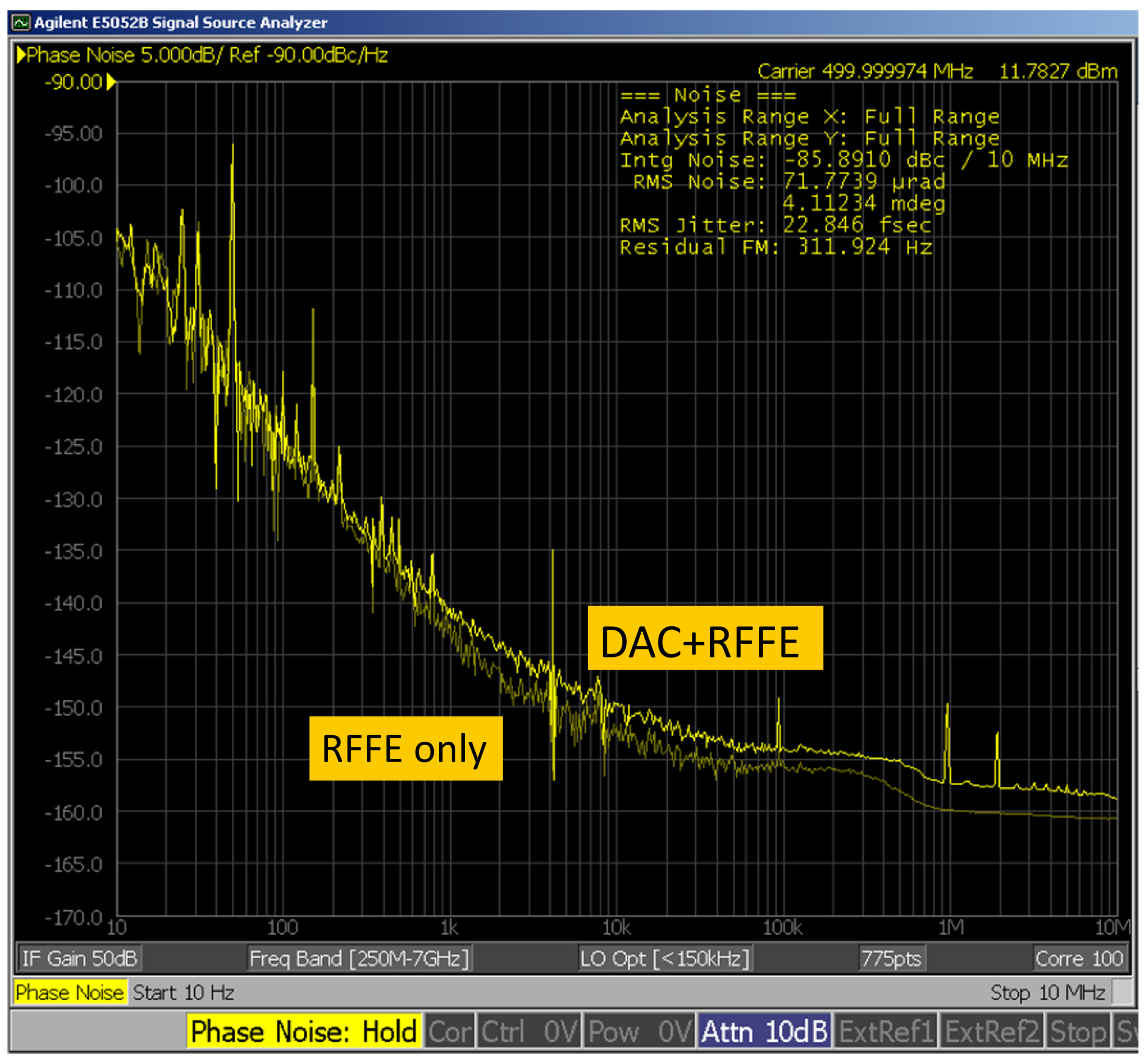

Fig. 2: Phase noise measurement graph

	Reference	RFFE only	DAC+RFFE
Abs. Phase Noise	14.4 fs	18.8 fs	22.8 fs [0.004'1 deg]

Table 2: Absolute phase noise measurements (10 Hz – 10 MHz)

RF Detector

Requirements

- Arbitrarily defined goal to measure **5 times better** than the requirement (Table 1).

Hardware

- RF frontend: Down-conversion mixer from 500 MHz RF to 50 MHz IF; with filters and control system adjustable attenuator in 1 dB steps (0..-7 dB).
- CPCI-Serial: FPGA FMC carrier (CPSI_UFC), ADC3110 FMC with ADC ADS42LB69 (16-bit, 250 MHz, LVDS data interface); clocked with 250 MHz. Demodulation in FPGA using non-IQ 1/5.

Full path measurement of the RF reference signal [data 20220602, FMC0485, ch1]

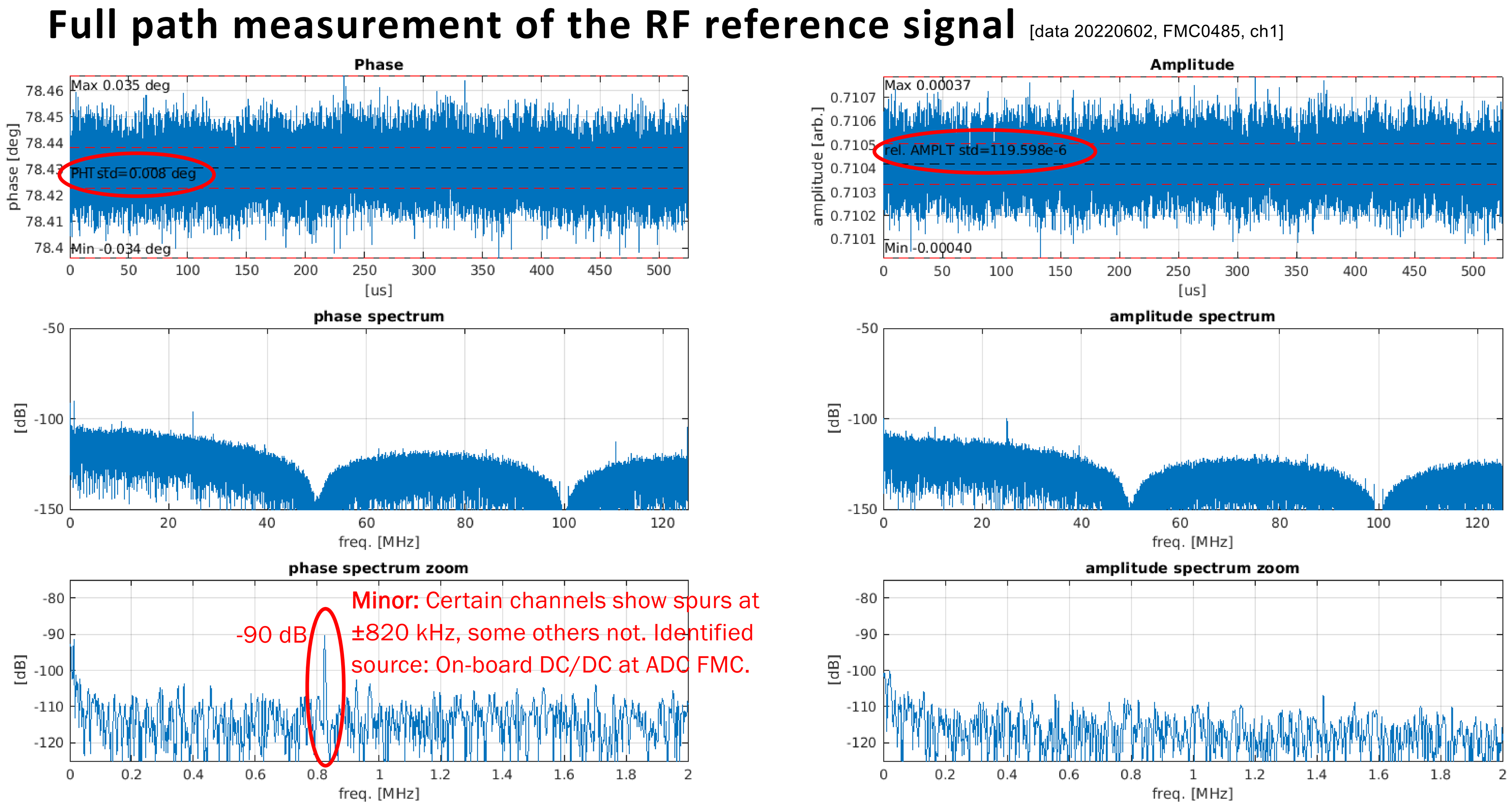

Fig. 3: Spectral analysis of demodulated phase and amplitude, full BW (250 MHz sampling)

	Maximum BW (limited by non-IQ 1/5 to 22.5 MHz)	Limited BW (downsampling to 100 kHz)
Phase	0.008 deg	0.001 deg
Amplitude	0.000'120 rel.	0.000'026 rel.

Table 3: Measured standard deviation of the CW type RF reference signal

Conclusion

The characterization of the most important RF actuator noise performance and RF detector resolution confirmed, the new system is within the given requirements. So the further focus is no longer in improving these performance parameters rather than system robustness, reliability, reusability, price and maintainability. The final LLRF measurement channel assignments are done such, that the important RF signals like cavity probe or cavity input are connected to "clean" ADC channels.

Version 03.10.2022