Contribution ID: **9** Type: **Poster**

RF Performance Characterization of the SLS-2 500 MHz LLRF Prototype in the Lab

Wednesday, 12 October 2022 14:27 (1 minute)

For the SLS-2 project and the 500 MHz RF upgrades, the LLRF will be renewed and the previously analog system is going to be replaced by a digital one. The new system is built into two separated chassis, an analog frontend and a CompactPCI Serial based digital backend interconnected with coaxial cables. The custom design analog frontend implements two up- and eight down-conversion channels 50 to 500 MHz and vice versa. The digital backend consists of low latency high speed ADCs and DACs connected to the same FPGA/MPSoC that processes the signals in the digital domain.
This poster focus on several generic- and RF-type performance characterization measurements of the actuator- and the DAQ-paths of the LLRF system, done in the lab environment.

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Session Classification: Poster Session

Track Classification: Low Level RF Workshop 2022