PAUL SCHERRER INSTITUT

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Design and Implementation of a Digital Tuning System for 50 MHz Cavities

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Abstract

At PSI, the high intensity proton accelerator (HIPA) delivers a proton beam of 590 MeV energy at a current of up to 2.4 mA. The RF cavities are operated in CW mode at a frequency of 50 MHz. The initial system was built about 30 years ago with the technology at that time which was predominantly analogue. With the modern replacement of the analogue system, the cavity operation and maintenance will be improved remarkably. Seamless integration to the control system (EPICS) will represent another advantage. Exception handling or additional operation modes are much easier to implement with the digital approach. This poster focuses predominantly on the design and implementation of the digital tuning system. First measurement results show the ability to tune the cavity.

Introduction and requirements

The tuning system is part of the digital Low Level RF system (LLRF) and is a piece of software running on the FMC carrier board (IFC1210 from IOxOS). The tuners are controlled via the Tuning Cooling And Control Unit (TCCU). On the other hand the TCCU box is connected to the tuning controller via EtherCAT bus. General requirements of the Tuning system are as follow:

- Tuning feedback operation at 25Hz
- Tuning feedback operation with phase signals, RF cavity input from coupler and cavity pick-up
- Operation modes: valve, position and resonance control
- Independent control of tuners in every mode
- Recording triggered by event, e.g. threshold value
- Monitoring and exception/fault handling

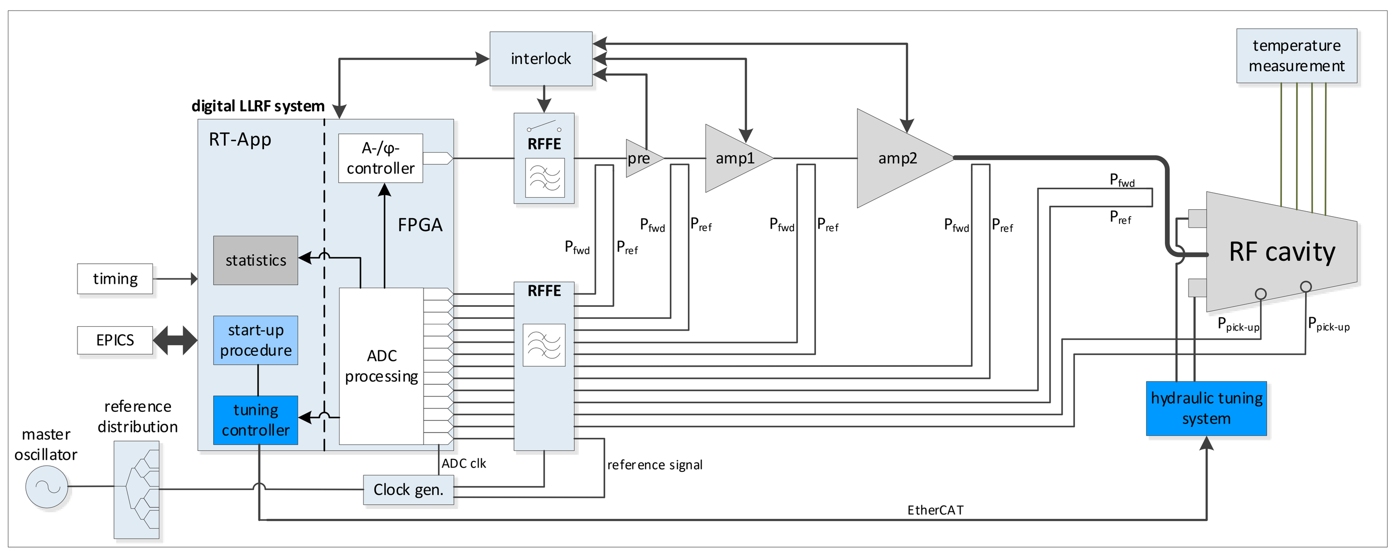

Figure 1: Overview of the entire RF system consisting of cavity, amplifiers, couplers, analog pre-processing units, interlock unit, hydraulic tuning system and the two tuners. Particularly noteworthy is the dark blue tuning controller, which is located in the lower left-hand corner of the figure. Control signals are sent to the hydraulic tuning system via the EtherCAT bus. Currently the cavity tuning feedback runs at 25Hz.

Design decisions

At the beginning of the project some decisions were made which are as follows:

- EPICS for IO, e.g. EtherCAT
- Time critical things are carried out in a separate process (RT-App) , e.g Tuning feedback
- Hardware platform is IOxOS IFC1210
- Linux with PREEMPT_RT patch, GNU toolchain for software development in C++

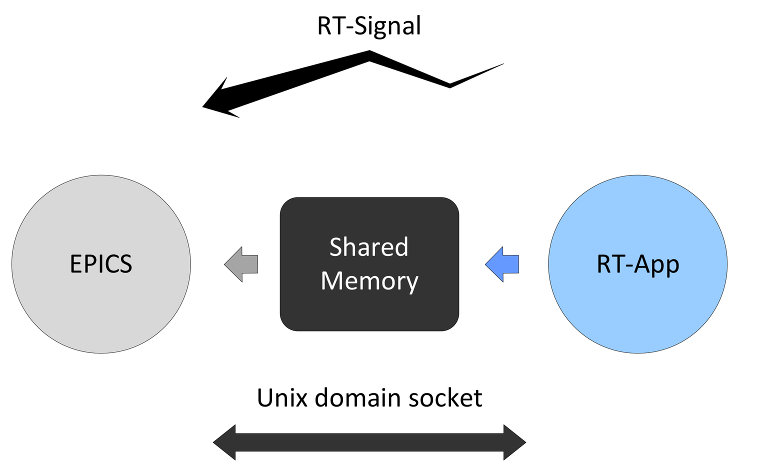

Figure 2: IPC methods used in the current approach to exchange data and synchronisation commands between EPICS and the RT-Application. Unix domain sockets are used for settings and parameters. Shared memory for big data blocks like wafeforms, and RT-Signals for example to trigger the Sharerd memory access of EPICS.

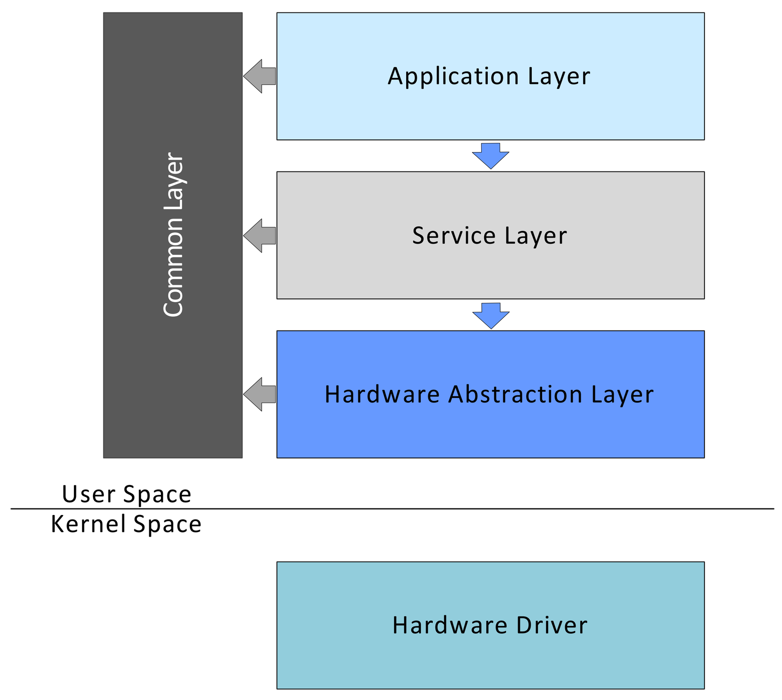

Figure 3: The application (RT-App) is a layered architecture. Responsibilities were divided into hardware abstraction, service and application layer. Additionally there is a common layer. Every layer includes components with specific responsibilities that are consistent with the layer's abstraction. The component dependencies are organised so that they always point downwards. From higher to lower (or same) levels of abstraction. The common layer can be used by all other layers.

Signal pre-processing

The carrier board from IOxOS IFC1210 assembled with FMC ADC 3110 pre-processes all ADC signals. We sample all ADC signals with fs=253MHz and demodulate via Non-IQ modulators. Thereafter we use down sampling techniques like CIC filters to get a data rate of 50.6 kSps and finally the CORDIC to change from cartesian to polar coordinate system for the tuning statistics calculation.

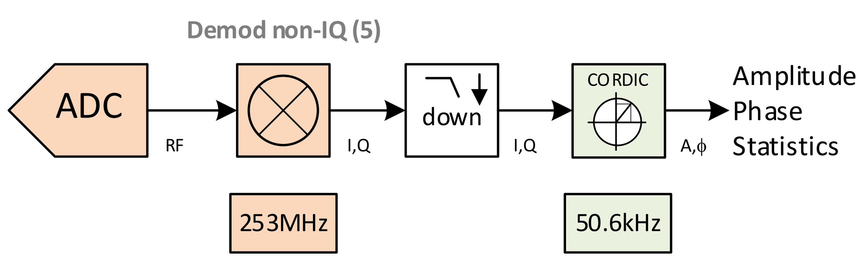

Figure 4: If we simplify the pre-processing inside the FPGA we get basically three main blocks. First we demodulate the ADC data, downsample it and convert it to polar representation. Of course there is a lot more to do, like buffering and synchronising.

Feedback controller

Basic building block for all feedbacks (position and phase tuning) is a PID controller having a two degree-of-freedom (2-DOF) structure. Control signal saturation is handled via back-calculation and tracking.

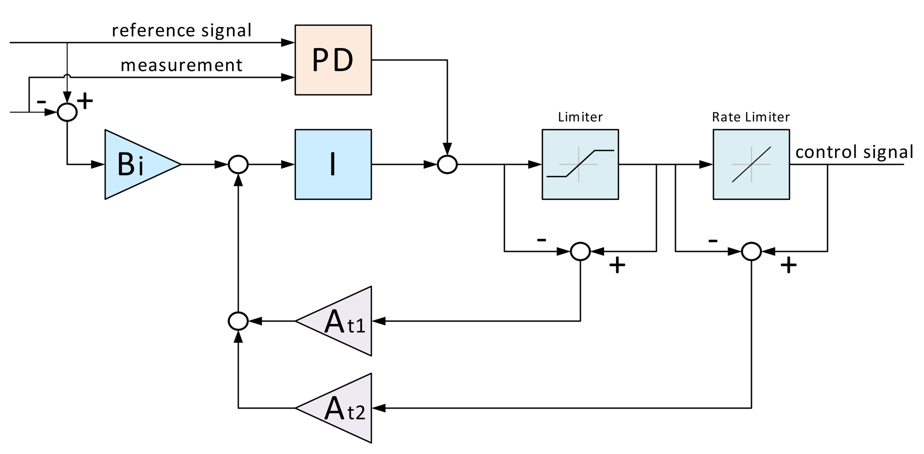

Figure 5: PID controller with differentiator on measurement signal, derivative filtering, euler forward integration, output limiter, rate limiter, set-point weighting and saturation handling (wind-up).

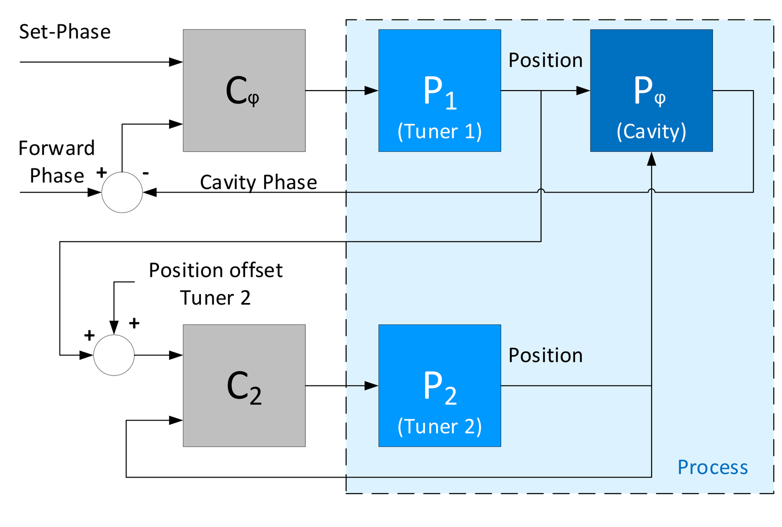

Figure 6: Feedback constellation to tune the cavity. Phase controller (C_ϕ) uses the phases to tune the cavity and the position controller (C2) uses the tuner (1) position to follow.

Comissioning results

All measurements were carried out without beam and were intended to verify the operation of the tuning system. During the measurements the cavity was not temperature stabilized. The power amplifier had a power of 25 W.

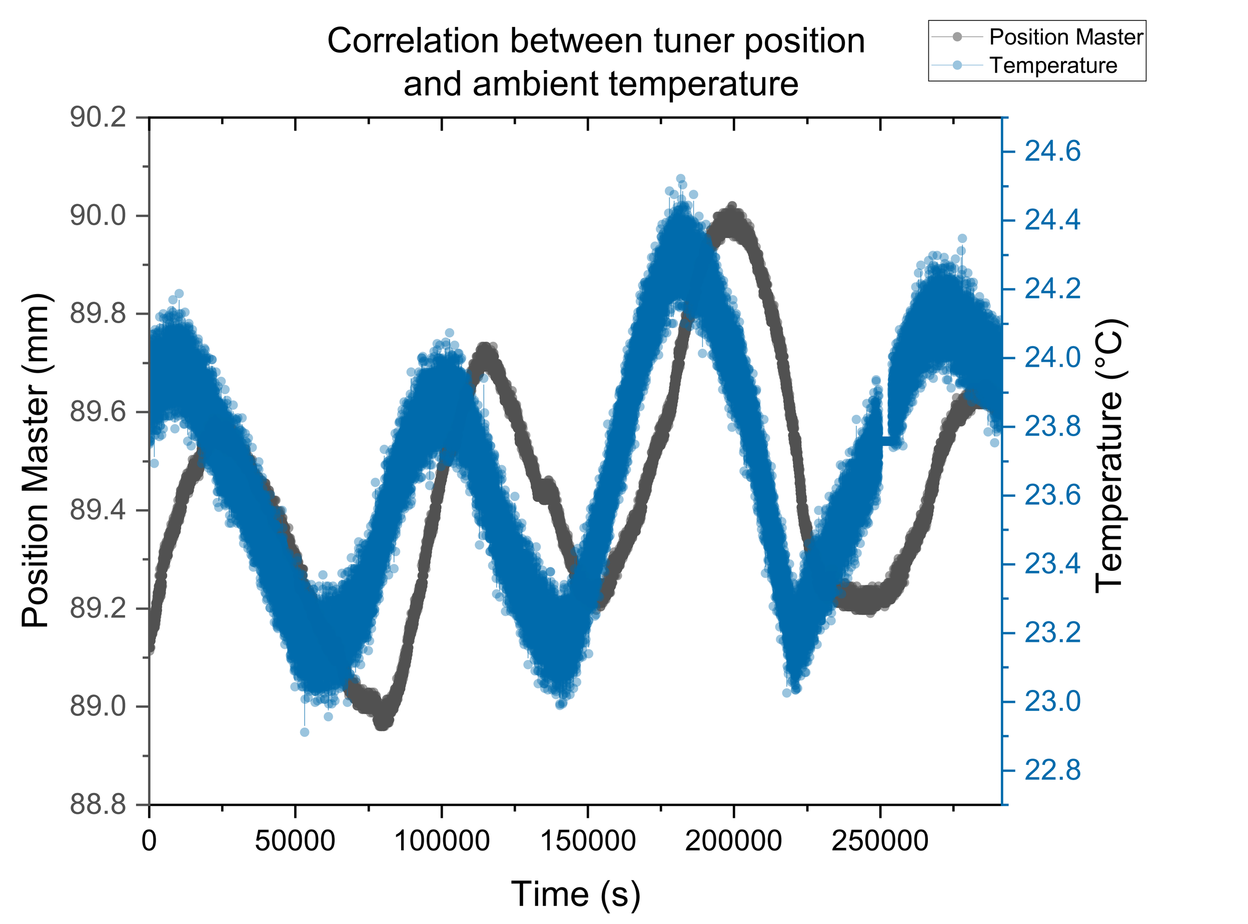

Figure 7: This measurement was taken over a period of approximately three days (81 hours). The tuner position follows the temperature with a delay of about 4 hours. (fs=0.2Hz)

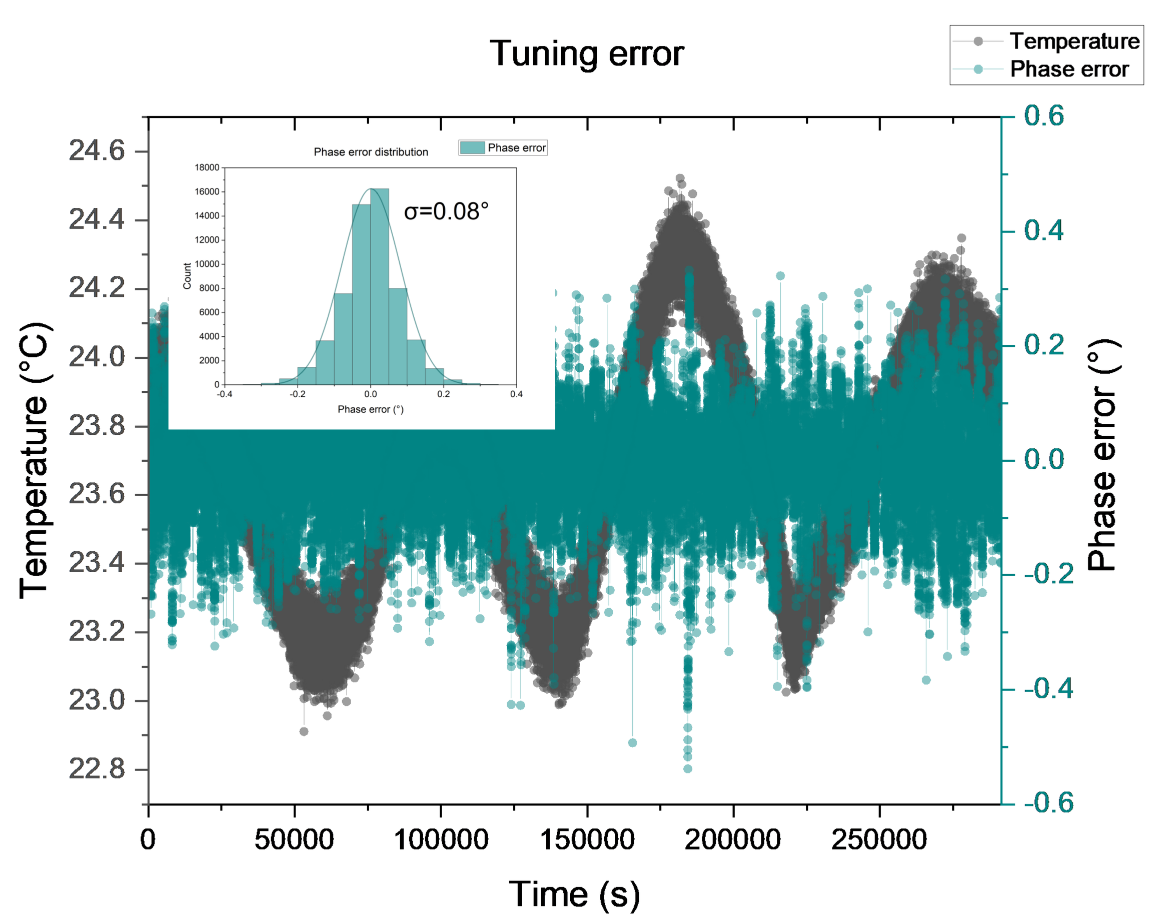

Figure 8: This measurement was taken over a period of approximately three days (81 hours).

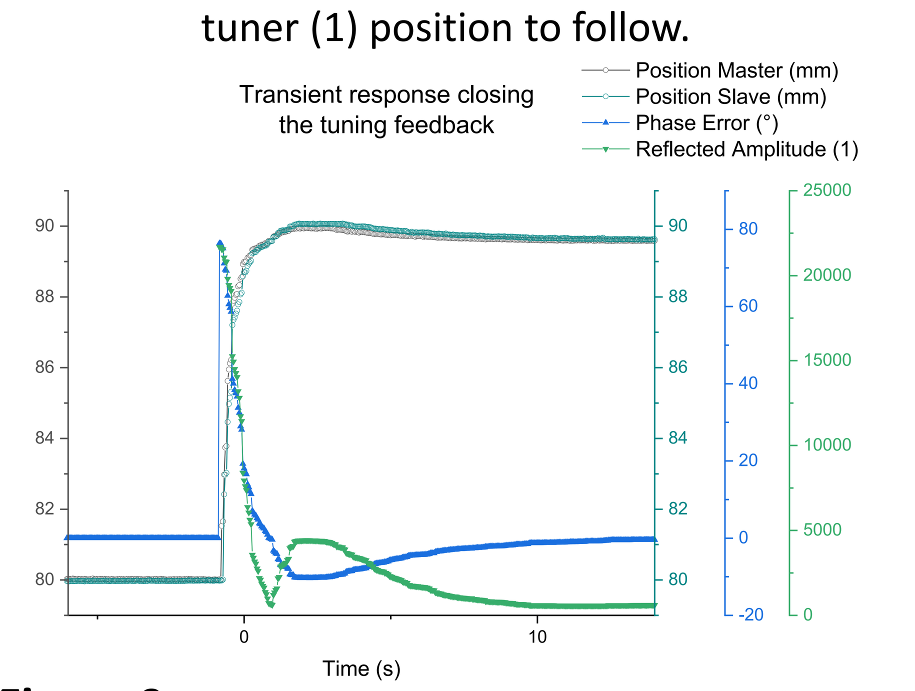

Figure 9: This measurement was taken with fs=25Hz. The bump in the reflected amplitude is due to the driving behaviour of the slave tuner.

Conclusion

This implementation of the digital tuning system will replace the currently used analog system. Measurements show that the system can be put into operation.

Acknowledgement

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