PAUL SCHERRER INSTITUT

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CompactPCI Serial Based Generic and Modular Processing Platform at PSI

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Abstract

CompactPCI Serial has been selected as one of the Next Processing Platforms (NPP) for development of future electronic systems at PSI. In this contribution, we describe the new platform and the pilot application for the Swiss Light Source (SLS) LLRF upgrade. We detail Hardware/Firmware/Software architectures, present automated testing procedures, as well as share the hands-on experience gained during first months of system's operation in the lab.

Boards Level

The PSI CPCI-serial crate is a 9 slot custom crate, where standard CPCI-serial front boards and custom rear boards can be used. The OpenCPSI-serial[1] pin mapping definitions extends the CPCI-serial standard, it's aim is to guarantee interoperability between FPGA and I/O boards.

Used board:

- **CPSI_UFC:** Design at PSI*, Zynq US+, 4GB DDR4 Mem, SFP+ & USB
- **CPSI_DAC_RTM:** Design at PSI*, DAC 500MHz 2ch, SFP+
- **ADC3110**: COTS FMC module*, ADC 250MHz 8ch, GPIO

*(*cf. Poster #9 & https://indi.to/666jk*)

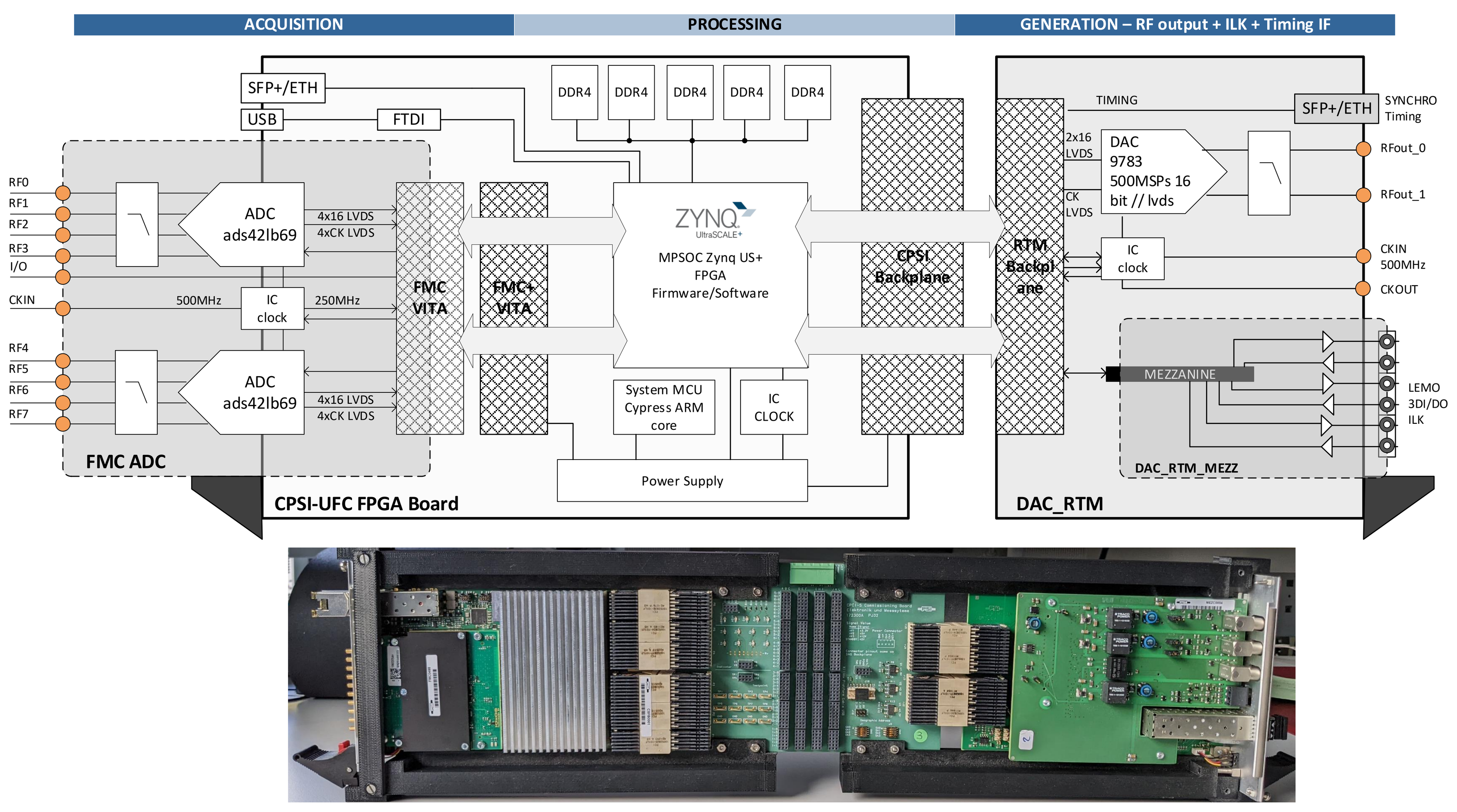

Fig. 2: CPSI-UFC FPGA carrier board + FMC ADC and DAC-RTM with mezzanine

System Level

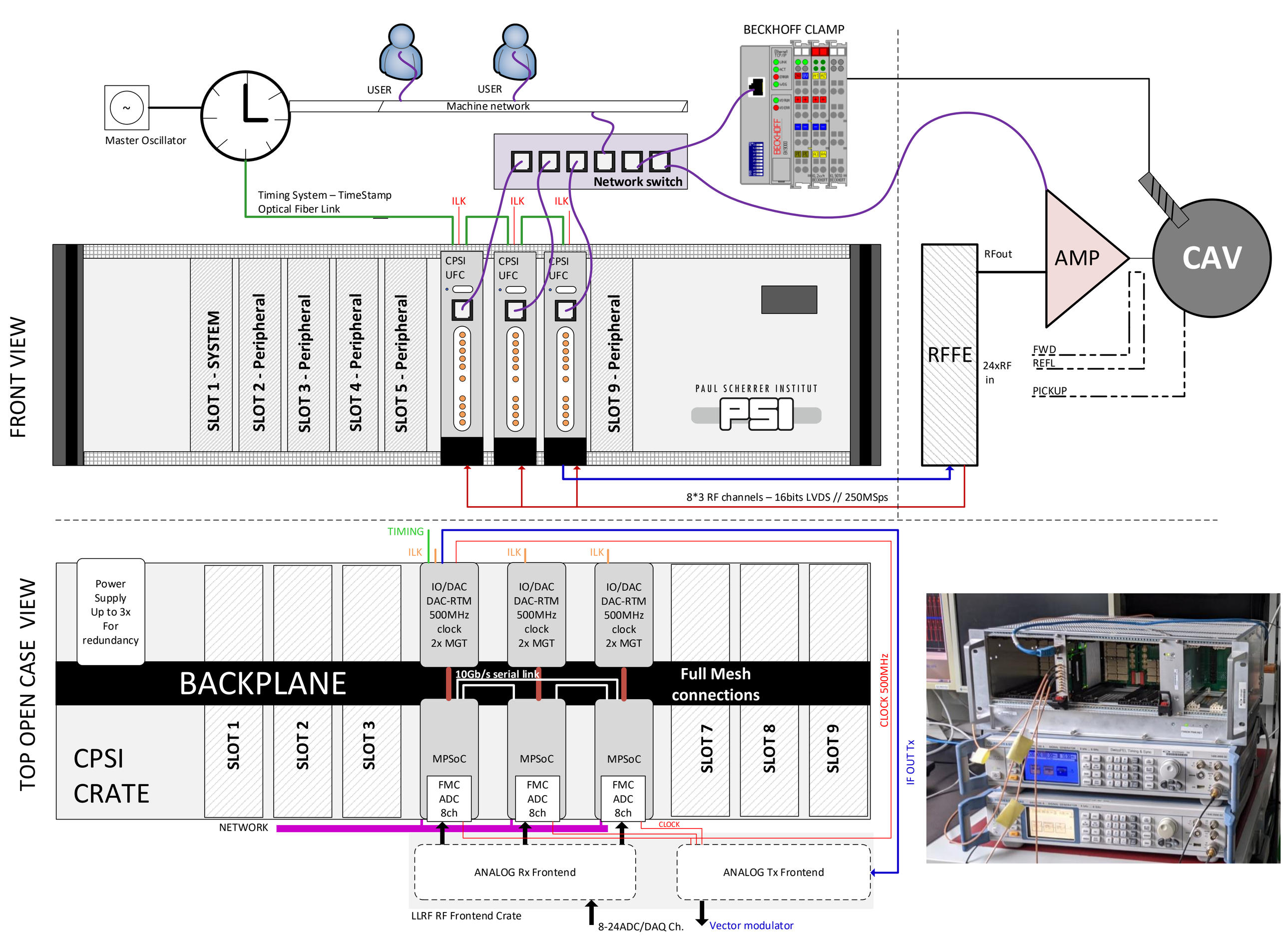

Fig. 1: CPSI-Crate 24 Ch. in LLRF Application Hardware – Used in the lab

In the use case for LLRF, the digital part with ADC, FPGA/CPU and DAC is located in the CPCI-serial crate. Due to modularity the LLRF can be scaled up easily for more ADC channels, typically 8 channels per slot. The LLRF frontend is built in a separated box. Coaxial cables are used in between for the IF signals. The cavity resonance tuning control algorithm is done in software in the LLRF CPU, the motion part with motor controller and driver is split and done with standardized motion components. There is high potential for synergies at PSI such as BLM and ICT measurements.

SoC Level

VIVADO AMD XILINX

AMD/Xilinx MPSoC Zynq US+ xczu11eg-ffvc1760-1-e
APU: Quad-core Arm© Cortex A-53 up to 1,5GHz
RPU: Dual-core Arm© Cortex-R5F MPCore up 600MHz
Dynamic Memory Interface x16: DDR4 w/o ECC; x32/x64
Static Memory Interfaces: NAND, 2x Quad-SPI Connectivity
High-Speed Connectivity PCIe® Gen2 x4, 2x USB3.0, SATA 3.1, DisplayPort, 4x Gigabit Ethernet
General Connectivity 2xUSB 2.0, 2x SD/SDIO, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO
System Logic Cells (K): 653
CLB Flip-Flops (K): 597
CLB LUTs (K): 299
Max. Distributed RAM (Mb): 9.1
Total Block RAM (Mb): 21.1
UltraRAM (Mb): 22.5
CMTs:8
DSP Slices: 2,928
PCI Express® Gen 3x16: 4
150G Interlaken: 1
100G Ethernet: 2
AMS - System Monitor: 1
GTH 16.3Gb/s: 32
GTY 32.75Gb/s: 16

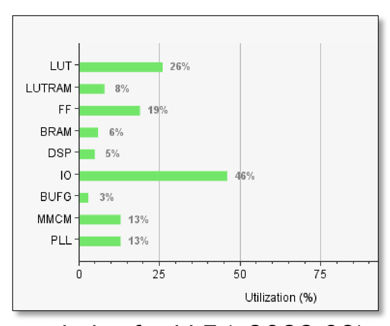

Fig. 3: PL Usage statistics for LLF (v2022-09)

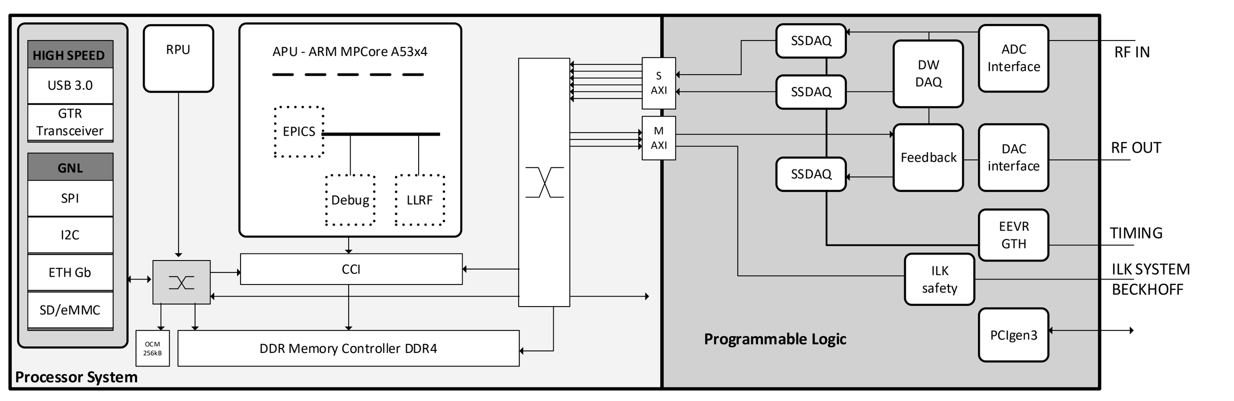

Fig. 4: SoC Architecture synoptic PS/PL

SW architecture

The MPSoC allows to embed software component in a single chip. It has been possible to run EPICS server and develop specific LLRF High-level application.

DDC A/Phi: SR 97,7 KS/s 16 Ch (DAQ Tuning)
DDC A/Phi: SR 7,8 MS/s 28 Ch (Scope)
Debug Raw data: SR 250 MS/s 8 Ch 0,5 ms duration & 16Mb data storage post-analysis
Post Mortem dump: 32 Ch. 0,05sec duration & 200Mb data storage post analysis

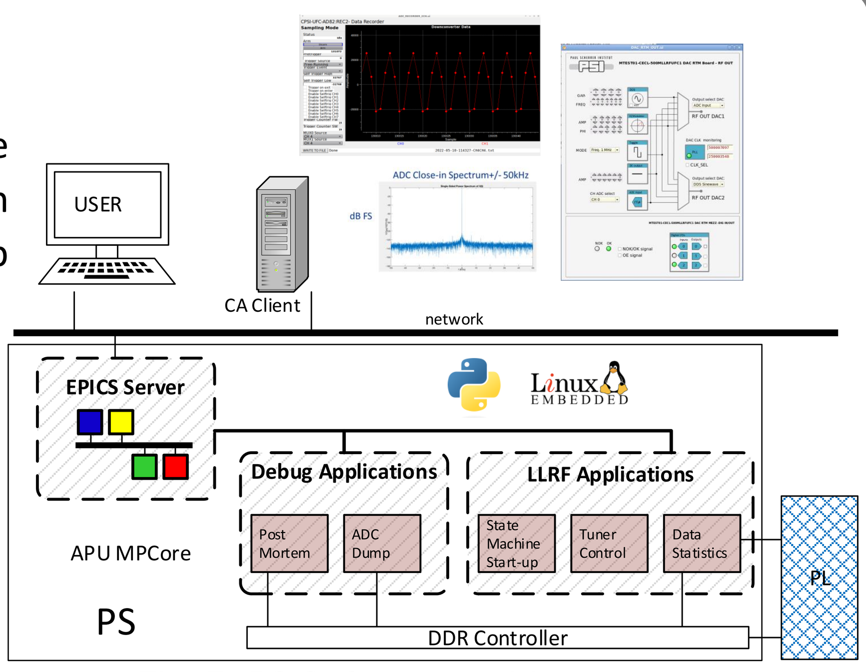

Fig. 5: PS Software architecture at a glance

A python framework is under development to validate hardware components. An automatic test report is generated to help commissioning CPSI-Crate and its sub-parts. Additionally a specific hardware in the loop to test ADC/DAC interface is foreseen to help commissioning and/or debugging.

FW architecture

The FW LLRF SLS-2 architecture is intensively using blocks from PSI library.
https://github.com/paulscherrerinstitute/psi_fpga_all
It consists in having feedback control with low latency (<1,0 us) and digital down converter to perform diagnostic. Additionaly a frequency sweep can be used to condition cavity and pulse waveform can be downloaded in feed-forward loop. Interlock as well as embedded timing receiver is being integrated at FW level.

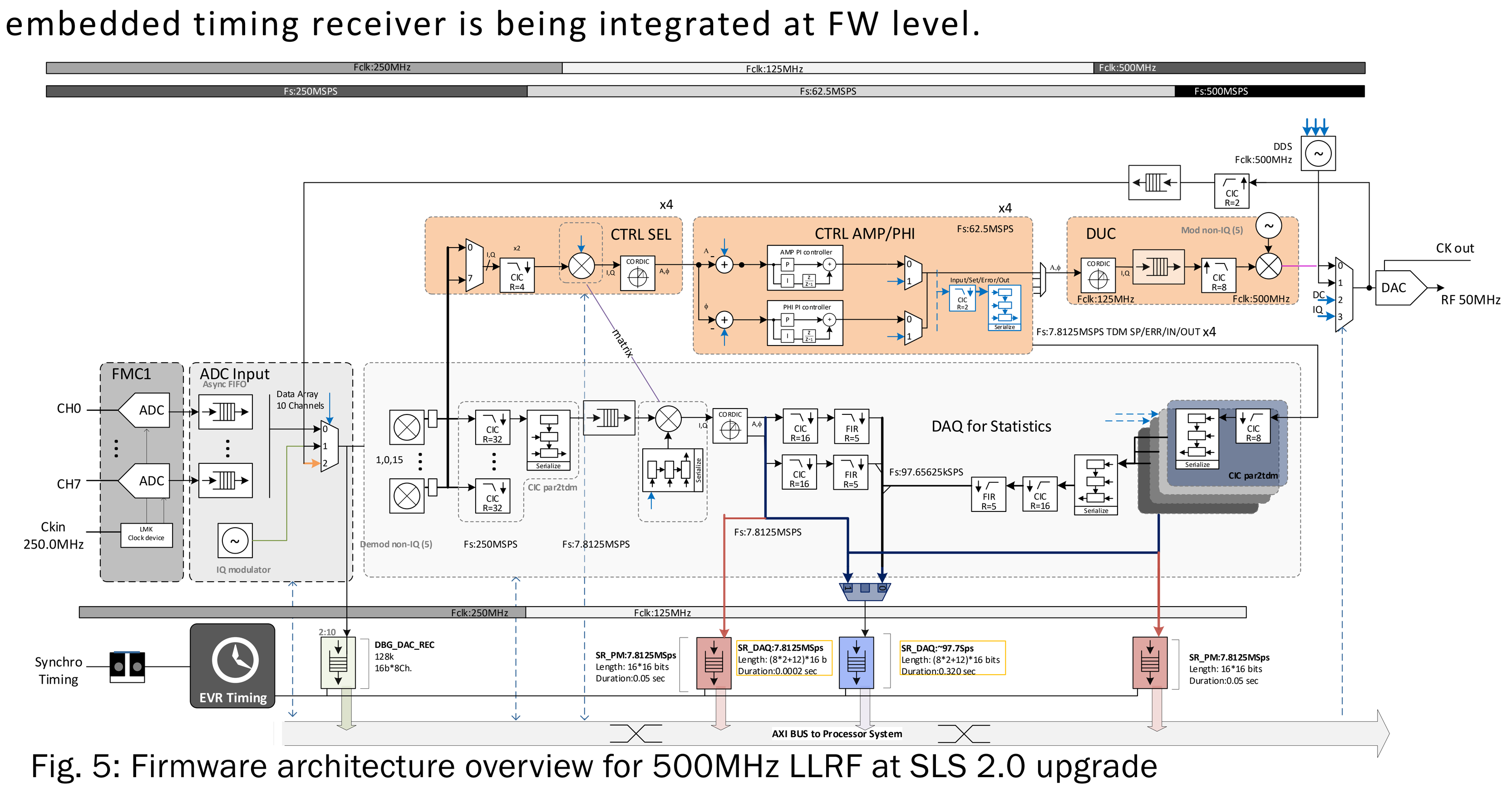

Fig. 5: Firmware architecture overview for 500MHz LLRF at SLS 2.0 upgrade

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Conclusion

The use of Open CPSI-S backplane and boards pinout standard proves the potential of the platform to be a good candidate for multiple electronics measurement and control systems. The LLRF application demonstrates that low latency feedback control can be achieved. The number of slots on the backplane with high speed communication lines allows comprehensive synchronization. The use of MPSoC Zynq US+ chip and its large number of resources ease development and redefining specification on the fly.