Status of the uTCA Digital LLRF design for SARAF Phase II

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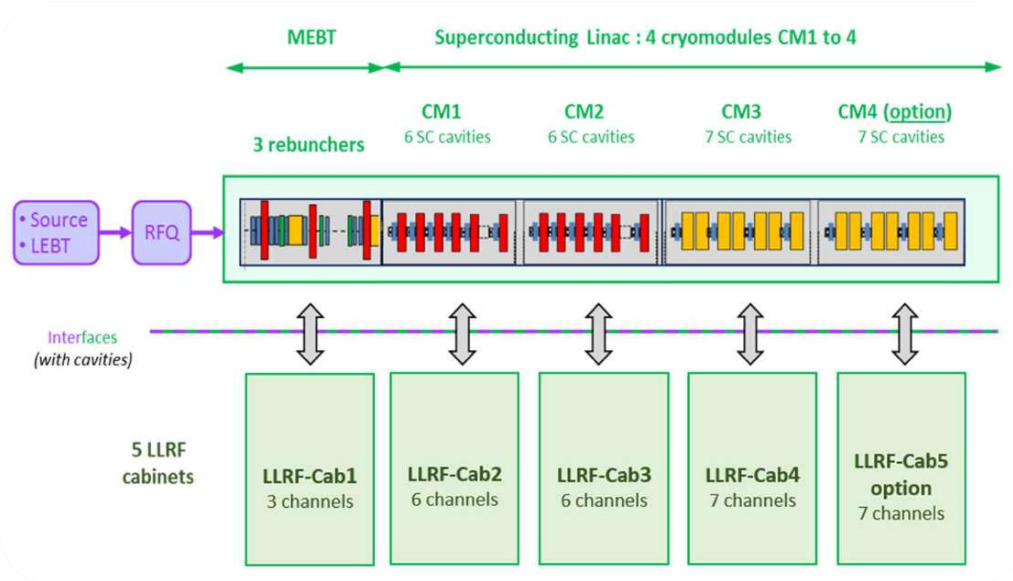
SARAF (Soreq Applied Research Accelerator Facility)

Constructed at Soreq Nuclear Research Center (SNRC). The main scientific objectives of this facility are:

- Search for Beyond Standard Model **Physics**
- **Nuclear Astrophysics**
- **High Energy Neutron** Induced Cross Sections
- Neutron Based Material Research/**Neutron Based Therapy**
- Development of New **Radiopharmaceuticals**
- Accelerator based **neutron imaging**

Superconduction Linear Accelerator	
Parameter	Value
Ion Species	Protons/Deuterons
Energy Range	1. 5 Me. V/u – 40 Me. V
Current Range	0. 04 – 5 m. A CW
Operation	6000 hours/year
Availability	> 90%



SARAF - LLRF Requirements

The LLRF is a key component to regulate RF filed inside the cavities. It operates in closed loop maintaining the cavity gradient and phase stability when operating the cavity with beam.

Operating frequency range: **175-177 MHz**

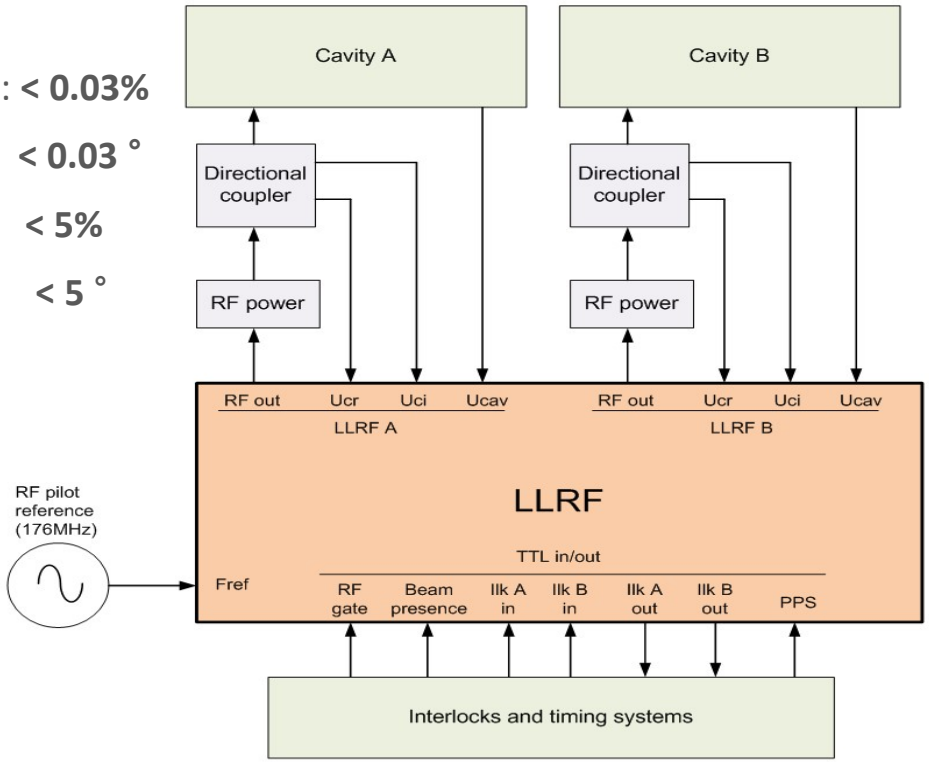
Delay: **< 1us**

Amplitude measurement RMS error: **< 0.03%**

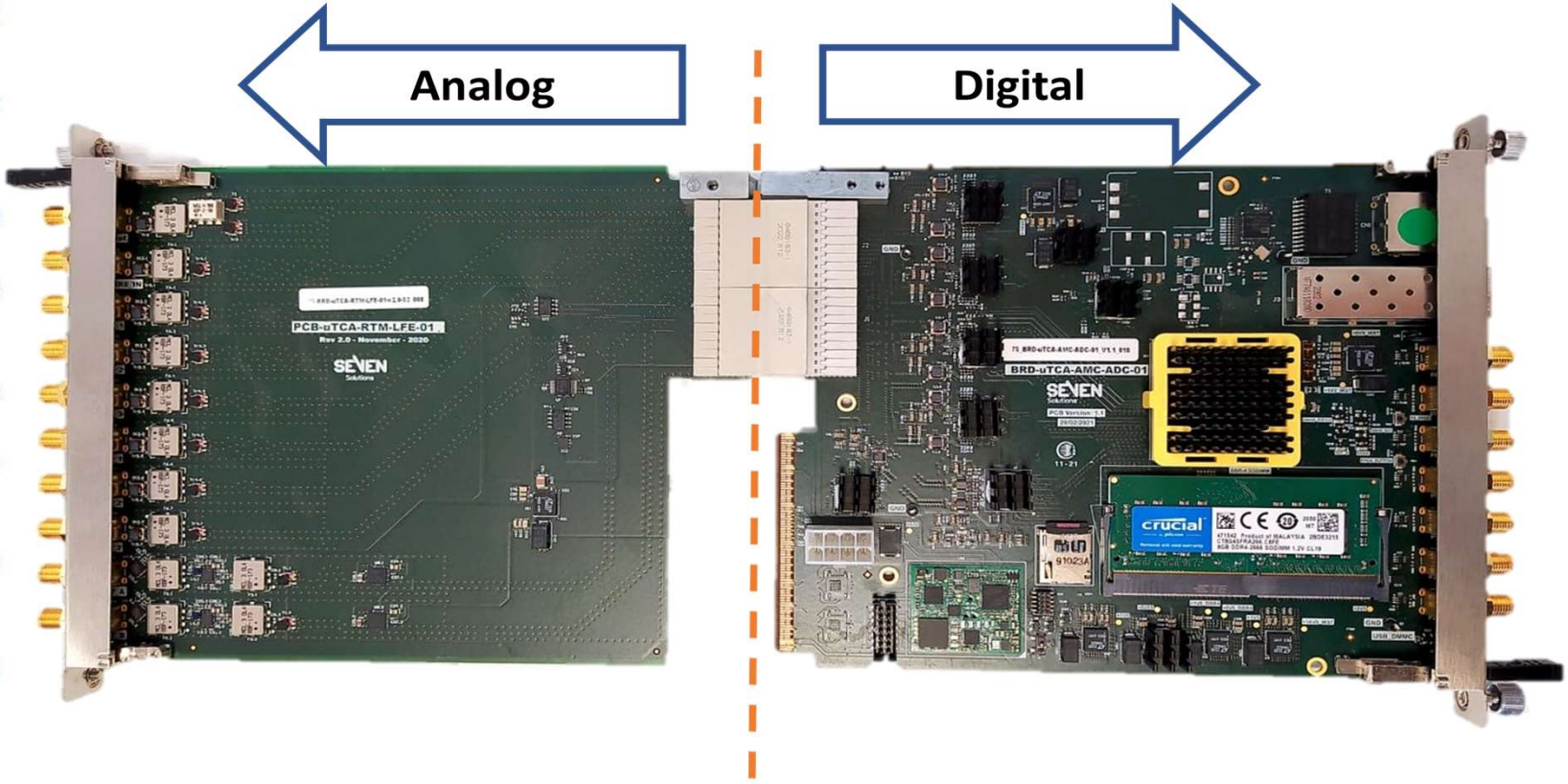
Phase measurement RMS error: **< 0.03 °**

Output amplitude uncertainty**:** **< 5%**

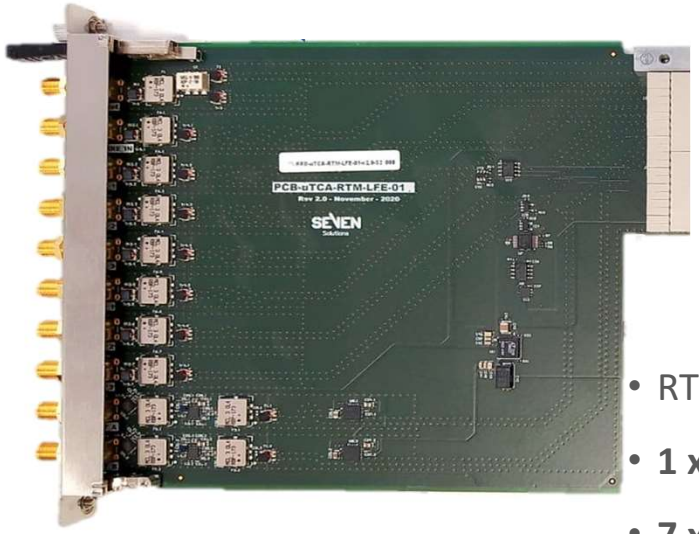
Output phase uncertainty: **< 5 °**



2 LLRF on a single pair of uTCA.4 boards

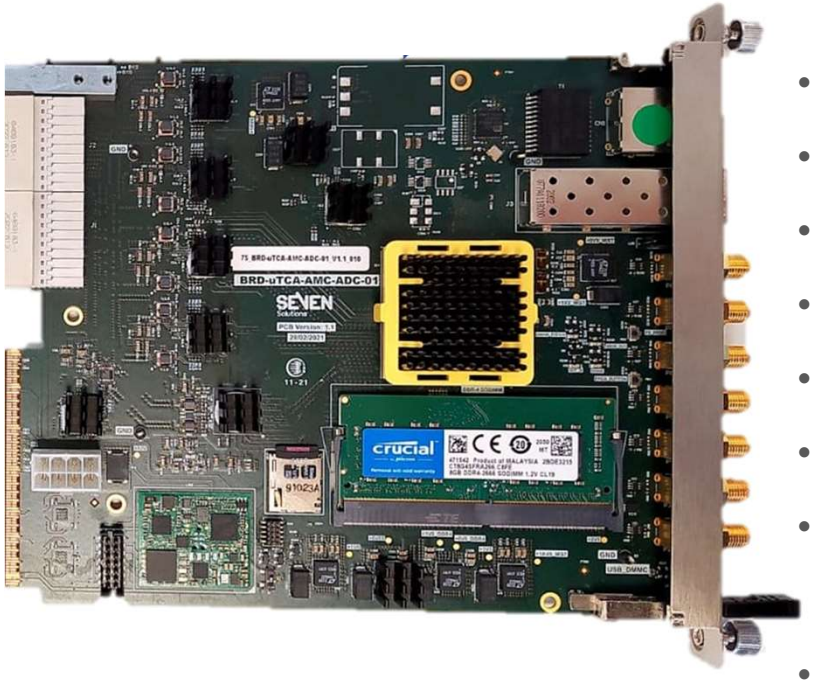


LFE RTM – LLRF front-end RTM



- RTM with double height and mid-size form factor **uTCA.4**
- **1 x RF MO Ref.**: 176 MHz sine wave for LLRF reference
- **7 x RF inputs** to monitor up to two cavities
- **2 x RF outputs** to drive up to two cavities
- **Direct sampling** architecture
- RF input power dynamic range: **[-60,+10] dBm**
- Maximum RF output power: **+10dBm**
- **Fail-safe for overheating** mode
- EEPROM memory

ADC board – AMC Digitizer Controller

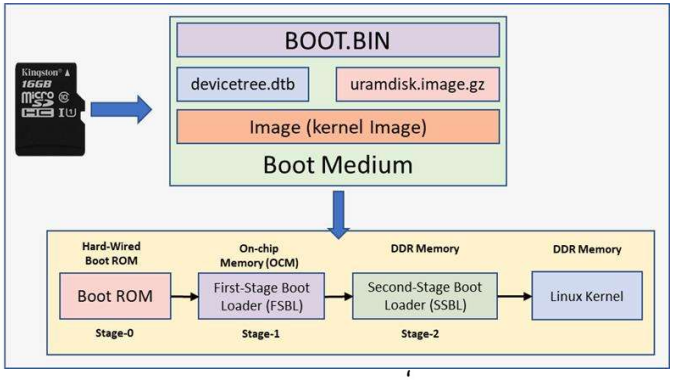


- **8 x ADC** channels
- **2 x DAC** channels
- **16 bits, 250MSPS ADCs - QDR LVDS** interface
- **16 bits, 1.5 GSPS DACs – DDR LVDS** interface
- **Zynq UltraScale+ FPGA** from Xilinx
- **PLL** for low phase noise distribution clocks
- **8GB DDR4** for processor and data storage (postmortem analysis)
- ETH & SFP port (**White Rabbit compatible**)
- uTCA MMC controller
- **Fail-safe for overheating** mode
- uSD socket, uUSB port

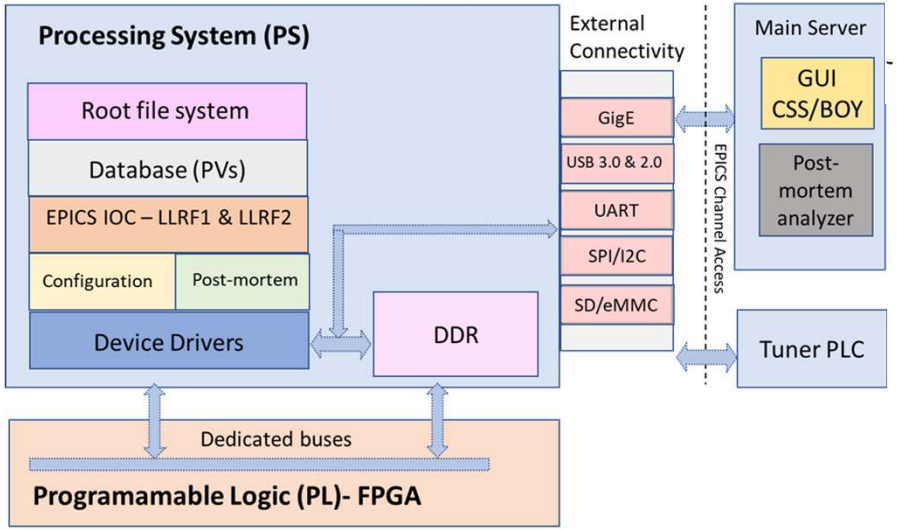
uTCA chassis for SARAF

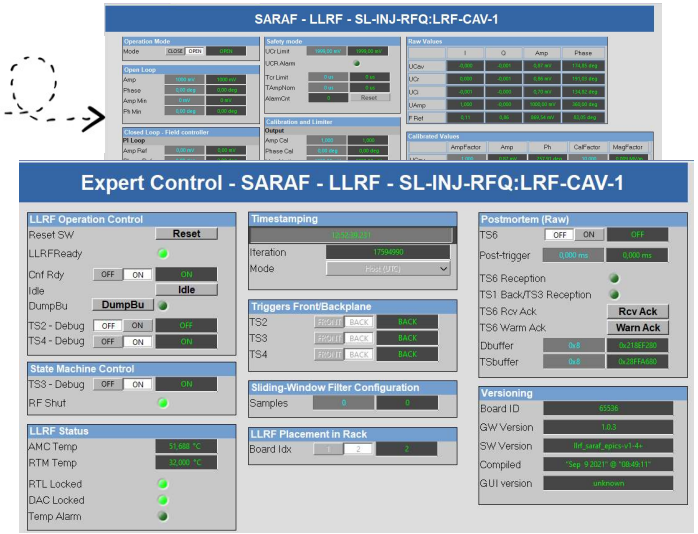
- NATIVE-R2 uTCA.4 from N.A.T. **(up to 5 LLRF boards - AMC + RTM)**
- NAT-MCH-**PHYS80**
- NAT-MCH-**RTMCOMex-E3**
- Timing gating and triggers:
  - 4 x **shared bidirectional backplane lines**
  - 4 x **point-to-point backplane lines**

Software architecture – 2 LLRF on 1 single board



- Buildroot for OS Image:
  - BOOT.bin: FPGA image
  - Uboot: instructions to boot the devices
  - Devicetree: mapping of devices of the system
  - Image: Linux kernel image

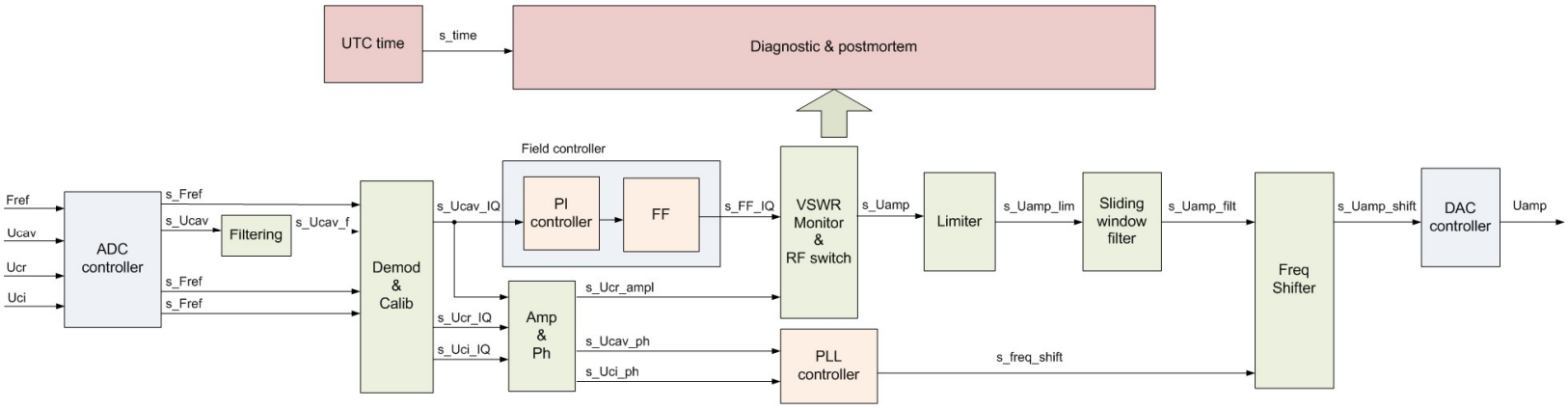




✚ EPICS as Control system (asynPortDriver, databases, PV, autosave…)
Integrated libraries for FPGA/ARM communication (AXI based)

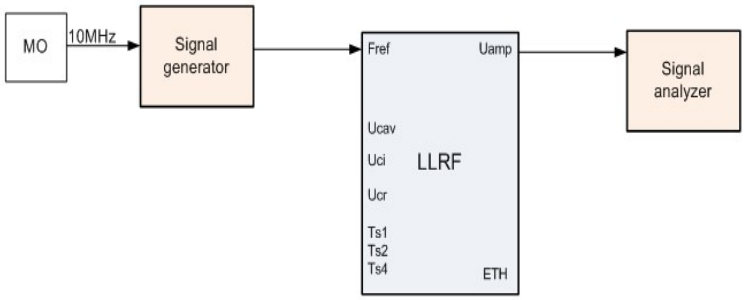
2 LLRF IOCs with complete functionality

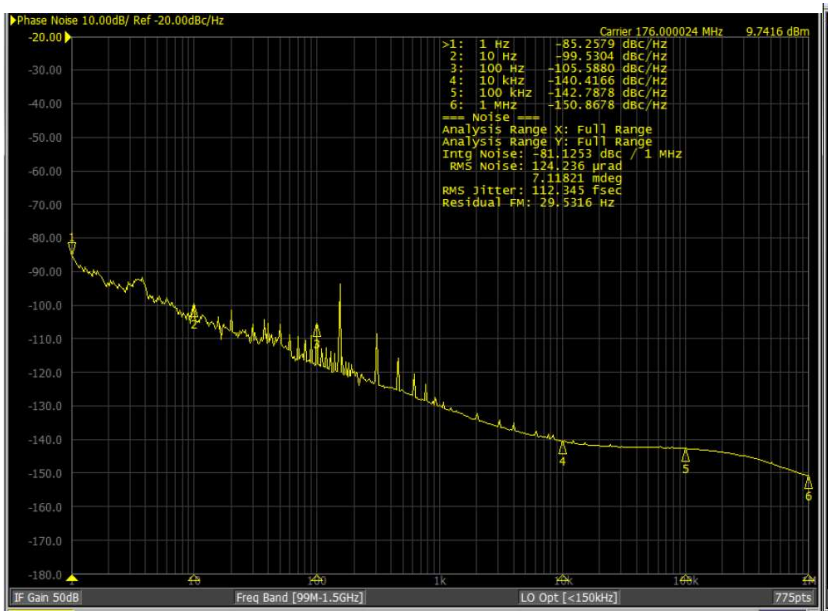
Gateware Architecture



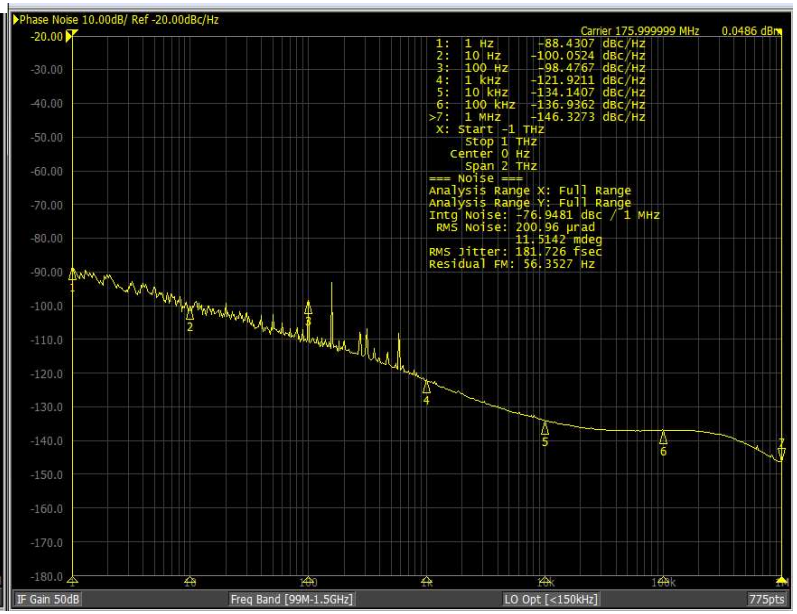
- **Direct sampling** architecture
- **Amplitude and phase loop controller** in pulsed and continuous wave
- **Feedforward** for beam loading compensation
- **VSWR** (arcing/reflection) detection and handling events
- **Pulse shaping** feature for smoothing RF pulses
- Provides information for **step tuner motors**
- **Fast output interlock** system (Machine protection)
- **Postmortem up to 0.2 us resolution** with selectable event triggers and configurable capture parameters. MATLAB, python, CSS/BOY libraries for post processing
- **RF output frequency shift +/- 1MHz**
- **Digital PLL** for tracking resonance frequency
- **White-Rabbit** and IEEE-1588 protocols.

Low jitter addition at the outputs





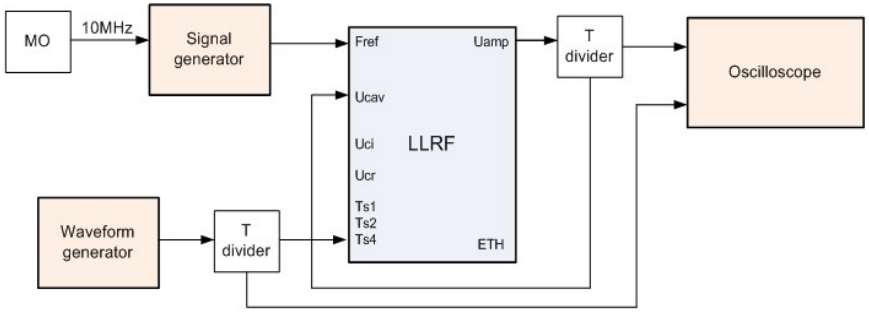
Jitter signal generator: RMS 112 fsec

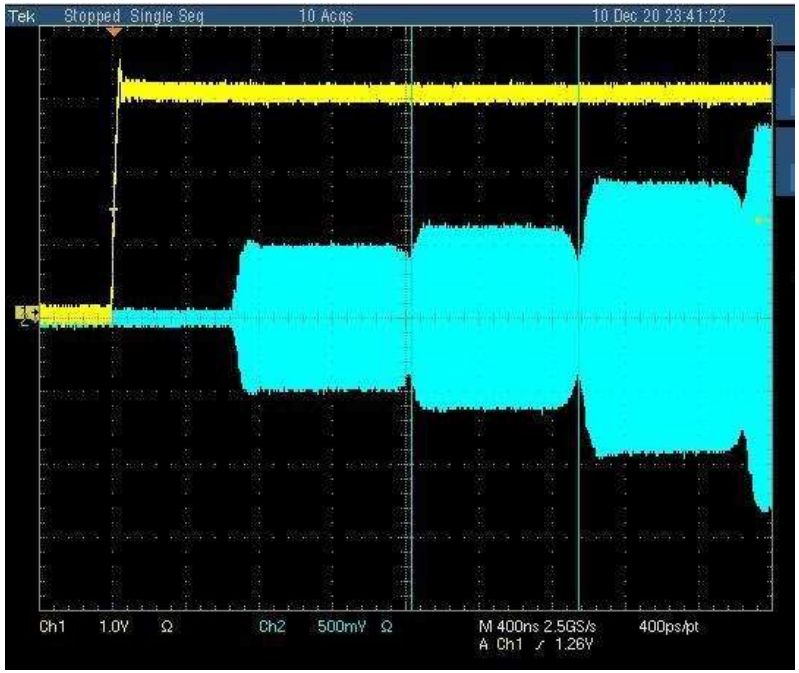


Jitter signal generator: RMS 182 fsec

Additive Jitter: RMS 70 fsec
Integration band: 1Hz - 1MHz

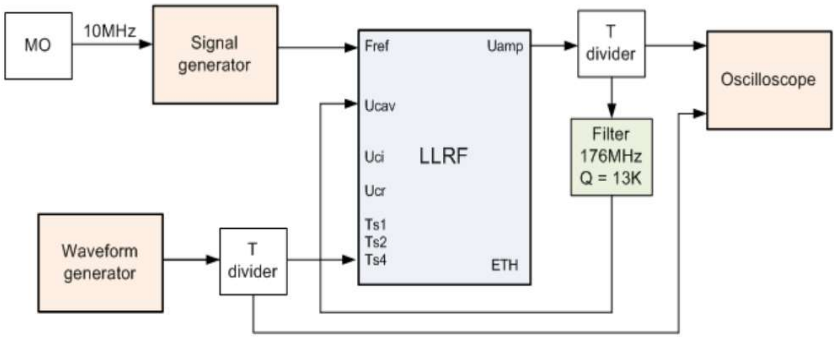
Low response time – PI delay

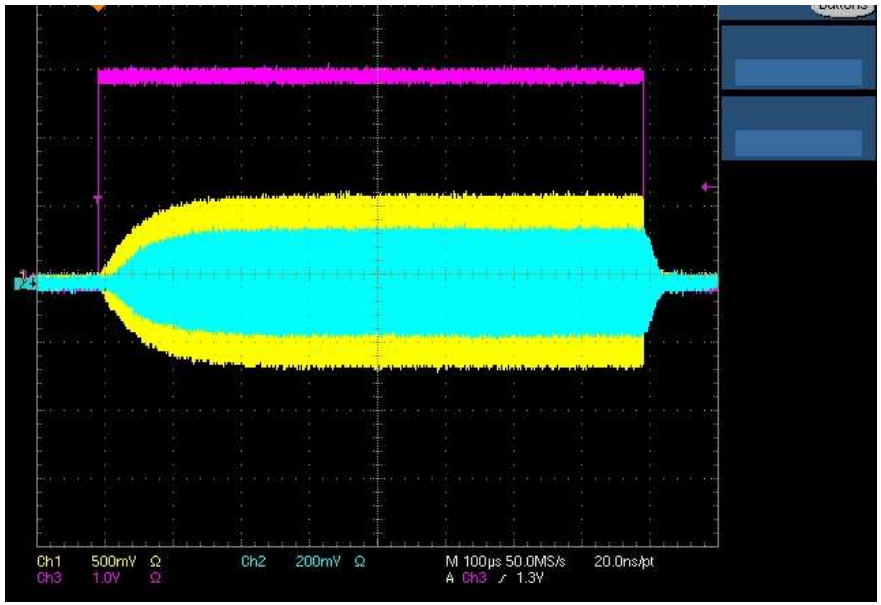




The duration of the steps produced by the effect of Kp determine the **total loop delay** of the system from RF-in to RF-out (**delay < 1us**)

PI for amplitude & phase regulation

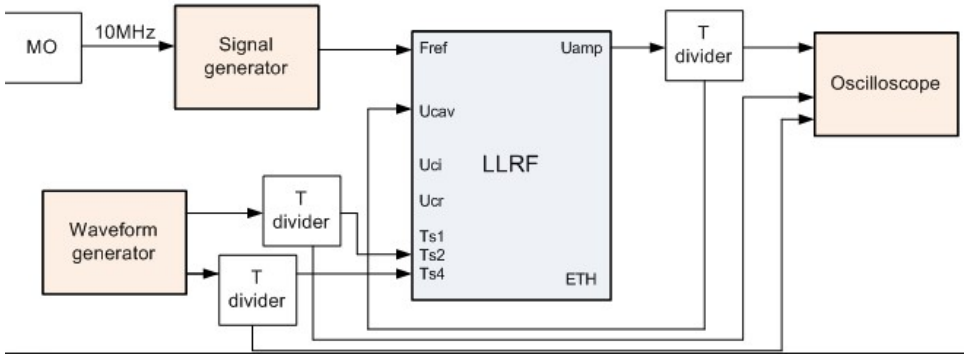


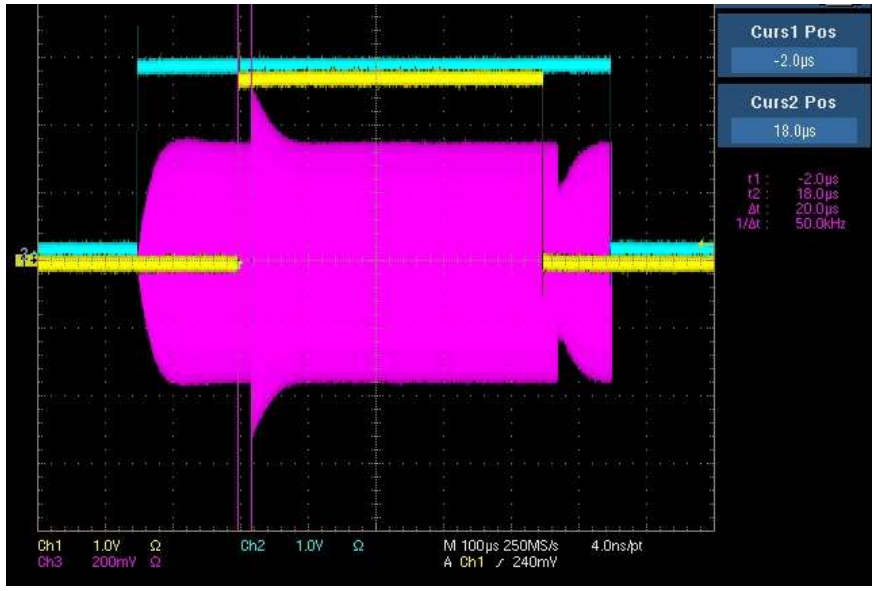


In pink, RF gate signal
In yellow RF output
In blue UCav

A high Q filter is used to emulate the cavity behaviour.
The PI controller keep constant the cavity field

Feedforward feature



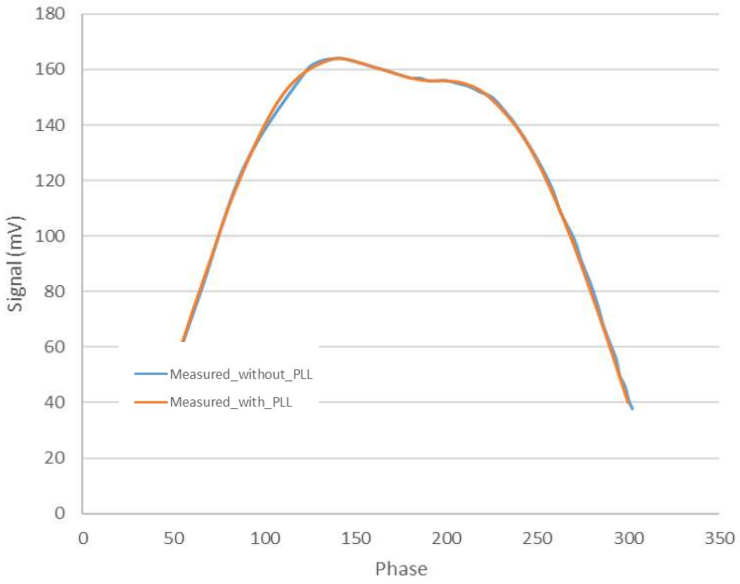


In blue RF gate signal
In yellow beam presence gate
In Pink RF output

Configurable gain and phase used to compensate the beam loading

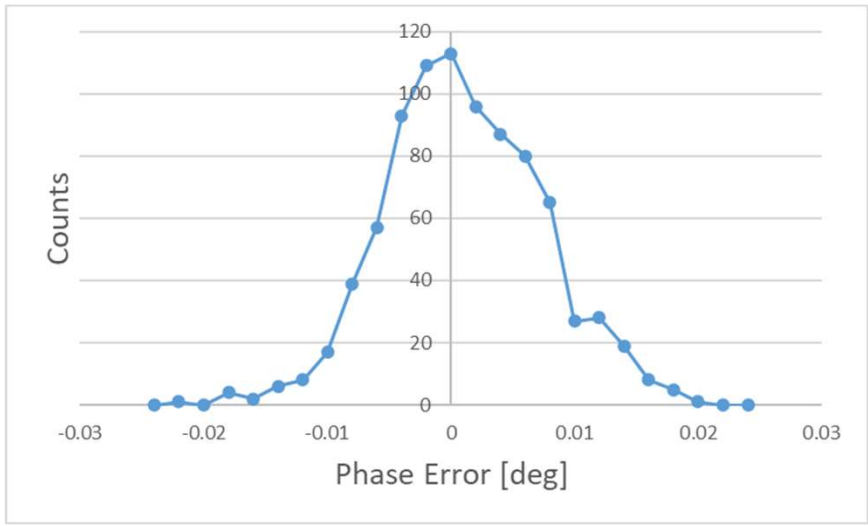
Test at CEA lab

PLL Capability



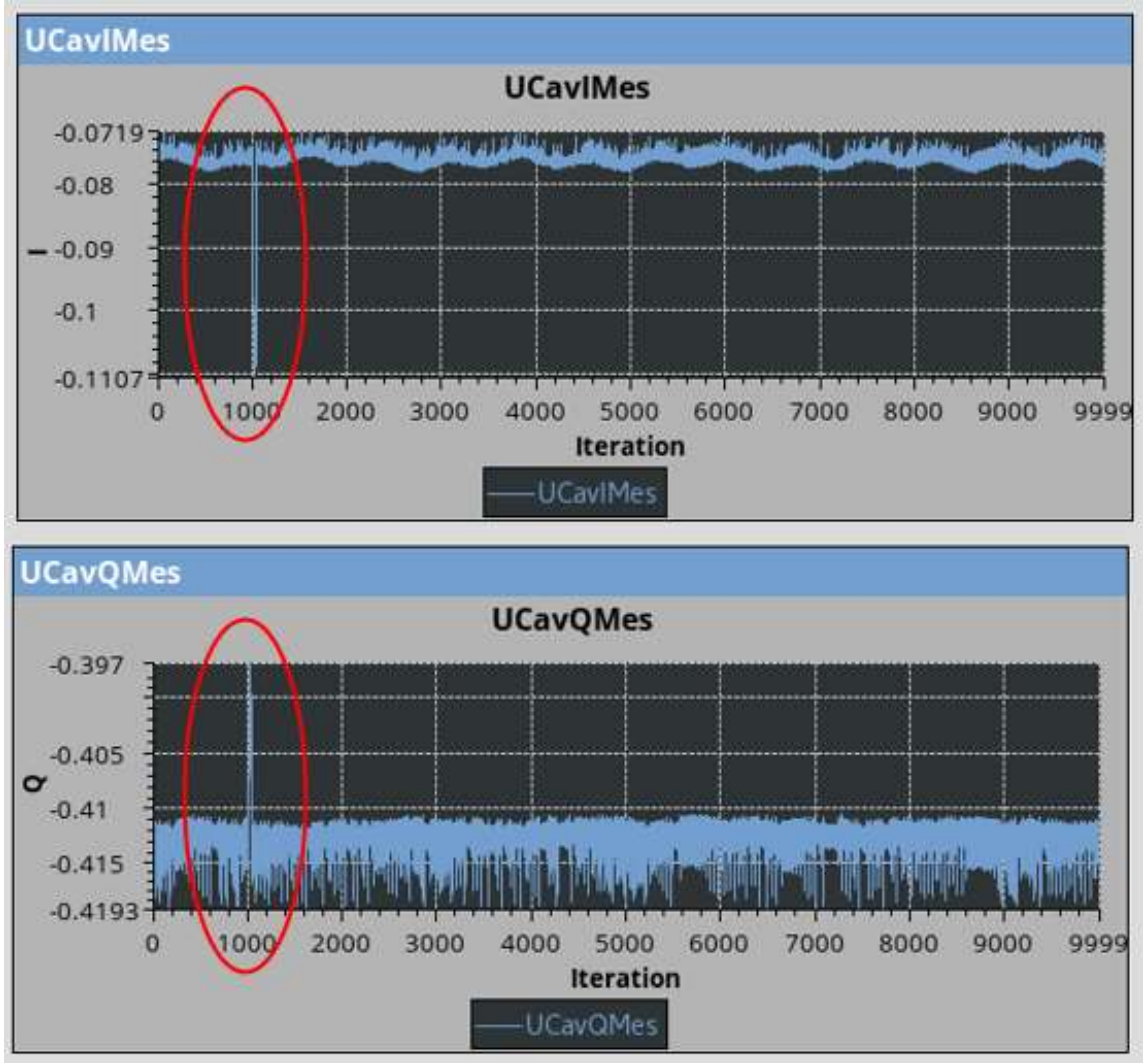
Frequency closed loop for **tracking the cavity resonant frequency** in open loop

Phase Stability in ECTS



Achieved phase stability in tests with the superconducting HWRs: **~0.006 deg [RMS]**

Short beam pulse detection during SNRC commissioning



How can we help you?

Introduction to Orolia

SARAF

LLRF hardware architecture

LLRF Gateware & Software architecture

System performance

Contact Us

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