

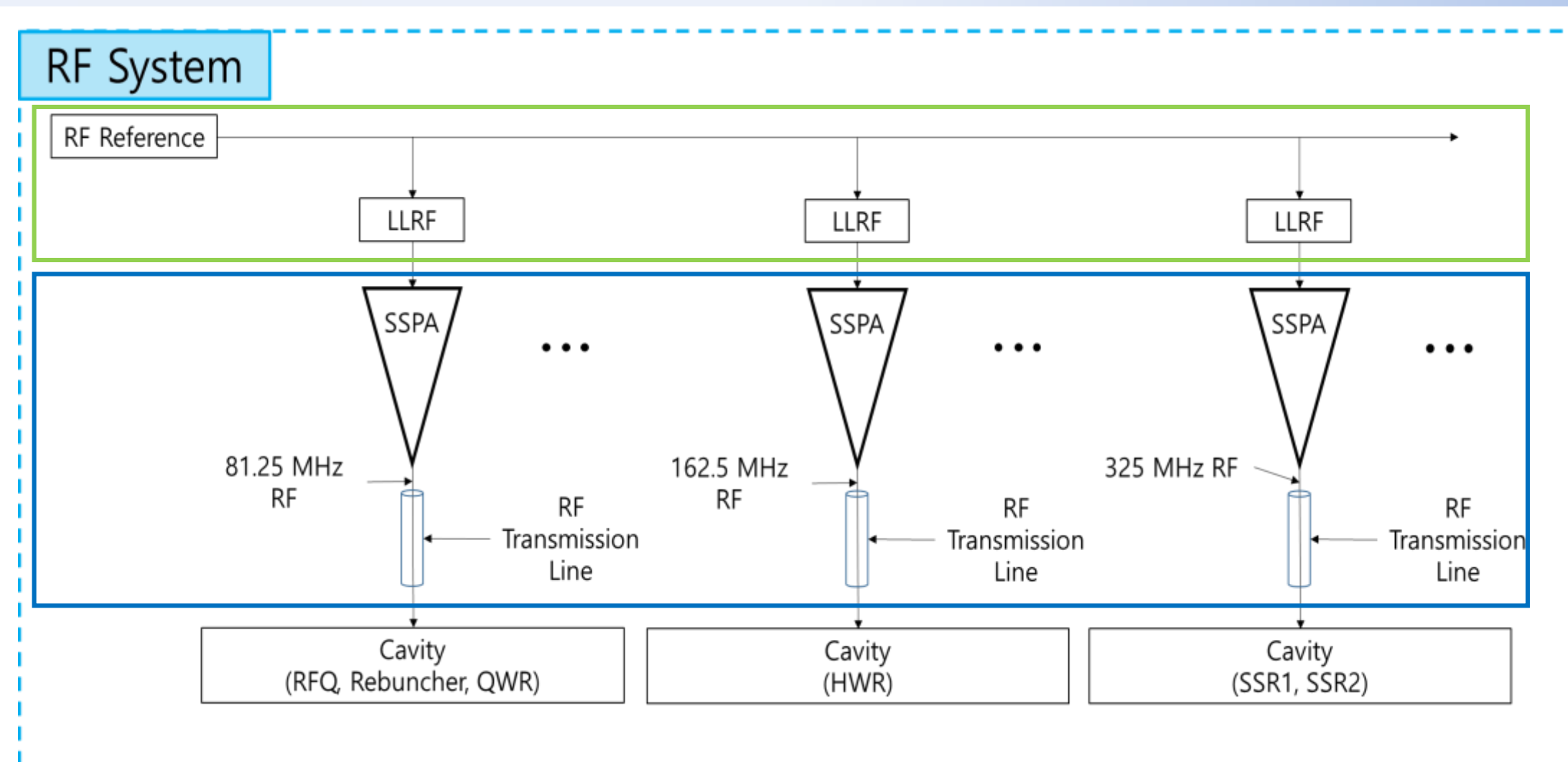
Development of a Digital LLRF System for RAON SCL3

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Abstract

Recently the test of superconducting cavities and the cryomodules of the low energy linear accelerator part (SCL3) of a heavy ion accelerator, RAON has been finished. They are installed and the preparation process for the commissioning is ongoing in Daejeon, Korea by Rare Isotope Science Project (RISP) team in Institute of Basic Science (IBS). The purpose of this accelerator are the generation of rare isotope by ISOL (Isotope Separation On-Line) and its acceleration for the nuclear physics experiment. The operating RF frequencies for SCL3 are 81.25 MHz and 162.5 MHz. Every cavity can be controlled independently for the flexibility to accelerate the various A/q ions. Recently the development, evaluation and installation of the digital LLRF based on the FPGA technology have been finished. The self-excited loop (SEL) and the generator-driven-resonator (GDR) algorithm are implemented and they were tested in the SRF test facility. In this presentation the status and test result of RAON LLRF controller will be described.

RAON RF CONTROL SYSTEM



Layout of RAON RF System



Installed LLRF

- For the RF control of 1 cavity, 1 SSPA(Solid State Power Amplifier / 1 LLRF (Low Level RF) pair is planned at RAON accelerator.

Specification of RAON RF Control System

RF Dynamic Phase Error Requirement	± 1 degree (Peak-to-Peak)
RF Dynamic Amplitude Error Requirement	± 1 % (Peak-to-Peak)

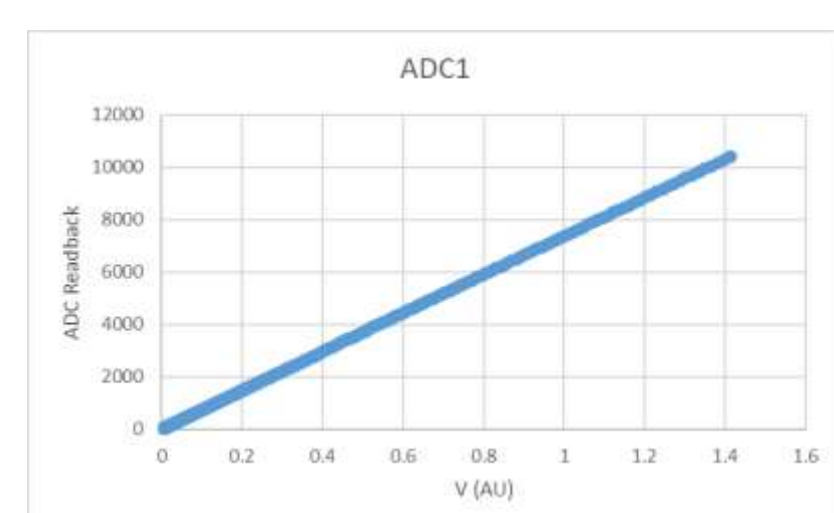
- For the cavity resonance control, the frequency error of cavity is measured by LLRF and the information is sent to tuner control system.

LLRF FOR RAON SCL3

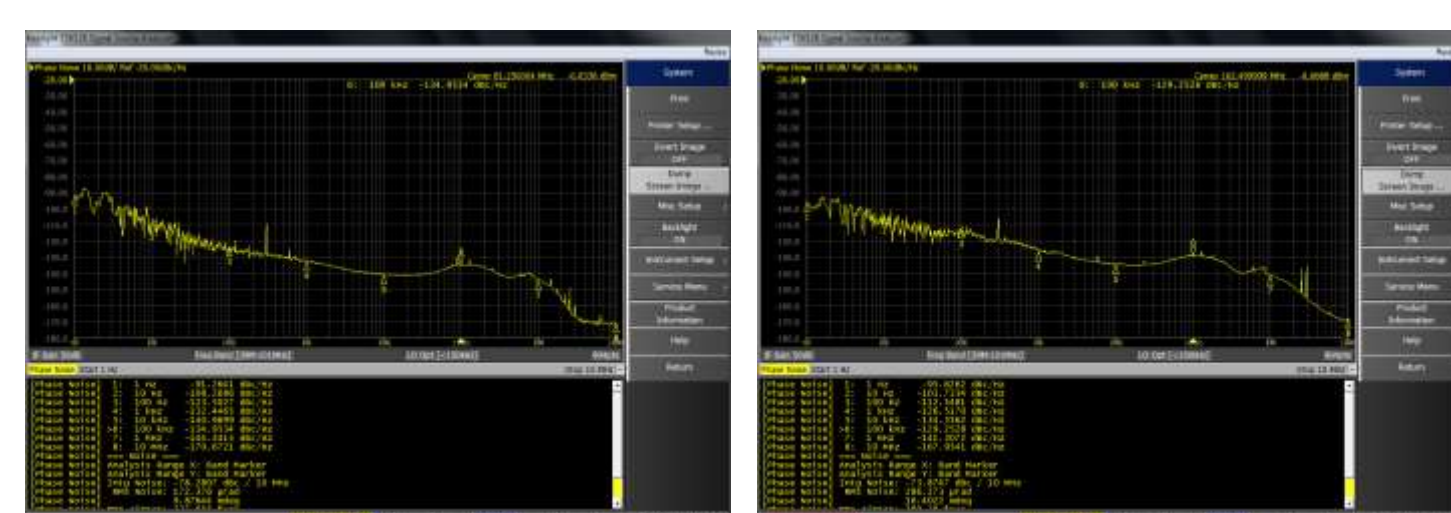


Item	Spec
RF Input	4
RF Output	1
RF ADC	AD9653(16 bit, 4 ch, LVSD)
SoC	Xilinx Zynq Ultrascale ZU9EG
EPICS IOC	In Arm core of Zynq
Clock Gen	LMK04828 PLL

- With PLL circuit, the sampling of ADC, DAC/clocking of FPGA can be changed easily.
- One hardware can support any cavity in SCL3 (low energy, 81.25 and 162.5 MHz) and SCL2 (high energy, 325 MHz)
- Generator-Driven mode and Self-Excited Loop algorithm have been implemented and being tested.



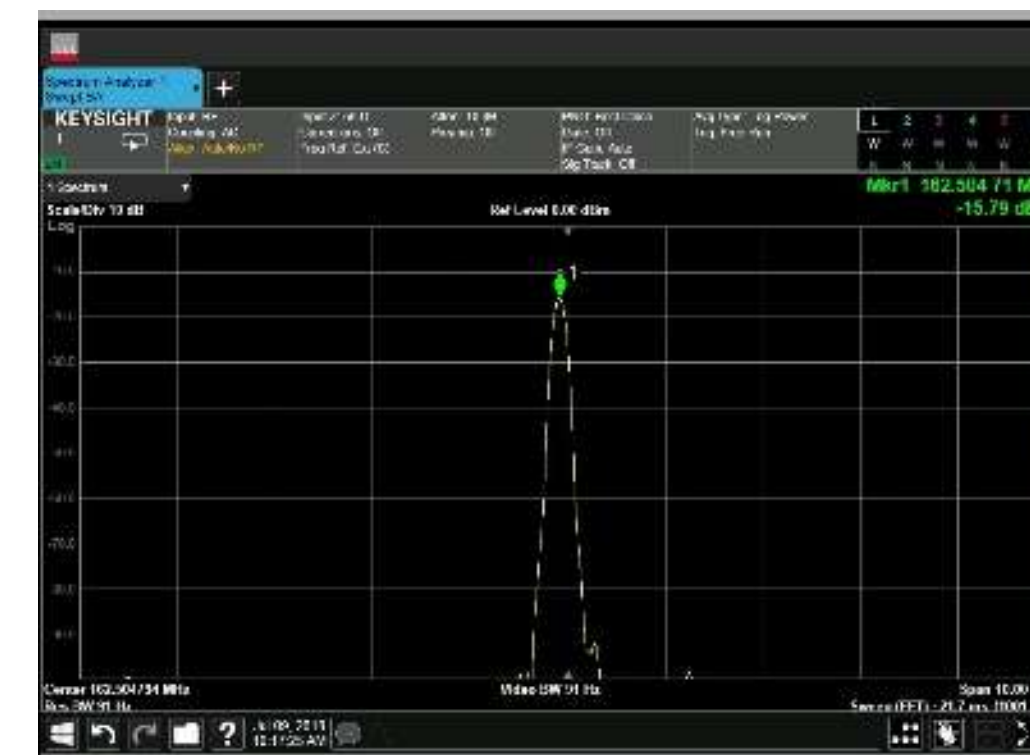
ADC Linearity Test
($P_{in} = +3 \sim -40$ dBm)



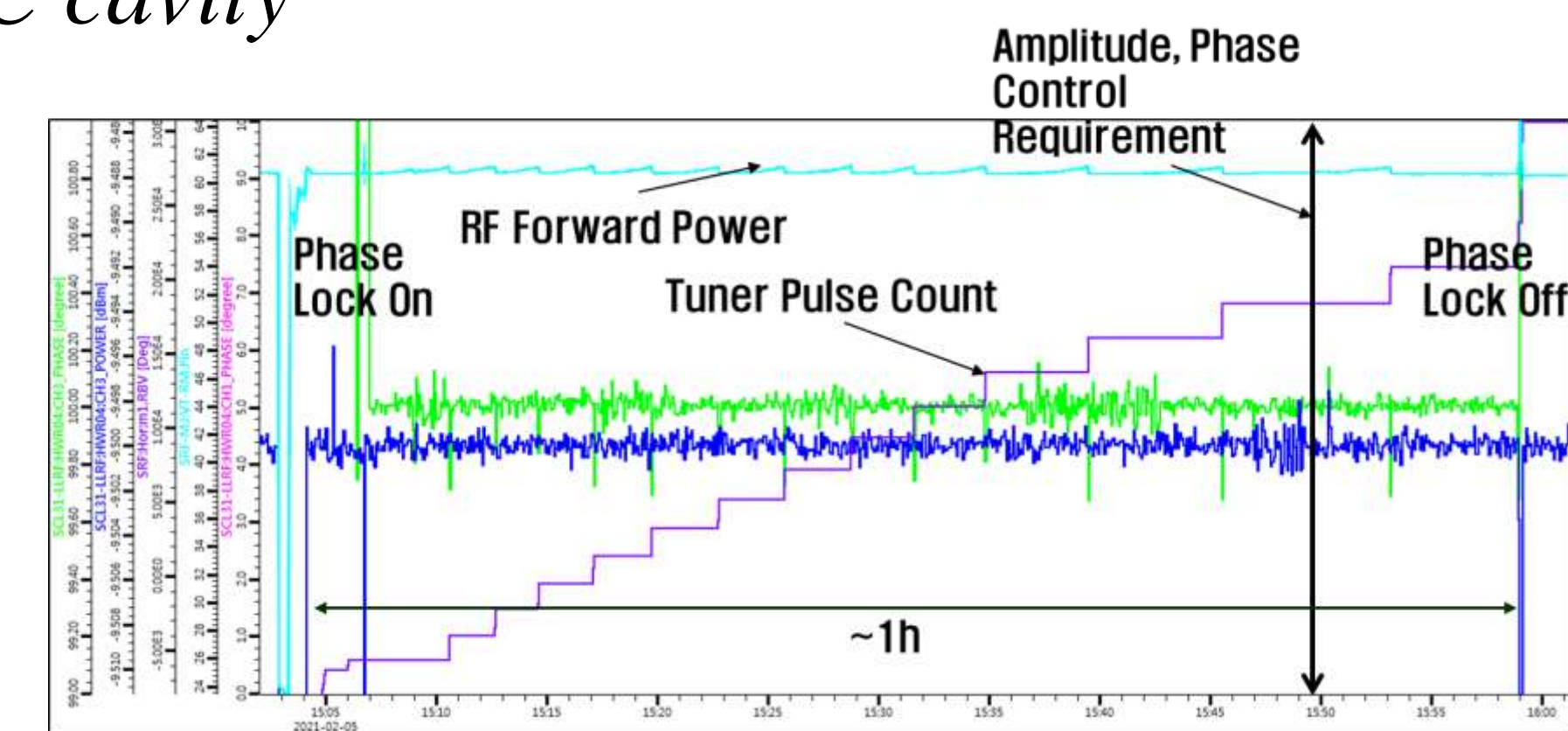
DAC Test @81.25 MHz, 162.5 MHz
RMS Jitter < 0.29 mdeg

SRF TEST RESULT OF DEVELOPED LLRF

- LLRF test result with SC cavity

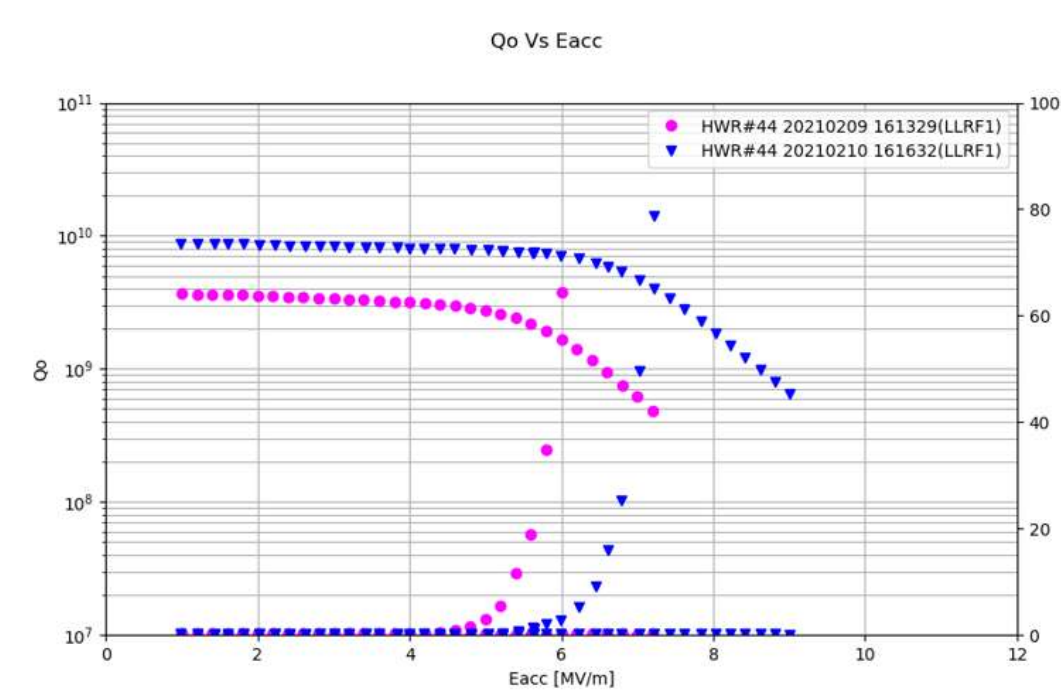


Cavity resonance frequency tracking and excitation test result with HWR SC cavity

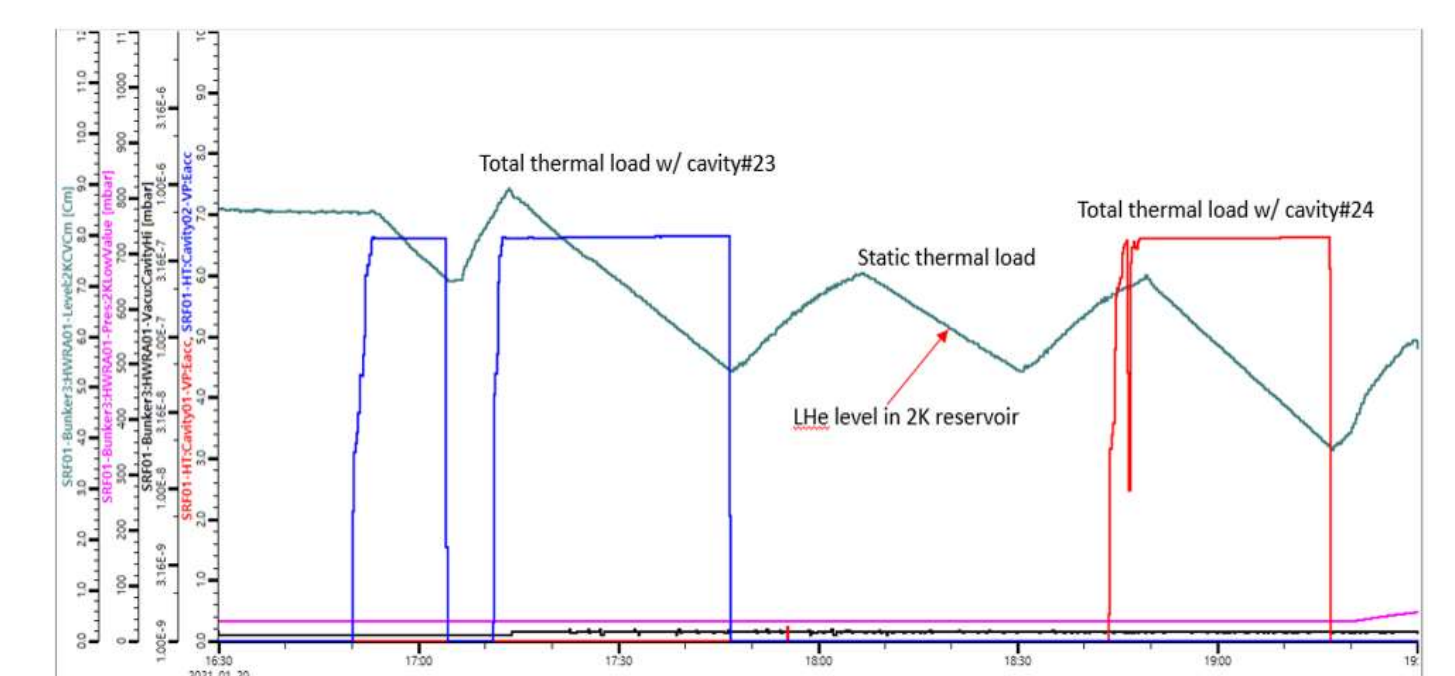


Amplitude and phase control test result with HWR SC cavity

- Amplitude control and frequency tracking test in SEL mode has been performed with QWR and HWR superconducting cavity at SRF.
- Phase and amplitude control test, resonance frequency measurement test has been conducted with SC conducting cavities.

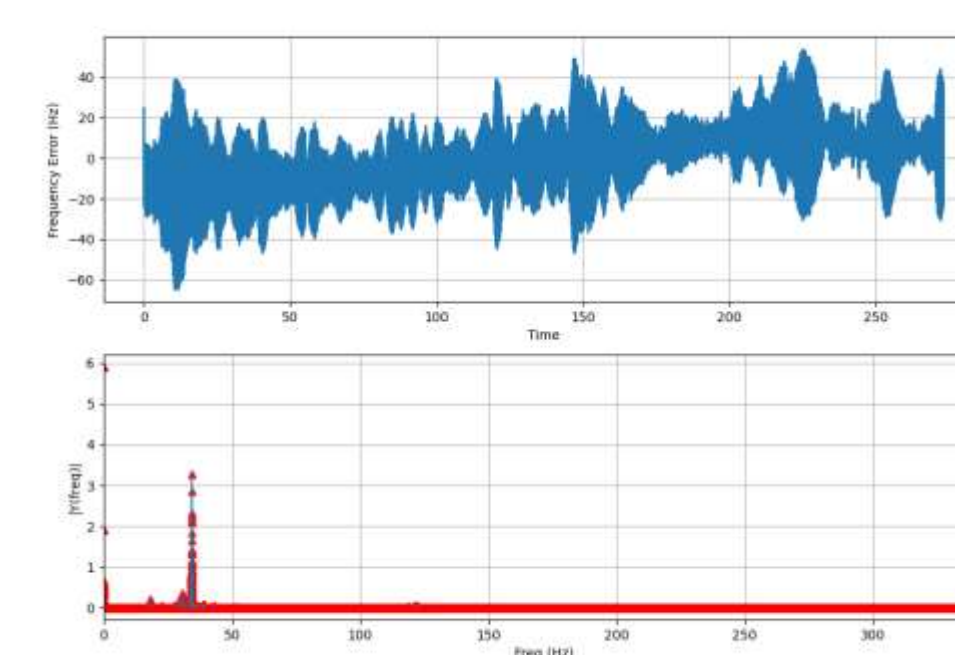


Vertical test result
(Q0 measurement in SEL mode)

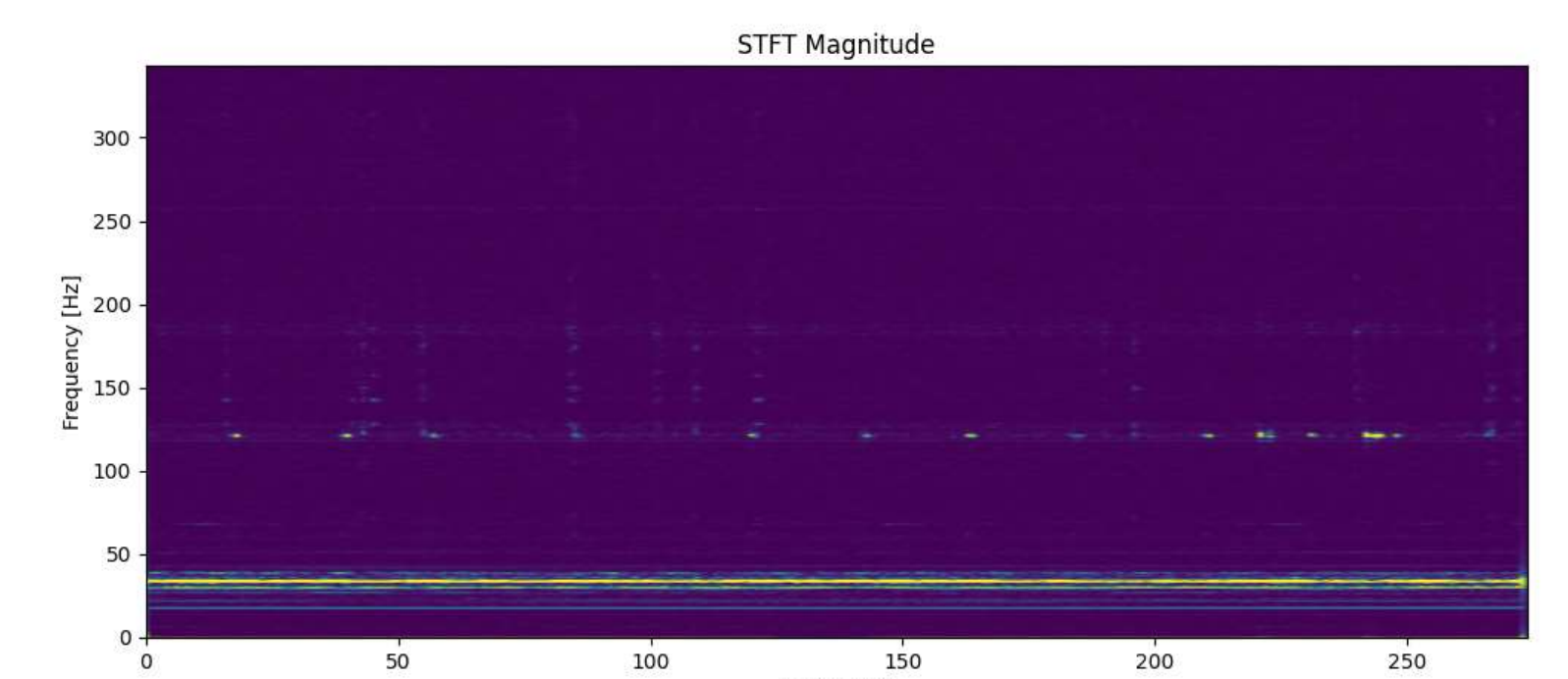


Cryomodule test result
(Dynamic heat load measurement)

- Microphonics Measurement



Top : Δ frequency vs time
Bottom : FFT result



STFT Result

- LLRF can measure the resonance frequency fluctuation according to the microphonics, etc.
- This function will be used to diagnose and reduce the microphonics at SRF test facility and accelerator site.

SUMMARY

- FPGA-based LLRF has been developed and installed at RAON accelerator.
- Implementation of Digital SEL mode and Generator Driven Mode algorithm and their verification test have been performed at RAON SRF TF.
- During the vertical test and the cryomodule test with SC cavities, the tests of SEL mode frequency tracking, amplitude control, amplitude-phase control, resonance frequency measurement have been performed and the result was successful.
- Some functions for the SRF test (microphonics measurement, etc.) were developed and implemented and its test was performed.

ACKNOWLEDGEMENT

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