

# PROGRESS OF DIAMOND DIGITAL LOW LEVEL RF

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## Introduction

- The first version of digital low level RF (DLLRF) for the Diamond Light Source storage ring and booster was developed with ALBA. Two systems were operational with two NC RF cavities since 2019. The DLLRF system for second booster cavity was tested successfully with beam this year. The DLLRF system for the third NC cavity in the storage ring is being commissioned.
- A new DLLRF system based on SIS8300-KU with RTM has been developed and tested. We are aiming to develop a common platform for the different RF systems in Diamond. It will also be our baseline design for the Diamond II. The Linac version was tested successfully to generate flat top pulse from SLED in the high power test in the Linac. The storage ring version was also tested successfully in RFTF.

## First Version DLLRF

The DLLRF was based on the MicroTCA standard. Perseus 601X with Virtex6 FPGA from Nutaq, is used as the core processor of the control algorithm. 16 Channel 14-bit ADCs and 8 channel 16-bit DACs FPGA mezzanine cards (FMC) are used for analogue input and out interface.

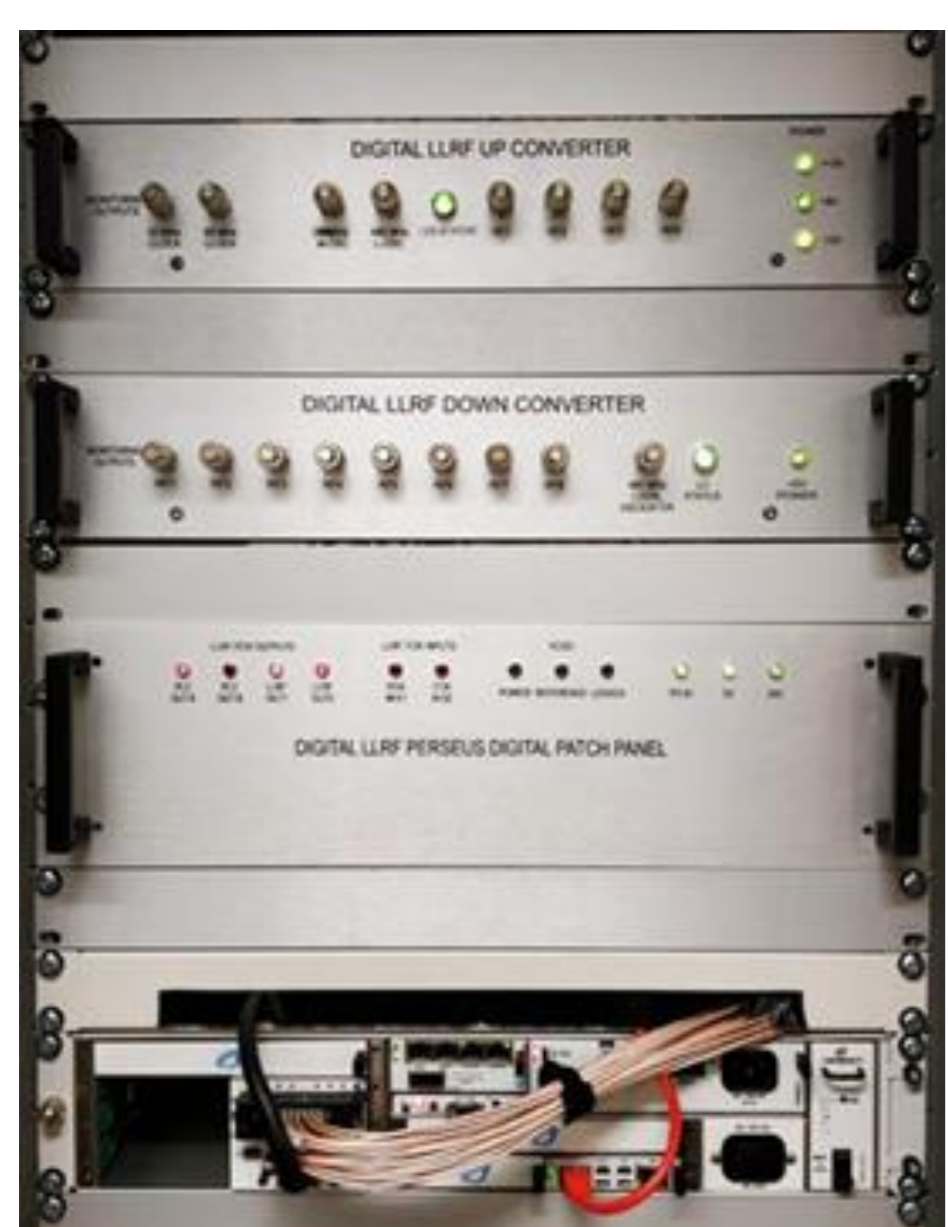


Figure 1: Installed DLLRF System.

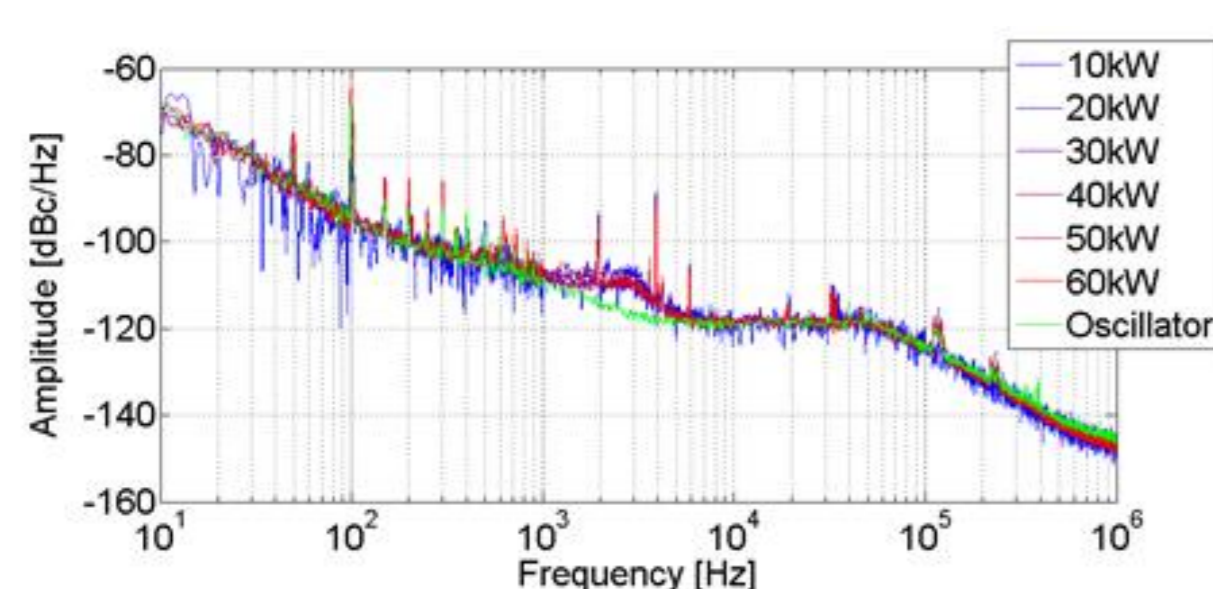
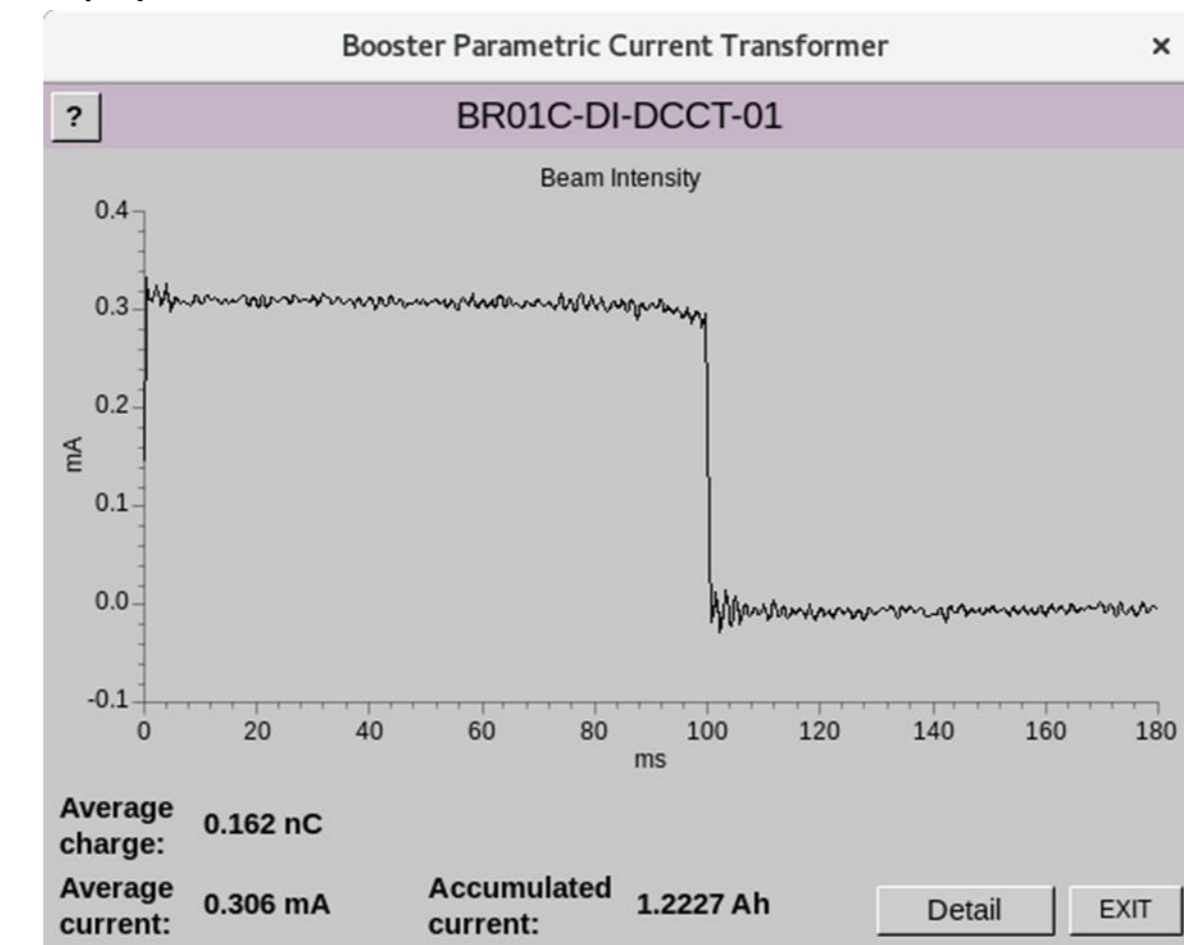


Figure 2: Measured Phase Noise



(a) RF Waveform in Cell 2 and Cell 4.



(b) Accumulated Beam in Booster.

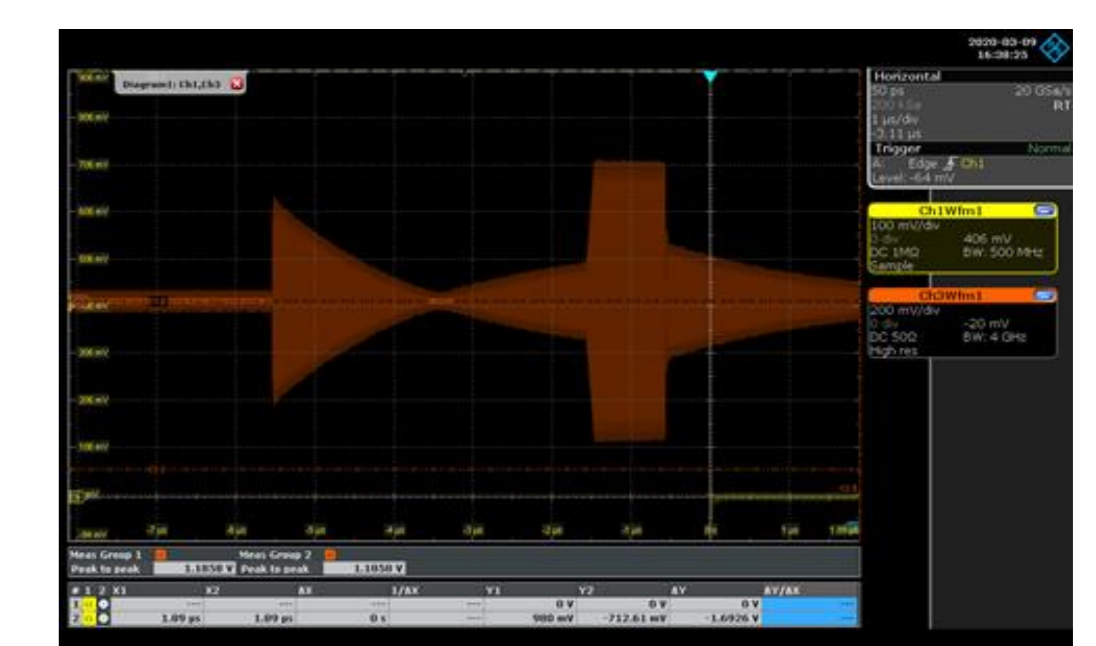
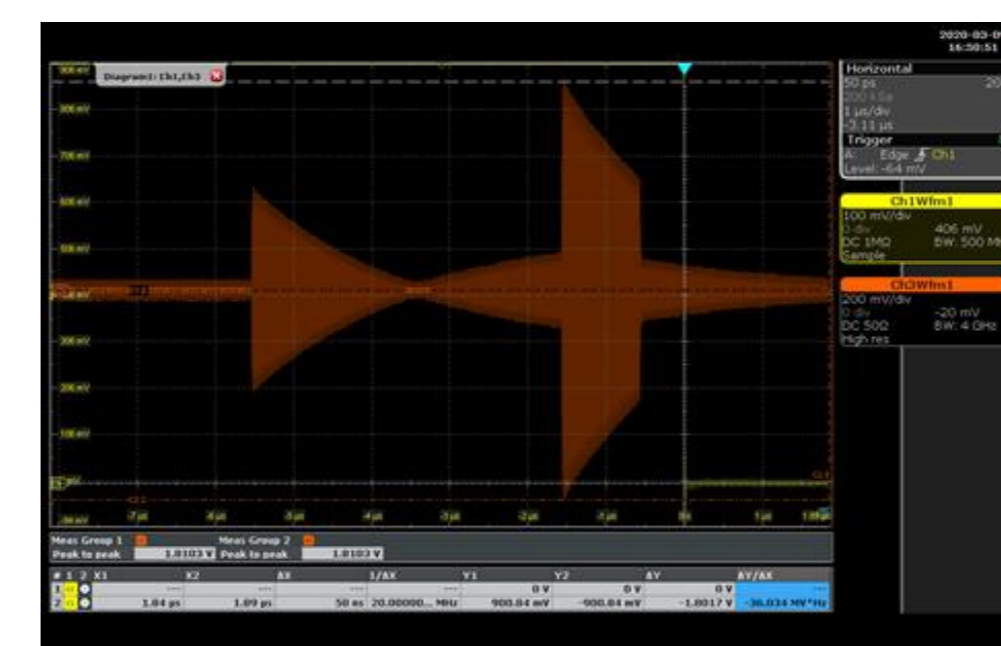
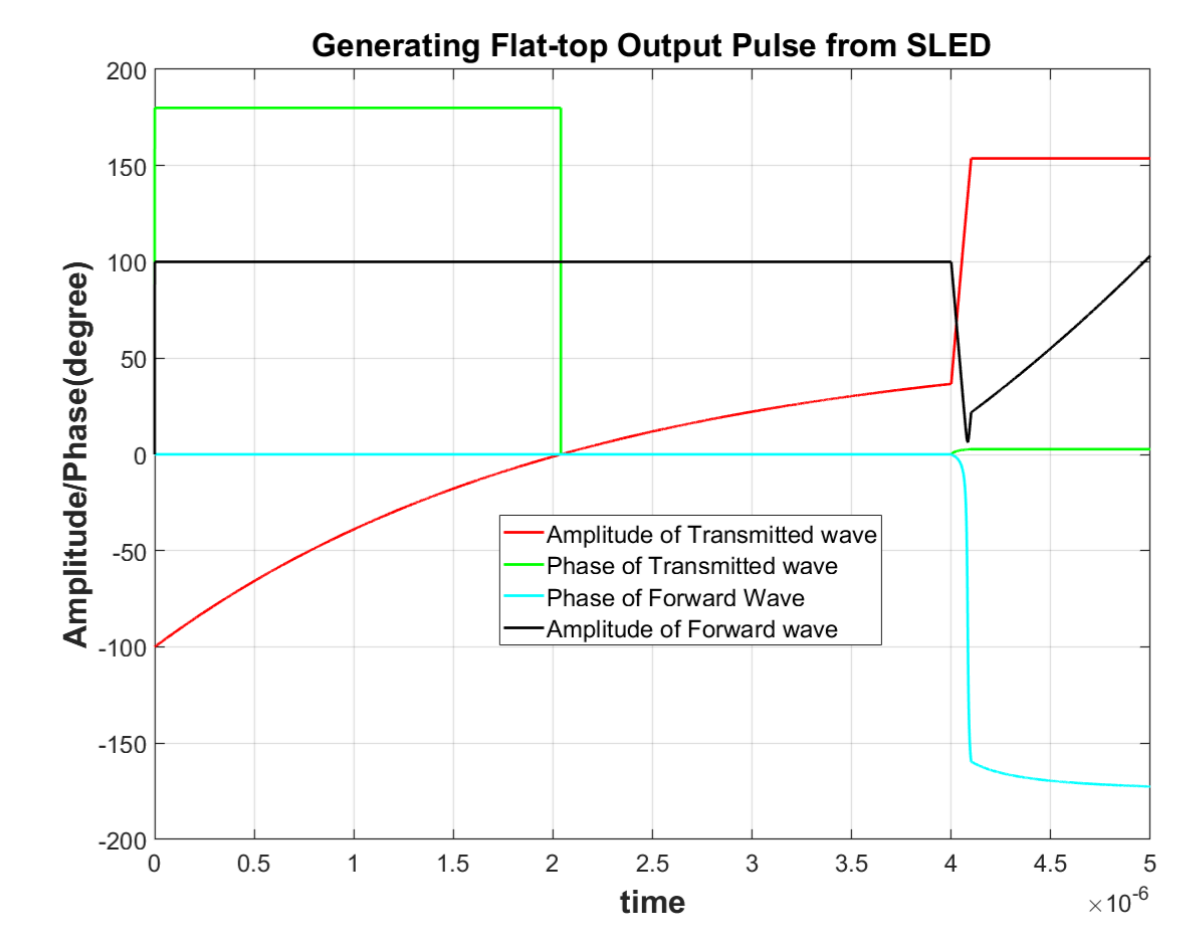
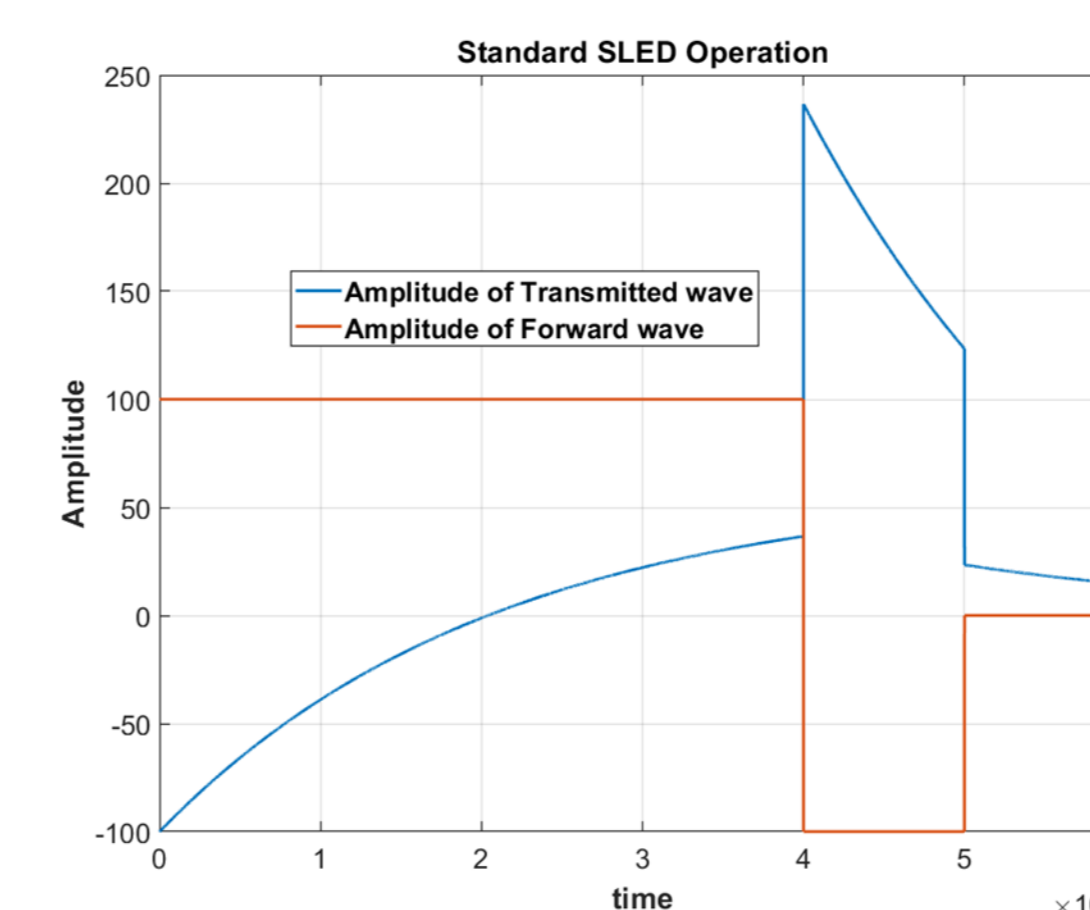
Figure 3: DLLRF for Second Booster Cavity.

## SLED Operation Requirement

Flat-top output pulse is required for the acceleration of long bunch trains. I and Q components of SLED input pulse should follow the equations below.

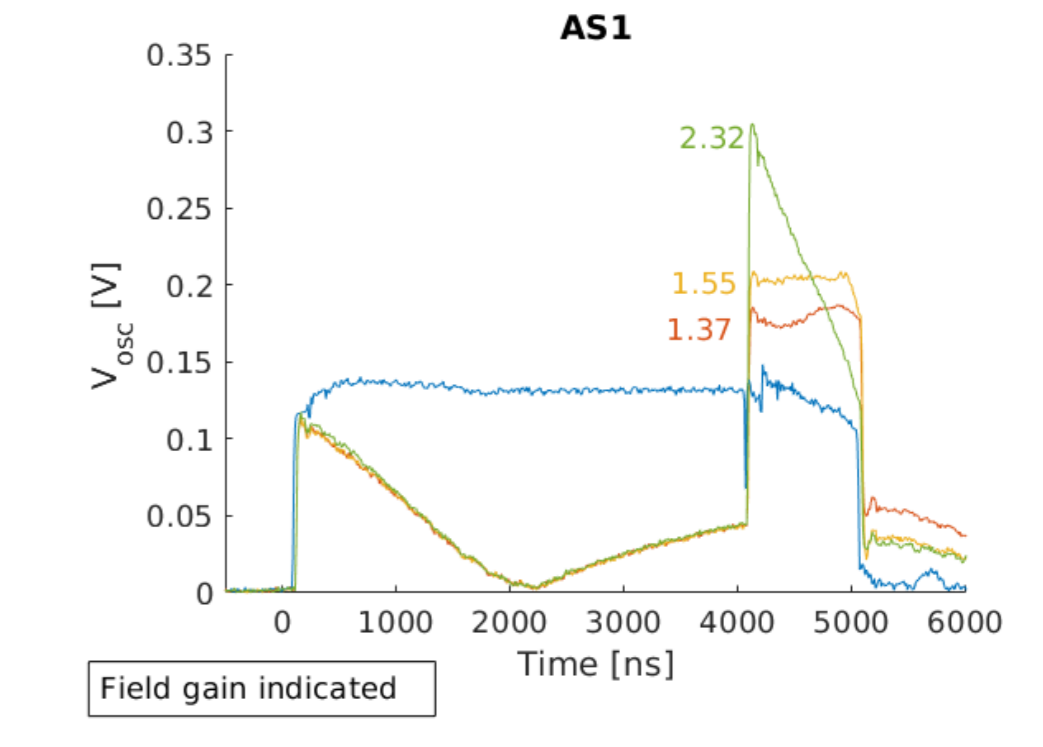
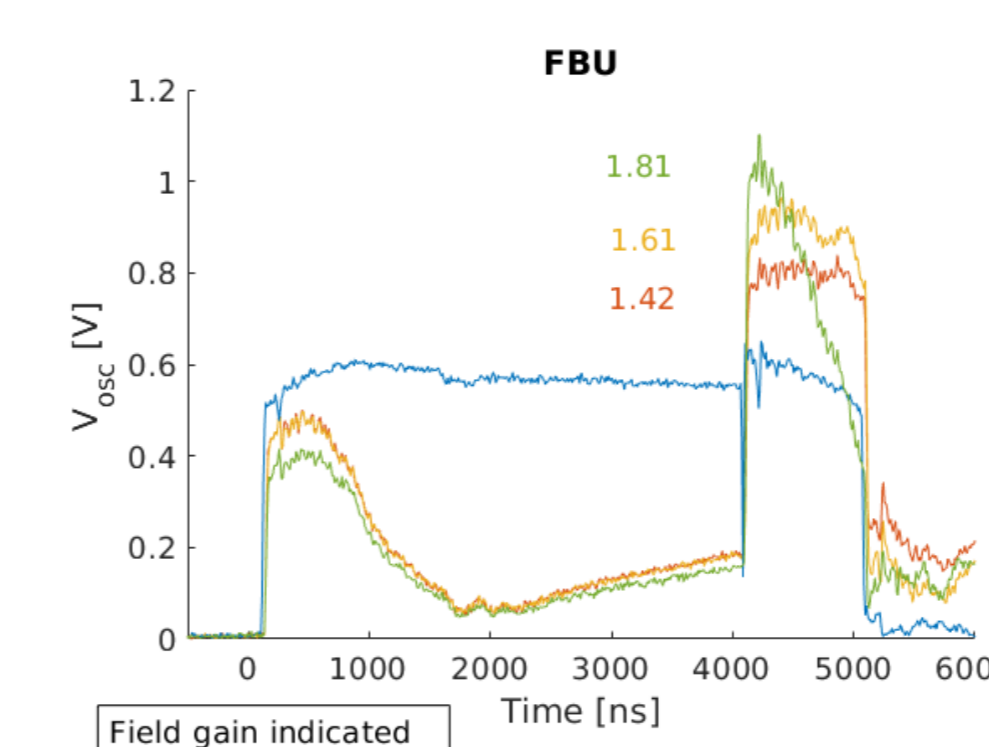
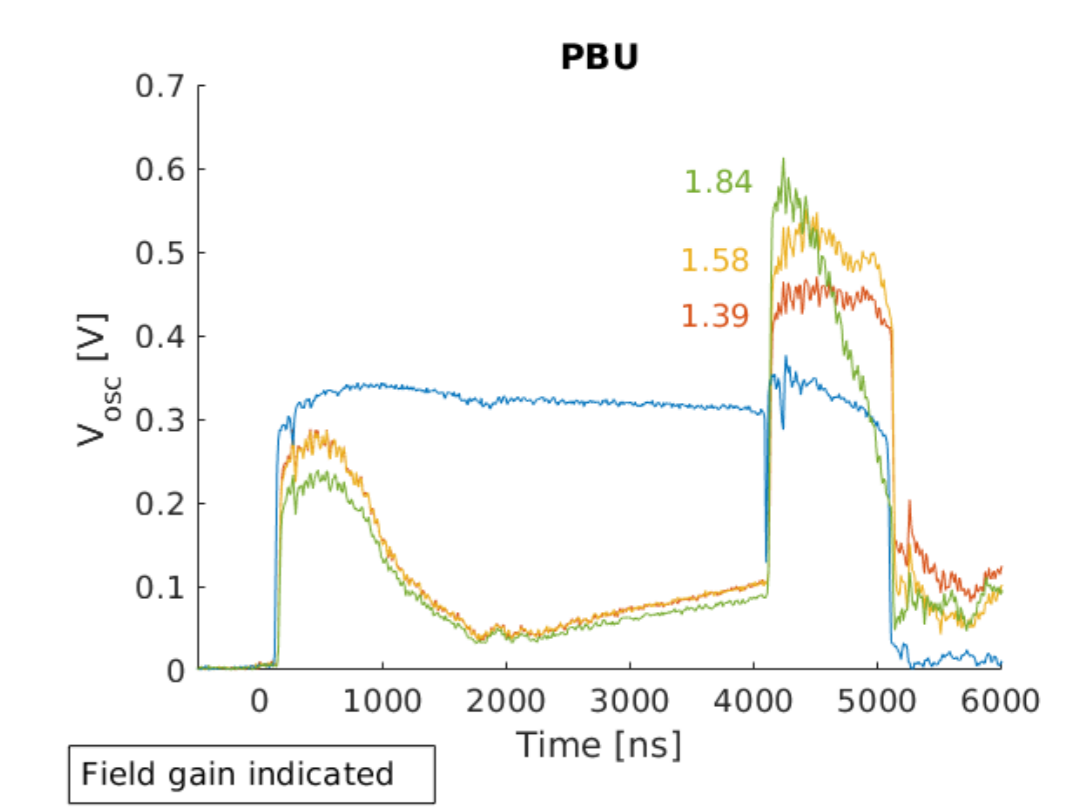
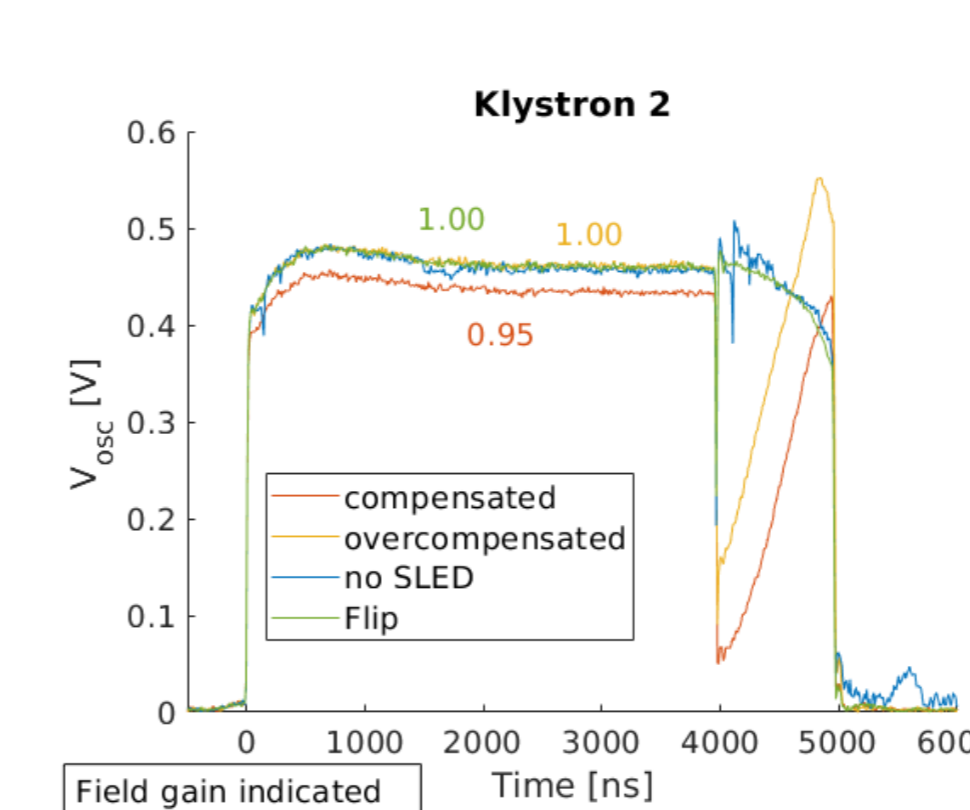
$$F_x = \frac{R_x}{\alpha-1} + \alpha \left( 1 - e^{-\frac{t1}{Tc}} - \frac{R_x}{\alpha-1} \right) e^{-\frac{(\alpha-1)(t-t1)}{Tc}} \quad F_y = \frac{R_y}{\alpha-1} - \frac{\alpha R_y}{\alpha-1} e^{-\frac{(\alpha-1)(t-t1)}{Tc}}$$

Three working modes were implemented in the firmware, namely standard mode, waveform and full waveform mode.



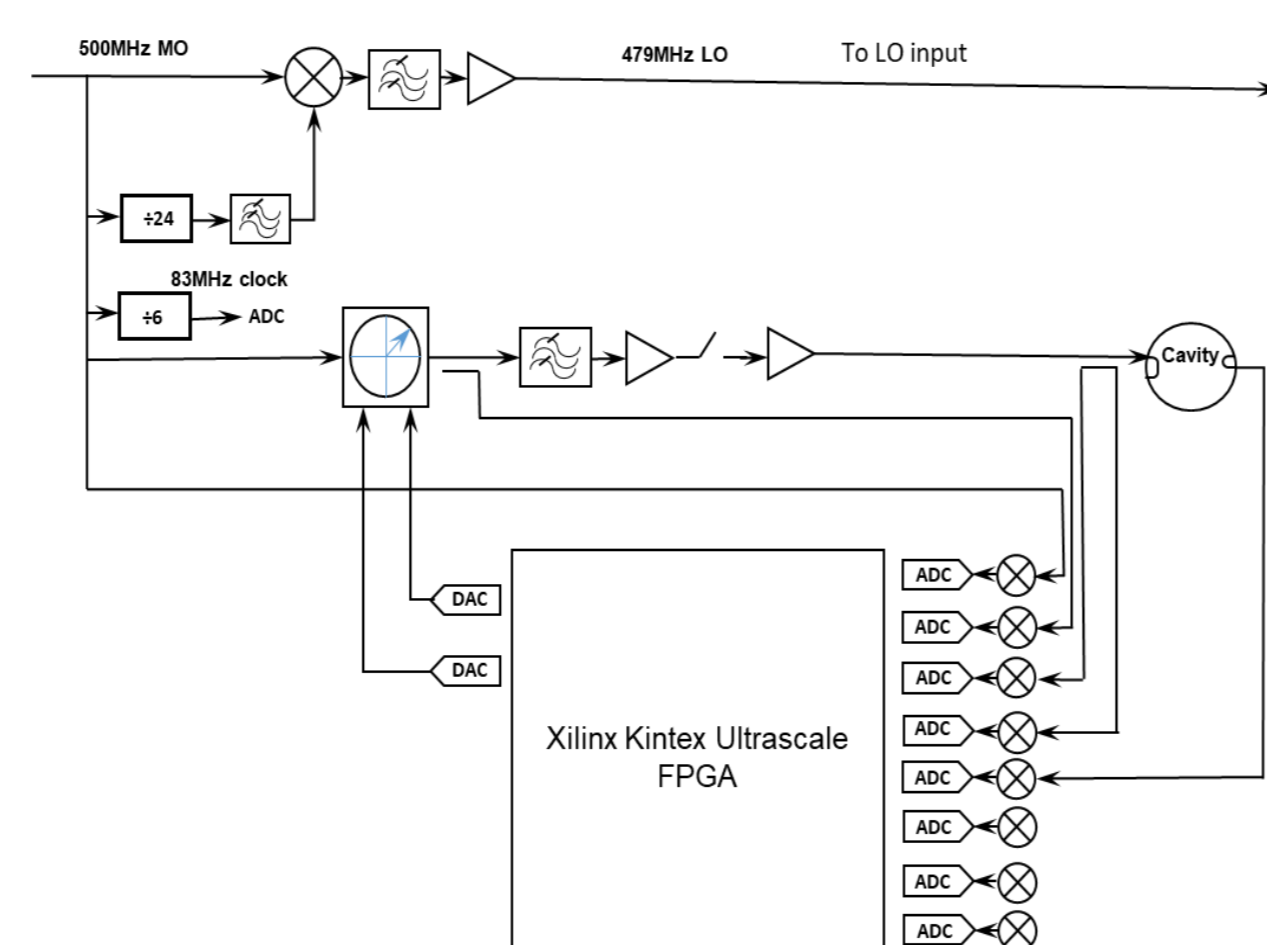
## NEW DLLRF TESTS

- Achieved better than 0.1% in amplitude and 0.03 degree in phase with all the control loops closed while controlling normal conducting RF cavity.
- Reached around 2 times power gain from the SLED with a 1 μs flat top pulse.
- Electron beam was accelerated to 65 MeV with one klystron.

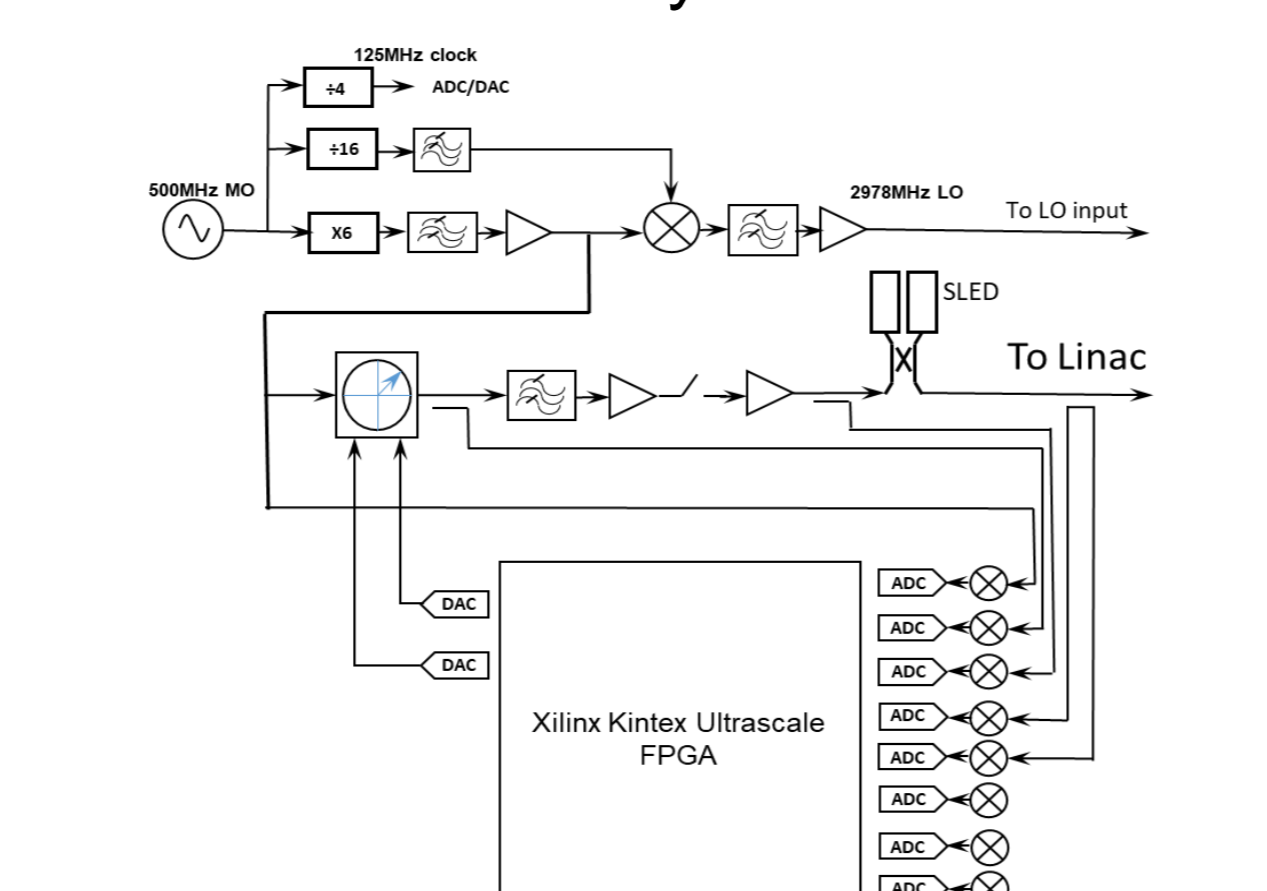


## New DLLRF

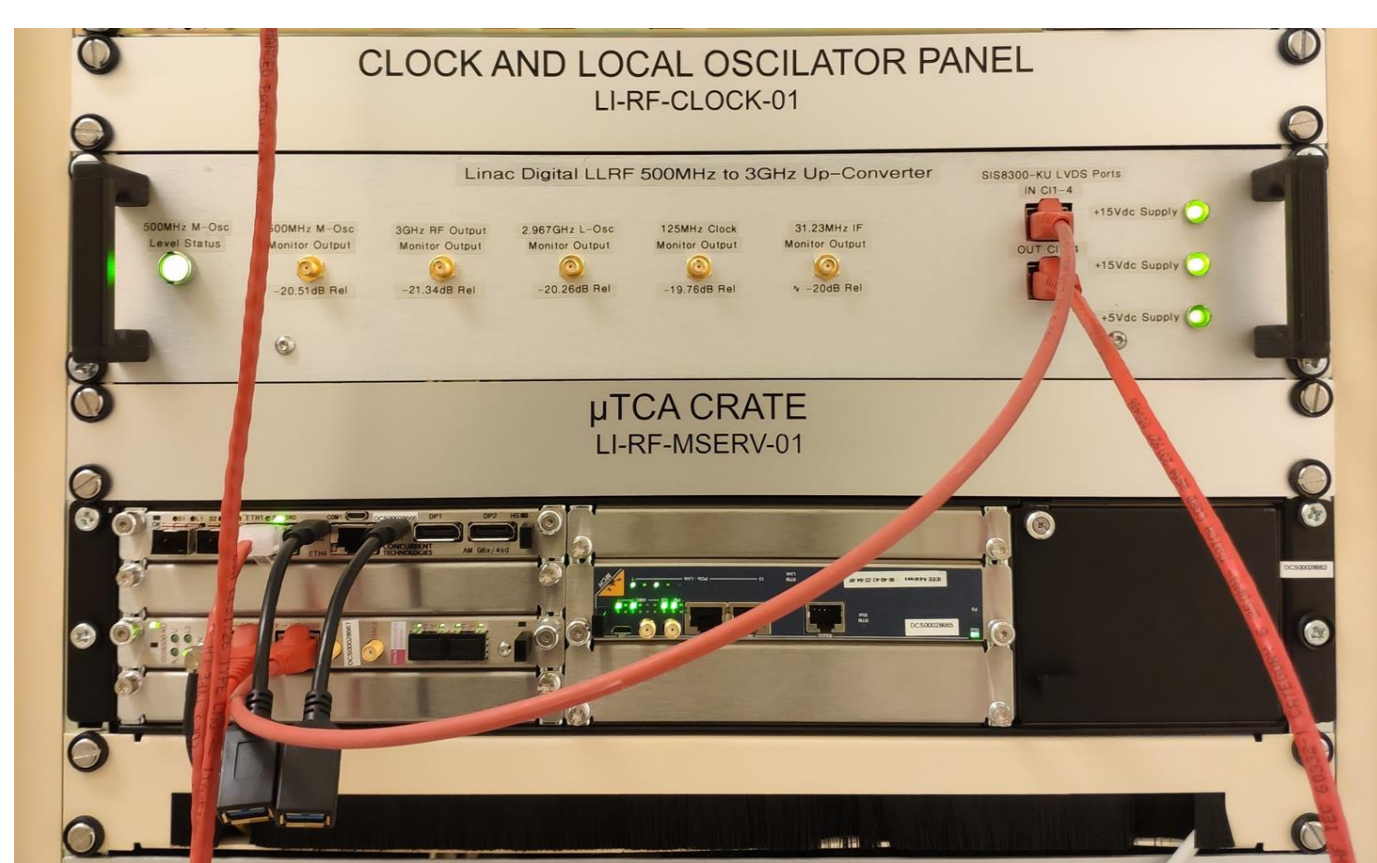
The new DLLRF consists of a 2U MTCA.4 chassis, a MCH, an AMC computer board, a Struck SIS8300-KU card, a Struck DWC8VM1 RTM with supporting clock/local oscillator (LO)/reference generation RF circuits.



500MHz DLLRF System Architecture



3GHz DLLRF System Architecture



## References

- [1] Pengda Gu, C. Christou et al., "Digital Low Level RF Systems for Diamond Light Source", in Proc. 8th Int. Particle Accelerator Conf. (IPAC '17), Copenhagen, Denmark, May 2017, pp. 4089-4091.
- [2] C. Christou, P. Gu and A. Tropp, "Programmable SLED system for single bunch and multibunch linac operation", in 31st Linear Accelerator Conference, Liverpool, UK, August 2022
- [3] Benjamin Woolley, Igor Syratcev et al, "Control and performance improvements of a pulse compressor in use for testing accelerating structures at high power", in PHYSICAL RE-VIEW ACCELERATORS AND BEAMS 20, 101001 (2017).