SPS bunch-by-bunch Phase Measurement with µTCA AFCZ & 5 Gsps FMC

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Abstract

In the Super Proton Synchrotron (SPS) during multi batch injection, we must distinguish between bunches that have been circulating in the machine, and newly injected bunches. This required a new Low Level RF (LLRF) module to measure phase of the individual bunches that are circulating in the machine. Individual bunch measurement is also needed to properly operate two phase loops during ion slip stacking.
To facilitate this, an FMC ADC mezzanine card was chosen with a sampling rate of up to 6.4 GSPS. This was paired with the AFCZ µTCA carrier board on which the signal processing of the data would be carried out. The design of the FPGA firmware presented some interesting challenges as the signal processing algorithms must process many samples in parallel due to the high throughput of data. In this case the ADC sampling clock is twenty times faster than the FPGA processing clock.
The hardware and processing architecture will be presented with details of the algorithms and how they cope with the high data throughput associated with using an ADC with a multi GSPS sampling rate.

Hardware Setup

The Beam Phase module has been designed on the uTCA platform. The beam phase module is based on a AFCZ mezzanine carrier with a Xilinx Zynq Ultrasacle+ FPGA and the Vadatech FMC217 mezzanine card. The FMC217 ADC FMC has sample rates of up to 6.2 Gsps. For this application we are using a sampling rate of 5Gsps for easier synchronisation with the 250 MHz FPGA processing clock.

Figure 1 – Beam Phase Module Hardware

Data Stream Slicing Into Successive SPS Buckets

The 5 Gsps data steam from the FMC217 mezzanine card is received continuously by the FPGA in batches of 20 parallel ADC samples at a rate of 250MHz. It is therefore necessary to slice the data into successive buckets and align the data such that the first sample of each bucket can be aligned with the first input sample of the Fourier transform. To find the bucket start we must find the point at which the RF phase crosses zero with a granularity of 200ps (5 Gsps) but the RF phase is only updated from the numerically controlled oscillator (NCO) at a rate of 125MHz. We therefore need to interpolate 40 RF phase samples in between phase updates from the NCO. For interpolation of the RF phase we can use the formula;

$$\varphi_n^{RF} \text{ (in radian)} = \frac{2\pi}{2^{49}}\left[4620\,\Phi_0^{H1,NCO} + n\,231\,FTW\right]\text{(in digits)}$$

Where n is the time index at 5 Gsps counted from the last NCO output at 125MHz.

As the phase is represented as unsigned with 2π as full scale, a bucket start (or end) corresponds to a transition from a large value to a small value and can easily be detected as a change in the MSB from 1 to 0. The ADC (FMC) provides 20 data samples at 250 MHz rate, while the NCO H1 phase and FTW are available at 125 MHz only. On each 250 MHz cycle we compute (in parallel) the 21 RF phases and FTW. , using the last available NCO H1

$$\Phi_{-1}^{RF} = 4620\,\Phi_0^{H1,NCO} - 231\,FTW$$
$$\Phi_0^{RF} = 4620\,\Phi_0^{H1,NCO}$$
$$\Phi_1^{RF} = 4620\,\Phi_0^{H1,NCO} + 231\,FTW$$
$$\Phi_2^{RF} = 4620\,\Phi_0^{H1,NCO} + 2\,231\,FTW$$
$$\ldots$$
$$\varphi_{19}^{RF} = \varphi_0^{H1,NCO} + 19\,231\,FTW$$

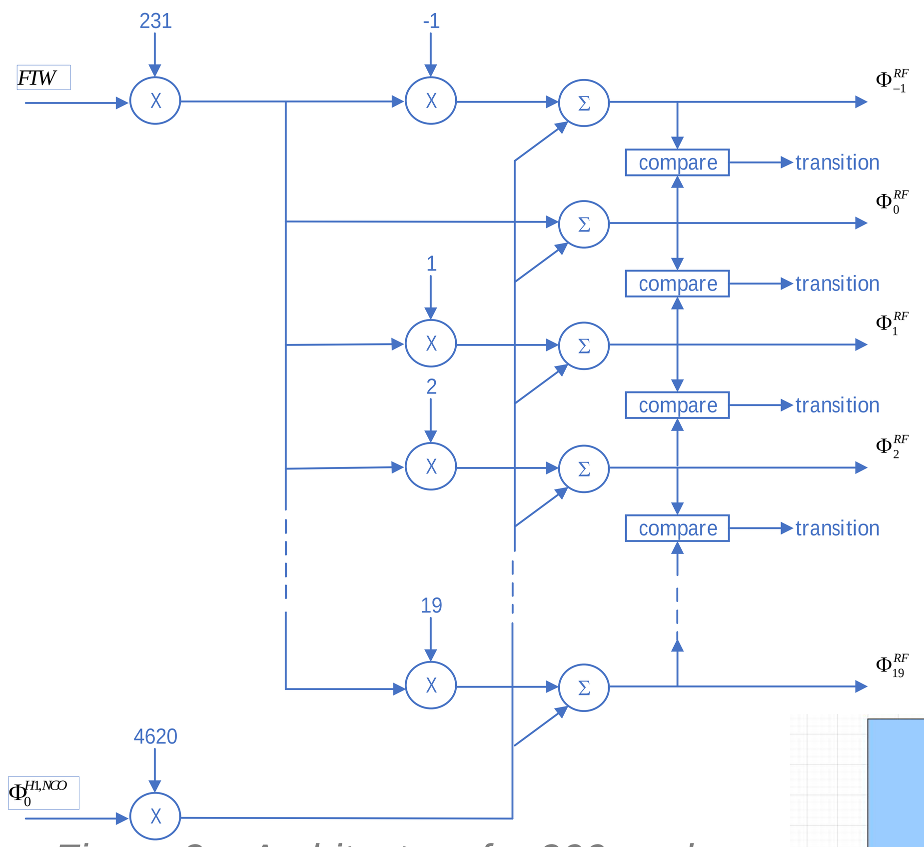

Figure 2 – Architecture for 200ps phase interpolation

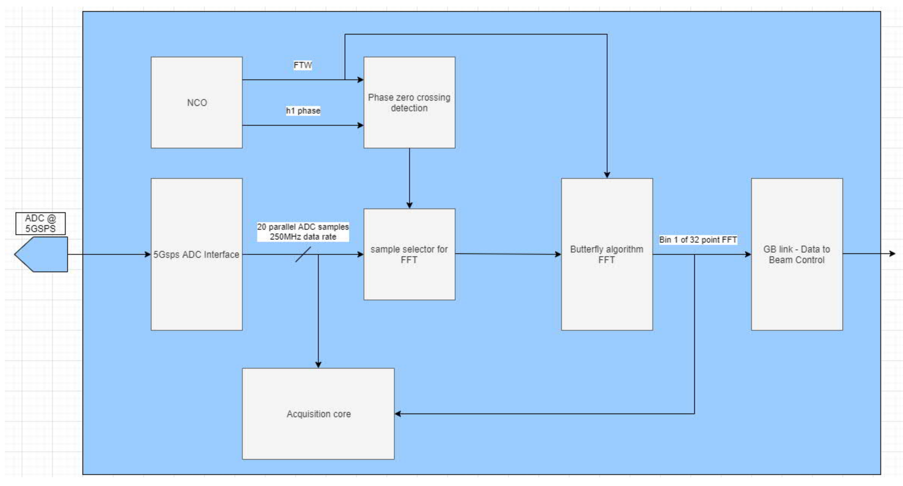

Figure 3 – Beam Phase Signal Processing Architecture

Short Time Fourier Transform

We start with the data stream $\{x_n\}$ at 5 Gsps sampled from a Wideband longitudinal PU. In the SPS we can consider an RF frequency from 199.9 to 200.4 MHz. With a sampling frequency of 5Gsps, we therefore have maximum of 26 samples in any given bucket. The RF component of the beam current from that bucket is calculated from the Short Time Fourier Transform;

$$X = \sum_{n=bucketStart}^{bucketStart+N-1} x_n e^{-j\varphi_n^{RF}}$$

Successive samples are padded with zeros such that we have N=32 samples to send to the Fourier transform processing block.

We can re-write the STFT as;

$$X = \sum_{n=bucketStart}^{bucketStart+N-1} x_n e^{-j\varphi_n^{RF}} = e^{-j\varphi_{bucketStart}^{RF}} \sum_{n=0}^{N-1} x_{bucketStart+n} e^{-j2\pi n\Omega_{bucketStart\ div\ 40}^{RF,NCO}}$$

With

$$W = e^{-j2\pi\Omega_0^{RF,NCO}}$$

The processing of this equation can be efficiently implemented using a variant of the butterfly computation (FFT) with input samples re-arranged in bit-reversed order

We can use a Flow-Graph to represent the processing. All intermediate data are complex values. Figure 4 shows the building block. The nodes (dots) represent signals (registers). Processing goes from left to right. If a branch bears a label, it means multiplication by that value. Two branches merging into a node mean addition. The basic block shown on Figure 4 represents a complex Multiply and Add (MAD)

$$X = G + W\,H$$

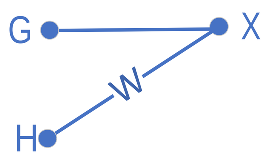

Figure 4 – Multiply add element as flow graph element

Now refer to figure 5. On the left we have the data $\{x_n\}$: x_0 is the first data sample after a detected bucket start. The data record extends to the end of the bucket and is then padded with zeros to 32 values. These data sampled are arranged in bit-reversed order. On the left we also input the phase and frequency given by the RF NCO at the time of the first data sample x_0. The processing contains six successive stages. The RF NCO phase and frequency must also be pipelined so that data $\{x_n\}$and NCO remain synchronised. With the parallel processing shown on Figure 5 we can easily process the 26 data acquired at 5 Gsps at the 250 MHz FPGA rate, allowing for one measurement per bucket.

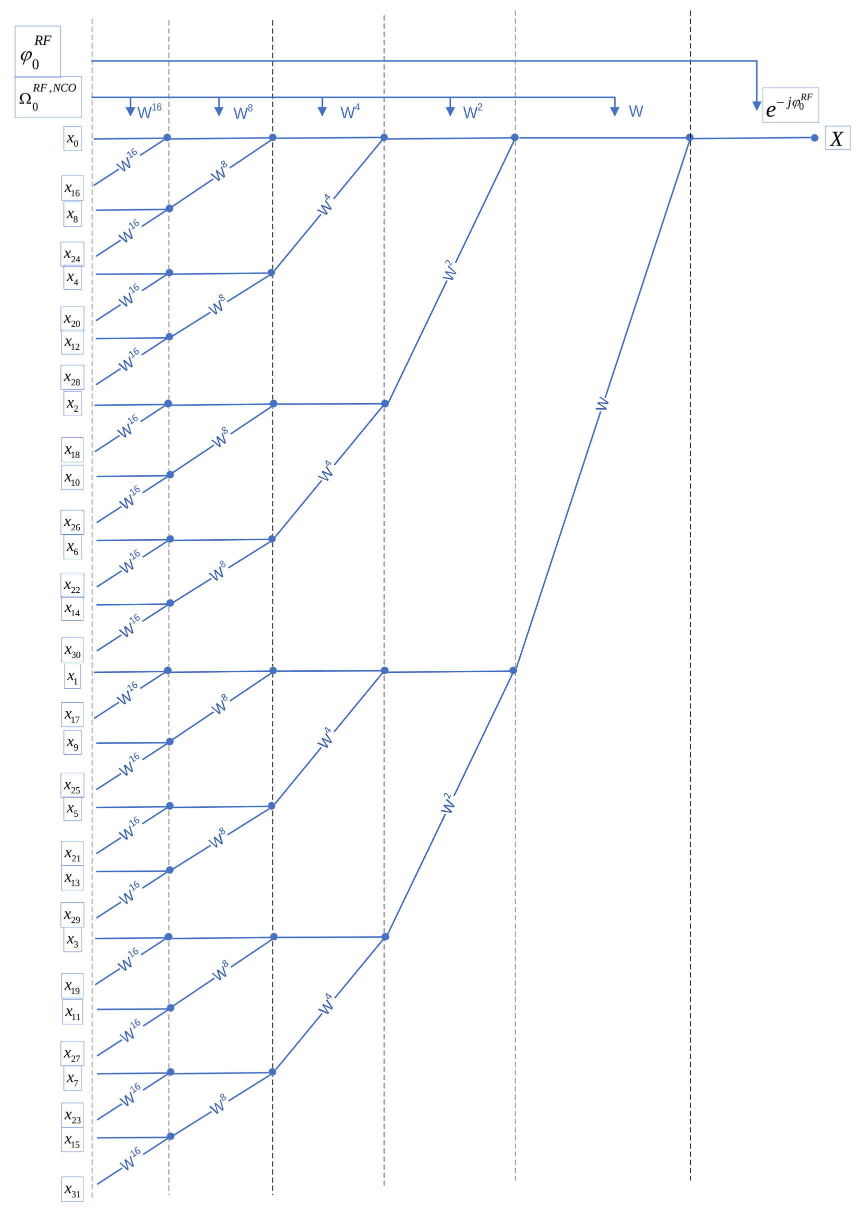

Figure 5 – Implementation of the STFT

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