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SPS bunch-by-bunch phase measurement with μ TCA AFCZ FMC

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In the Super Proton Synchrotron (SPS) during multi batch injection, we must distinguish between bunches that have been circulating in the machine, and newly injected bunches. This required a new Low Level RF (LLRF) module to measure phase of the individual bunches that are circulating in the machine. Individual bunch measurement is also needed to properly operate two phase loops during ion slip stacking.

To facilitate this, an FMC ADC mezzanine card was chosen with a sampling rate of up to 6.4 GSPS. This was paired with the AFCZ μ TCA carrier board on which the signal processing of the data would be carried out. The design of the FPGA firmware presented some interesting challenges as the signal processing algorithms must process many samples in parallel due to the high throughput of data. In this case the ADC sampling clock is twenty times faster than the FPGA processing clock.

The hardware and processing architecture will be presented with details of the algorithms and how they cope with the high data throughput associated with using an ADC with a multi GSPS sampling rate.

Primary author: BORNER, Robert

Presenter: BORNER, Robert

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