LLRF for PolFEL Accelerator

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INTRODUCTION

PolFEL, the first FEL research infrastructure in Poland, will be a 4-th generation light source, based on the 200 MeV superconducting linear accelerator. It which will operate in both, pulsed wave (PW) and continuous wave (CW) modes and will generate coherent light in 3 ranges: THz, IR and VUV.

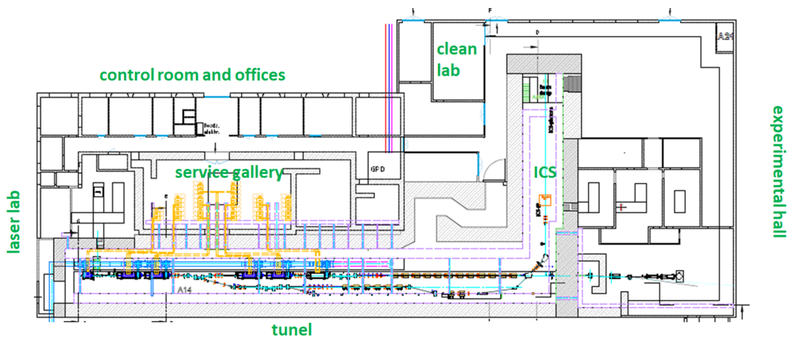

Figure 1: Layout of the PolFEL facility

ELECTRON BEAM PARAMETERS

Diagnostics system consists of button beam position monitors, Farady cups, YAG screens, coherent diffraction radiators current transformers and dark current monitor.

	Unit	Gun	VUV/e^- line	THz line
Bunch charge	pC	20-250	max 100	250
Bunch repetition rate	kHz	50	50	50
Trans. normalized 80% slice emittance	$\mu m \times rad$	0.1-0.4	< 0.6	<1
Diameter of the irradiated spot	mm	0.45-1.6	-	-
Bunch duration at the electron line exit	ps	2-10	0.1	up to 10
Beam energy at the line exit:				
cw	MeV	4	up to 154	up to 79
lp mode @ duty factor of 65%	MeV	4	up to 187	up to 79
Maximal beam current	μA	12.5	5	12.5
Beam power at dump:				
cw	W	-	770	938
lp @ duty factor of 65%	W	-	608	

Table 1: Electron beam parameters

PHOTON BEAM PARAMETERS

VUV and IR radiation will be generated in SASE process, while THz radiation will be emitted within superradiant regime by the bunches compressed below the wave length already using the linac chicanes. The sum of particular undulators wavelength ranges extends from 600 μm down to 65 nm. The shortest will be emitted as the 3^{rd} harmonic. This limited with the saturation length or undulator chain length rather than available electron energy available.

	Unit	VUV (1^{st} Harm.)	VUV (3^{rd} Harm.)	THz line
Min wave length:				
cw	nm	210	70	(0.5 - 6) $\times 10^5$
lp @ DF=40%	nm	165	55	(0.5-6 THz)
Energy per pulse, E_γ:				
cw	μJ	11.0	0.24	30
lp @ DF=40%	μJ	19.6	0.03	30
Radiation power:				
cw	W	3.75	0.01	1.5
lp @ DF=40%	W	0.40	0.0006	1.5
Pulse duration	ps	0.35	0.35	30
$\Delta E_\gamma / E_\gamma$	-	0.008	0.008	0.05

Table 2: Electron beam parameters

FPGA PROJECT

LLRF system to read field parameters and drive the vector modulator, proper functionality has been implemented in the FPGA using Xilinx Vivado Design Suite (fig 2). Dedicatd IP Cores has been implemented for ADC511 FMC board, LLRF Controller and DAC & vector modulator FMC board. The LLRF Controller have implemented such functionalities as IQ detection, ADC & DAC offset calibration, input and output matrix rotation and proportional and integral gain.

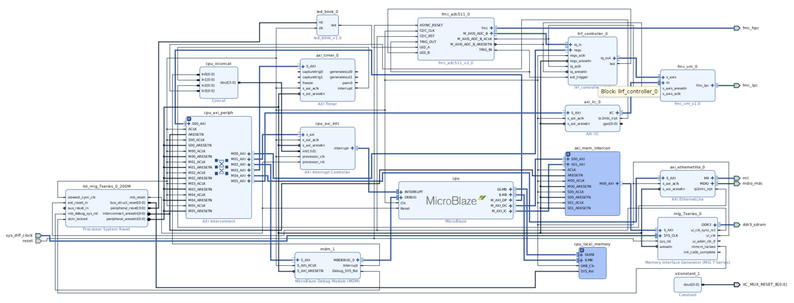

Figure 2: FPGA design in Vivado Design Suite

VECTOR MODULATOR FMC CARD

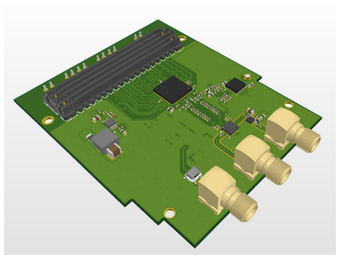

Figure 3: Vector modulator FMC board

Reading the field parameters was big step forward, but to close the feedback loop, vector modulator was needed. For the purpose of the LLRF control, the FMC board with dual-channel DAC and vector-modulator has been designed, and manufactured.

HIGH POWER RF SYSTEM OVERVIEW

The aim of the RF system is to deliver power to accelerating modules which is needed to accelerate the electron beam. The accelerating modules of the PolFEL accelerator will be made of TESLA-type, 9-cell RF Structures. Each criomodule will have two such RF structures, but each structure will be driven and controlled individually. RF power from solid state amplifiers to the criomodules will be delivered using WR650 waveguides. Solid state amplifiers will be placed in the hall next to the accelerator tunnel. Because the construction of PolFEL will utilize existing buildings, the design of the waveguides distribution system is not straightforward and requires significant effort.

One of the features that helps in the wageguide design is single cavity regulation mode. Because of this, there is no need for splitting the RF power withing the waveguide distribution system, and each waveguide will deliver RF power directly from the amplifier to the RF structure. In such configuration, circulators and loads does not have to be placed close to the criomodules and can be placed next to the RF amplifiers, out of radiation impact area.
The RF power in PolFEL accelerator will be generated by solid state amplifiers (SSA), because PolFEL will operate in continuous mode, a dedicated RF power source is needed. Such RF amplifier for PolFEL will be designed and delivered by the **Kubara Lamina S.A.** company.
By the time of this event, the prototype of the SSA amplifier was under development (Fig. 4).

Figure 4: Prototype of the solid state amplifier for PolFEL under development

The requirements for the RF amplifier are following:

Parameter	Value
Lower frequency range (-3dB)	$\leq$ 1270 MHz
Upper frequency range (-3dB)	$\geq$ 1310 MHz
Output power in pulsed mode	$\geq$ 7kW
Maximal pulse duration	$\geq$ 1 ms
Output power in continuous mode	$\geq$ 5kW
Maximal power of input signal	$\geq$ 10 dBm
Amplifier gain	$\geq$ 60 dB
Max. required power supply level	$\leq$ 20 kW
Operational temperature range	5 ℃ - 40 ℃

Table 3: SSA Key Parameters

LOW-LEVEL RF SYSTEM

High speed and high bandwidth ADCs makes possible to sample directly the RF signal of the 1.3 GHz frequency. Well known and also evaluated for this purpose is Texas Instruments ADS5474, which input bandwidth covers range up to 1.4 GHz. Possibility of direct RF sampling allows to significantly simplify the LLRF hardware.
The components of the PolFEL LLRF system are similar to the ones used at X-FEL[**?**] because of the same fundamental frequency 1.3 GHz, but the layout of the system is more like the one used at ESS[**?**], because ESS operates also in single cavity regulation mode.

LLRF system scheme in the Figure 5 show the configuration used at ESS. Configuration used at ESS for controlling single cavity occupies 3 slots in the MTCA chassis, and results in total number of 6 devices (3xAMC + 3xRTM) for single cavity (Fig. 5). One slot is occupied by the main LLRF Controller, which uses both boards: AMC with FPGA and data converters, and RTM with the downconverters and vector modulator. Other two slots are occupied by the piezo controller, and LO clock signal generator.

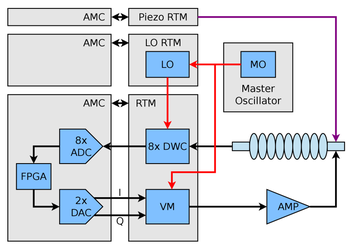

Figure 5: ESS LLRF System architecture

The concept of the PolFEL LLRF controller (Fig. 6) is much simpler, for single cavity control single MTCA chassis slot is occupied. From the rear side of the slot the Piezo RTM will be placed, and from the front side an AMC FMC Carrier will be used. All LLRF specific infrastructure will be placed on the custom dual FMC board. With respect to the amount of connected I/O pins in the FMC connectors, any MTCA.4 FMC carrier can be used. This configuration does not require down-converters, so separate LO generation device is not required as well.

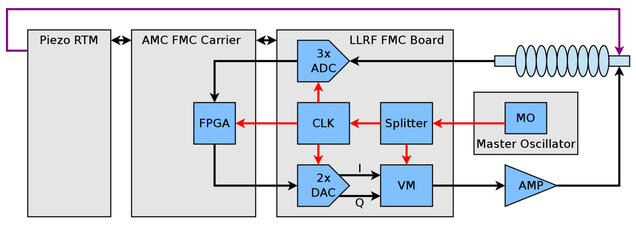

Figure 6: PolFEL LLRF System architecture

The function of the LO generation is performed by proper circuitry integrated in the FMC board along with the ADCs and DACs. The ADC sampling clock is generated directly from the 1.3 RF signal, and the distance from RF input to the ADC or vector modulator is less than 10 cm. All clock distribution for a single LLRF system will be made on the single PCB.

INITIAL TESTS WITH THE COPPER CAVITY

To eavluate described concept, a proper test setup has been assembled. To make tests as much simillar to the final case, a 1.3 GHz, 3-cell, copper cavity has been used.

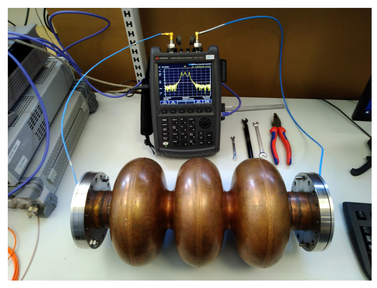

Figure 7: Cavity characterized using VNA

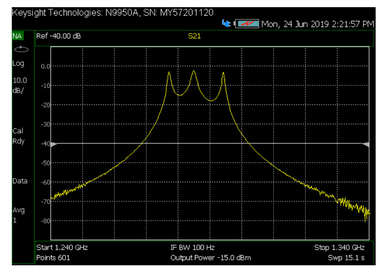

Figure 8: Cavity amplitude response

As a first step, the cavity has been measured and using Vector-Network Analyzer (fig. 7). It was also the time to tune the couplers. When the cavity response was proper 8
For the next step, the field in the cavity has been excited using the RF generator on one side, while the signal from the other coupler was attached to fast ADC on the Curtiss-Wright ADC511 FMC mezzanine attach to Xilinx KC705 evaluation board. Using digital I/Q detection, it was possible in the FPGA to read the amplitude and phase of the cavity field.
Having all components available, finally the complete setup has been assembled (fig. 9).
Signal from the RF generator has been splitted and delivered to vector modulator as source RF signal to be modulated, and to clock divider, which generates frequencies suitable for ADCs and DACs. Clock divider can additionally provide clock signal to the FPGA device using FMC_M2C signals, but this is not necessary because ADCs and DACs provides clock synchronized with data.

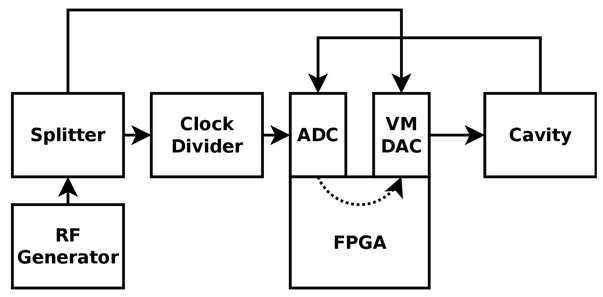

Figure 9: The scheme of the test setup

RESULTS

Finally, using presented test setup, feedback loop on the copper cavity has been closed. Images below shows the single pulse of the input and output of the controller. Figure 10 shows amplitude and phase the output signal from the controller on top of the feed-forward value (the ideal drive signal). The difference between feed-forward and output signal is caused by working closed loop feedback.

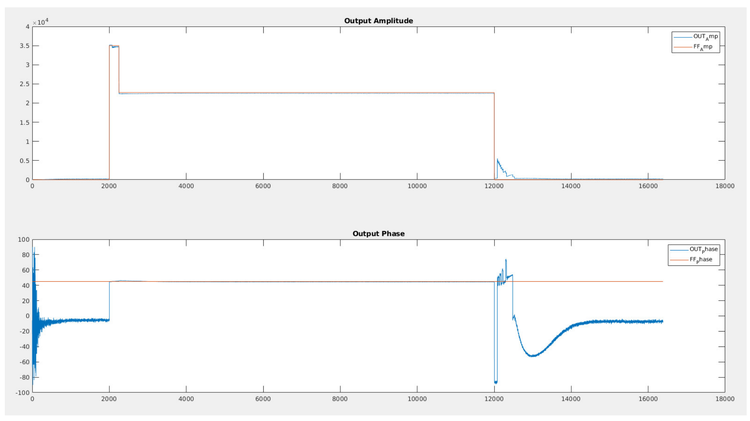

Figure 10: Controller output

Figure 11 shows simialr image like fig. 10, but it shows the amplitude and phase of the controller input signal on top of the set-point value (expected cavity field).

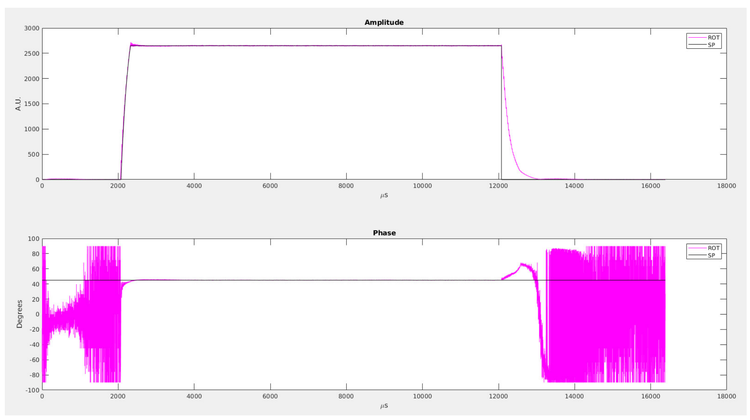

Figure 11: Controller input

To show better the input signal on top of the set-point figure **??** shows zoomed amplitude and phase regions of the RF pulse.

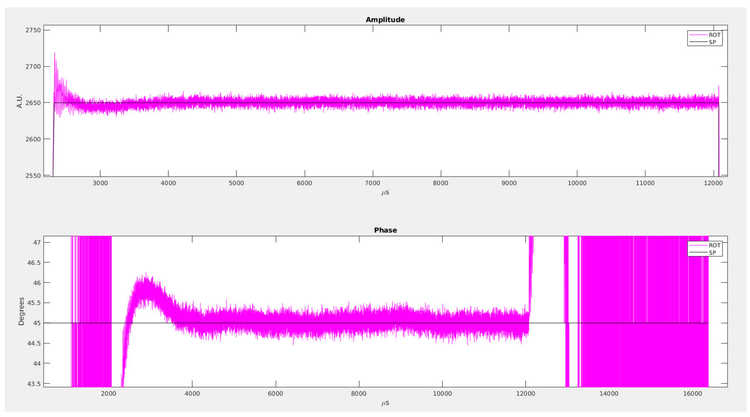

Figure 12: Controller input

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