Status of the LLRF system for ESS related in-kind project by PEG

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ESS Principles

European **S**pallation **S**ource – **E**uropean **R**esearch **I**nfrastructure **C**onsortium

Parameter	Units	Value
Energy	GeV	2.0
Current	mA	62.5
Pulse length	ms	2.86
Pulse repetition frequency	Hz	14
Average power	MW	5
Power during pulse	MW	125

Target
D02 Target Building

Experimental Halls
D01 Experimental Hall 1
D03 Experimental Hall 2
D04 Labs, Hall 2
D05 Substation
D06 Substation
D07 Labs, Hall 2
D08 Labs, Hall 2

E01 Experimental Hall 3
E02 Beam Line Gallery
E03 Labs, Hall 3
E04 Labs, Hall 3
E05 Substation

Utilities
H01 Central Utility Building
H05 Substation
H06 Substation
H09 Waste Building
H10 Sprinkler Building

Service
F03 Logistic Center
F04 Entrance Building

Campus
B01 Office Building
B02 Lab/Workshop Building

Figure 1. Layout of the ESS facility.

ESS Principles – accelerator

European **S**pallation **S**ource – **E**uropean **R**esearch **I**nfrastructure **C**onsortium

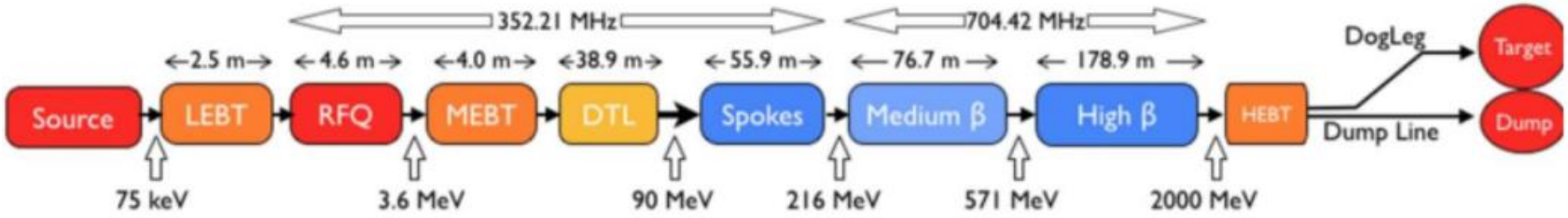


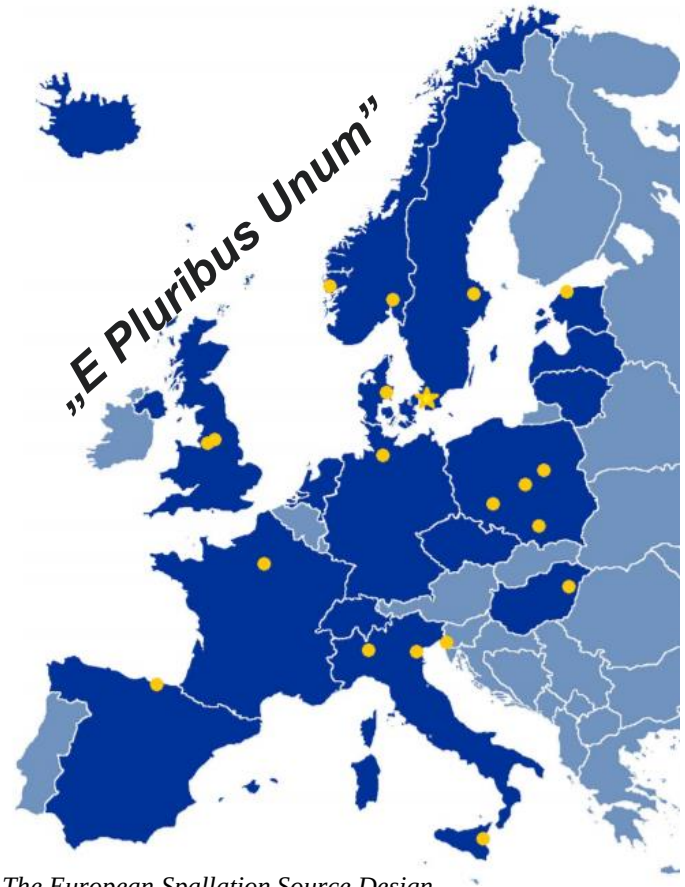
Table 19. Number of cavities, frequency and peak power level.

Linac section	Energy (MeV)	Freq. (MHz)	Number of cavities	Cavities per cryo-module	Geometric β	Temp. (K)	Max. RF power (kW)
Source	0.075	—	0	—	—	300	—
LEBT	0.075	—	0	—	—	300	—
RFQ	3.6	352.21	1	—	—	300	1600
MEBT	3.6	352.21	3	—	—	300	20
DTL	90	352.21	5	—	—	300	2200
Spoke	220	352.21	6	2	0.5 β_{opt}	2	330
Medium-β	570	704.42	36	4	0.67	2	870
High-β	2000	704.42	84	4	0.86	2	1100
HEBT	2000	—	0	—	—	300	—

The European Spallation Source Design
Roland Garoby et al 2018 Phys. Scr. 93 014001

ESS Principles – accelerator collaboration

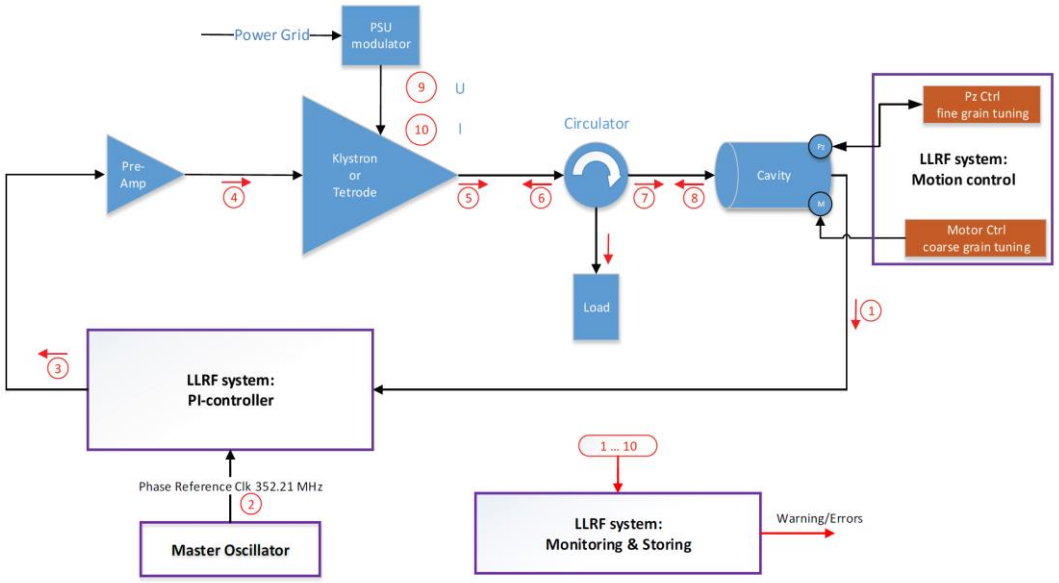
European **S**pallation **S**ource – **E**uropean **R**esearch **I**nfrastructure **C**onsortium

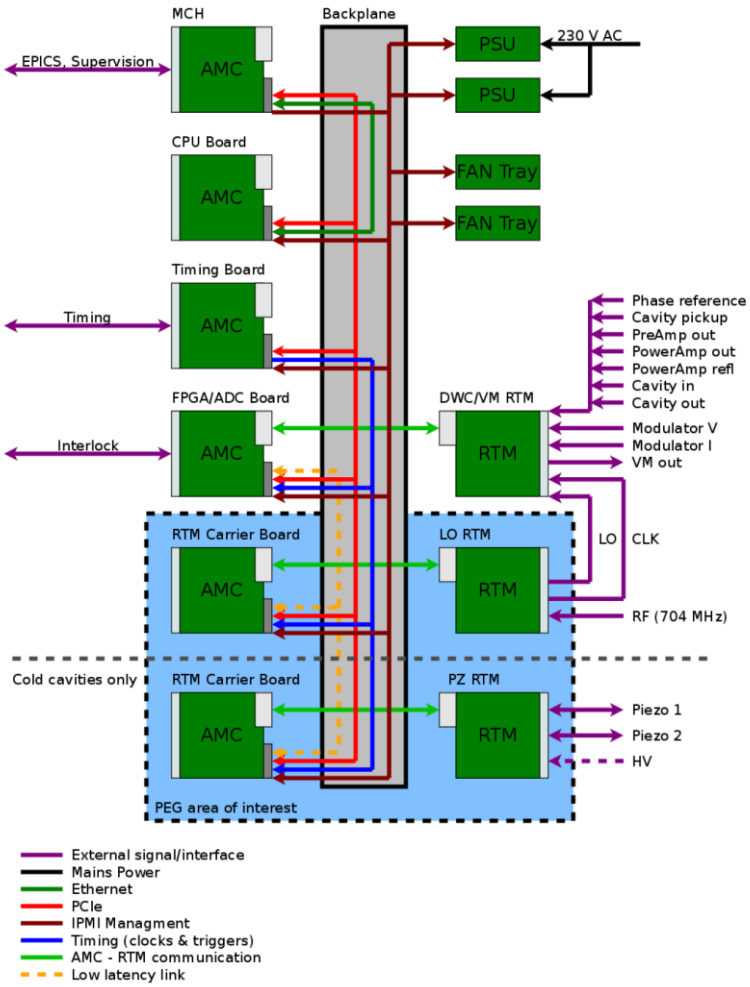


The European Spallation Source Design
Roland Garoby et al 2018 Phys. Scr. 93 014001

Institution	Main deliverables
Aarhus Univ (DK)	Rastering system
Atomki (HU)	RF local protection system
Bergen University (NO)	Seconded staff
CEA Saclay (FR)	RFQ, elliptical cavities and cryomodules, diagnostics
DESY (DE)	Diagnostics
Elettra (IT)	Spoke RF sources, magnets, power converters, diagnostics
ESS-Bilbao (ES)	MEBT, warm linac RF, diagnostics
Huddersfield Univ (UK)	RF distribution, radiation protection
IFJ PAN (PL)	Manpower for installation
INFN Catania (IT)	Ion source, LEBT
INFN Legnaro (IT)	Drift tube linac
INFN Milan (IT)	Medium-beta elliptical cavities
IPN Orsay (FR)	Spoke cavities, cryo distribution
Lodz Univ of Techn (PL)	Low-level RF
Lund Univ (SE)	Low-level RF
NCBJ (PL)	Low-level RF, gamma blockers
Oslo Univ (NO)	Diagnostics
STFC Daresbury (UK)	High-beta elliptical cavities, vacuum
Tallinn Univ of Techn (EE)	IOT modulator development
Uppsala Univ (SE)	Tests of spoke cavities and cryomodules
Warsaw Univ of Techn (PL)	Phase-reference line, low-level RF
Wroclaw Univ of Techn (PL)	Cryogenic distribution

ESS LLRF systems for elliptical resonators





*Talk ID 98: A. Svensson,et al..
ESS LLRF status and activities

Source: A. Johansson The ESS LLRF CDR

ESS PEG Polish in-kind project

Polish Electronic Group (PEG) Consortium:

- Warsaw University of Technology - WUT, Institiute of Electronic Systems - ISE
- National Center of Nuclear Science,
- Lodz University of Technology – LUT, Department of Microelectronics and Computer Science - DMCS

Funding agency: Ministry of Education and Science

Minister of Education and Science

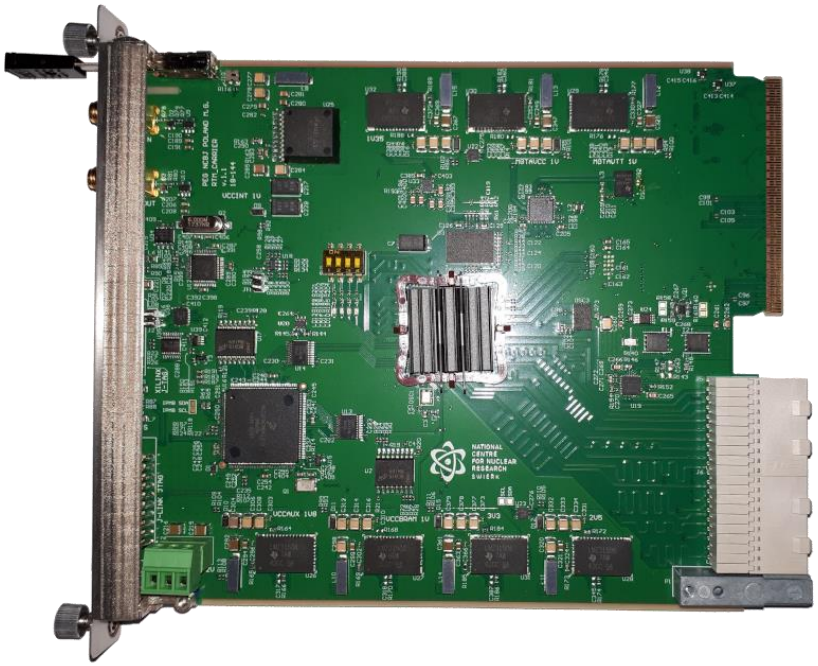
Project duration:10.2016 – 07.2023

Figure 1: High beta 704.42 MHz undressed cavity.

PEG main responsiblities

- Hardware components design, evaluation and production for M-Beta and H-Beta cavities control systems:
  - RTM Carrier board,
  - RTM Piezo Driver,
  - Local Oscillator board,
  - PSS switch,
  - Pin diode,
  - Electron pick-up,
  - RF splitbox
- Reference LLRF system integration and evaluation,
- Hardware cavity simulator design and evaluation,
- LLRF systems integration, installation in the ESS and evaluation,
- Chosen firmware components preparation.

RTM Carrier (general purpose AMC module)



- FPGA based MTCA.4 AMC module,
- supporting LO RTM and Piezo RTM,
- equipped in Artix-7 FPGA device, 1GB of DDR3 memory PCIe x2 and Low latency Links,

General functionality:

- communication with the RTM via ZONE 3,
- powering RTM devices,
- communication via PCI-Express on the backplane,
- data processing in the FPGA,
- the AMC board defined in the MTCA.4 standard.

Status

- All M-Beta required pieces produced, tested and delivered ,
- Mass production of the H-Beta batch planed for Q4 2022

RTM Piezo Driver

- provides signal for LFD and microphonics suppression,
- actuator and sensor mode of operation,
- two independent channels,
- ready for elliptical and spoke cavities operation,
- synchronization with the linac timing,
- digital diagnostic and health monitoring available,
- MTCA.4 compatibility,
- external Piezo Power Supply Module control.

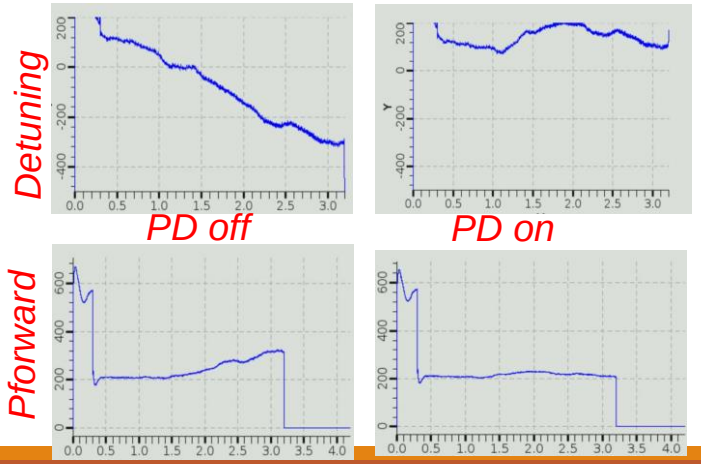
Parameters :

- output voltage: 0 to +200V (-40 to 160V - for spokes),
- controller bandwidth DC-1kHz,
- repetition rate - 14 Hz,
- Max. power - 30W,
- PowerSupply voltage -/+ 100V,
- Actuator: 1MHz, No of samples: 30k, resolution 16 bits,
- Sensor: 1MHz, No of samples: 30k, resolution 16 bits, input voltage -/+1V, impedance: 10kOhm,
- piezo capacitance (room temp.) 6.6 to 11 uF.

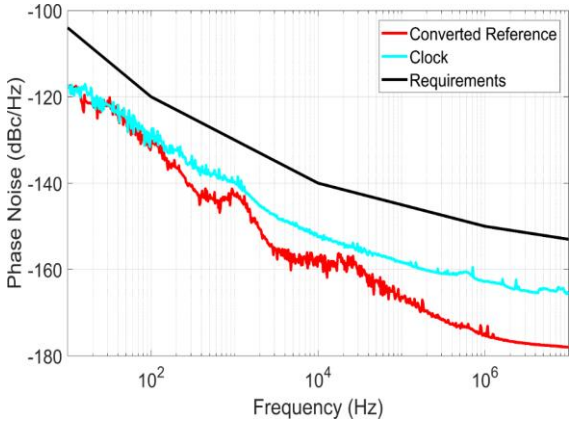
Status:

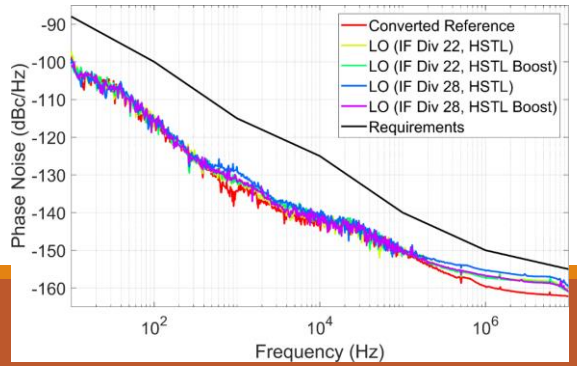
- Final prototype produced 03.2021 (installed @TS2 ESS, and local TS)
- Mass production in preparation, to be finished Q4 2022.

*Poster ID61: W. Cichalewski,et al..
The ESS cavities dedicated piezo driver evaluation status



RTM Local Oscillator module





- generates clock *Fref*/6 = 117.403 MHz
- generates LO (736.439MHz - 23/22 or 729.578MHz - 29/28)
- synchronous to 704.42MHz reference,
- clock signal achieved by a frequency divider and the LO using a frequency divider, mixer, and band-pass filter (direct analog scheme) (to follow the input phase noise in wide offset bandwidth)
- communicates with an AMC via the Zone3,
- the AMC can set the board parameters and read out the input and output powers.

Status

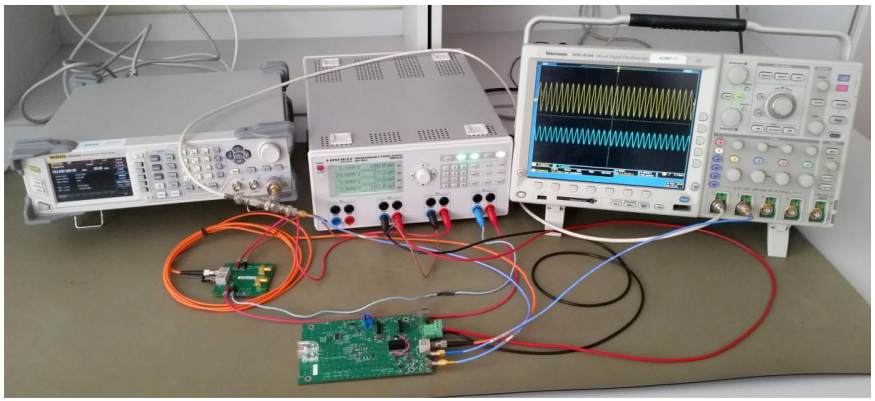
- All M-Beta required pieces produced, tested and delivered ,
- The H-Beta planed for Q4 2022

PSS switch module

- turns off the RF power going to high power if Personal Safety Systems detect an emergency,
- based on an RF relay manufactured by Radial.
- control signal from the PSS controller,
- specifed by ESS, produced and delivered by PEG (126 pieces)

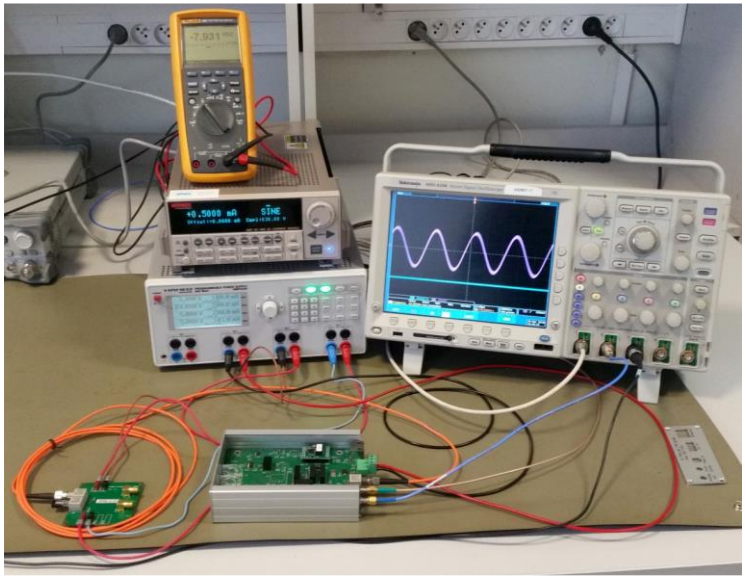
Pin diode module

- fast RF-gate to block the RF signal from the LLRF system when the Machine Protection System (MPS) event occurs,
- the blocking signal delivered using optical fiber,
- designed by ESS and verified behavior (by PEG) for power loss,
- equipped with Ethernet interface for device status monitoring and MPS testing,
- 125 pieces produced, tested and delivered to ESS (2021)



Electron pick-up interlock module

- measures the current from the multipacting,
- generates interlock if current threshold exceeded ,
- interlock signal passed to MPS via optical fiber interface,
- 118 pieces produced, tested and delivered to ESS (2021)



RF Splitbox

- distribution of the RF signal inside the LLRF racks,
- consists of 9 custom-designed power splitters optimized to achieve the lowest possible phase drifts and very low crosstalk,
- manufactured in different versions for different sections of the ESS linac (RFQ,MEBT,DTL,M-Beta….),
- 87 pieces produced and delivered to ESS,
- H-Beta version to be produced in 2022

Chosen firmware components preparation

FPGA firmware

- Firmware framework and the main accelerating field controller software implementation delivered by the ESS,
- PEG handles:
  - board support package (BSP) for the RTM carrier board,
  - functional FW for the LO-RTM (config and management),
  - functional FW for the piezo driver (config, management, acquisition, control signal shaping, etc)

MMC Firmware

- the IPMI functionality integration,
- provided access to the various types of sensors (voltage, temperature, etc) and Field-replaceable Unit (FRU) records,
- integrates support for both AMC, RTM and external (PPSM) PEG modules.

ESS Cavity simulator

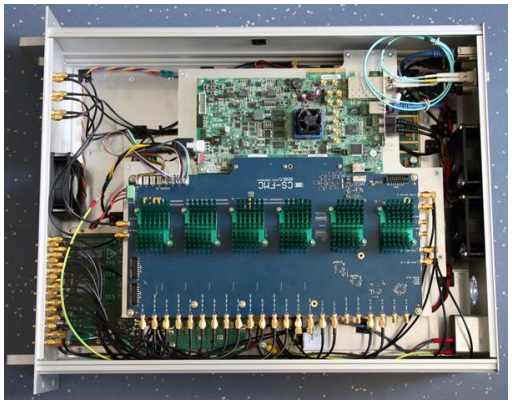
- designed to provide test env. for PEG installation and help the developers,
- simulates the M- and H-Beta cavities,
- includes: cavity dynamics, piezo detuning, beam current, amplifier nonlinearity and behavior

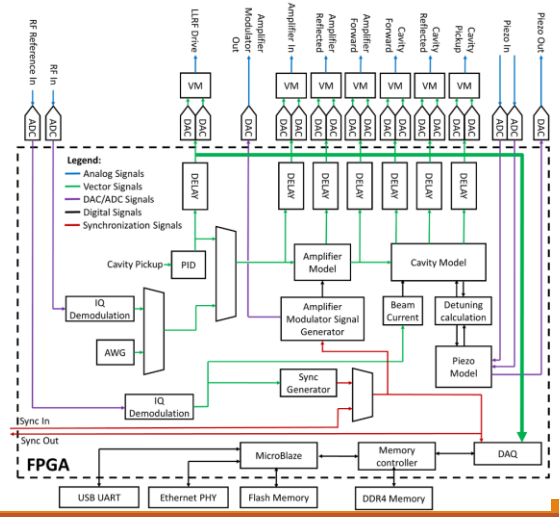
Design:

- high-performance FPGA with data converters and RF frontend,
- six (out of 7 in total) modules designed in-house (by ISE),
- the LLRF control signal is digitized then processed inside the FPGA firmware. The responses generated and converted to analog and RF outputs.

Status:

- 4 pieces build and delivered to ESS and partners,
- work on the last FW improvements in progres.





LLRF system integration and evaluation – local TS

Local LLRF hardware and software test stand established for:

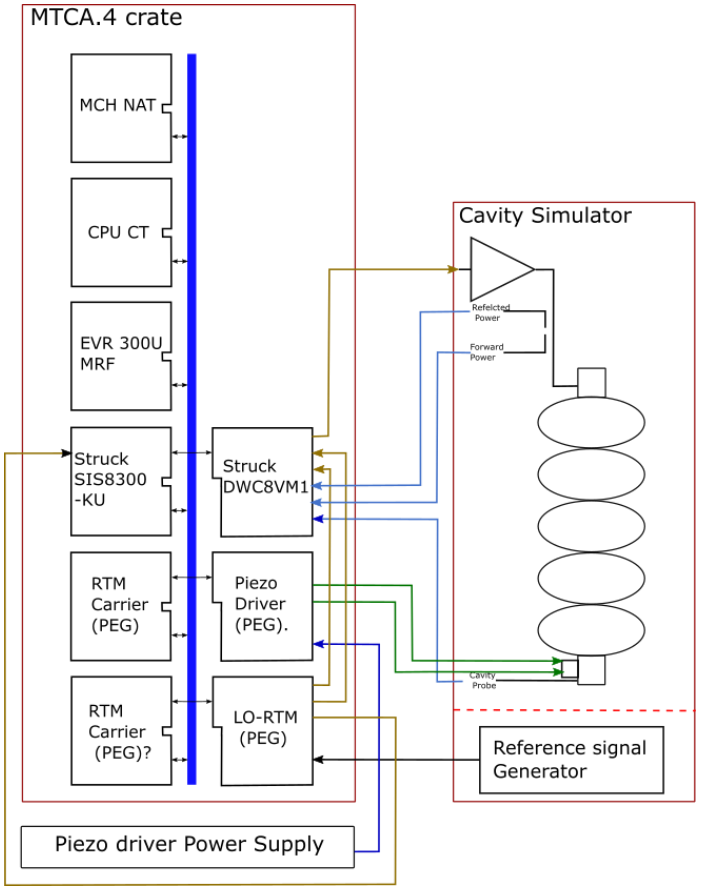
- system integration study,
- particular sub-modules verification and debugging,
- FW and software developement and testing,
- LLRF system tests procedures development.

Consists of:

- Fully equipped LLRF MTCA.4 system,
- Cavity simulator with „MO” functionally enabled

Status:

- updated with latest FW/SW and HW versions,
- currently Used for long term tests of components and SW development



LLRF systems integration, installation and evaluation

Procedure for system testing and installation:

- MTCA crate assembly in the lab.,
- local test with the cavity simulator (FAT),
- installation in the klystron gallery,
- the inner rack cabling,
- repeat the crate test with the CS attached to the patch-panel on the top of the rack (SAT).

Status:

- 8 systems installed Feb 2021,
- installations postponed due to the global market situation (semiconductor shortage),
- rest of the M-Beta systems (-4) installed 10.2022,
- Piezo driver to be installed later, when available.

Summary

Status:

- Most hardware modules produced in the finall quantities for M-Beta LLRF systems (apart from the piezo driver) and delivered,
- The H-Beta dedicated production – on-going. To be concluded beginning of 2023,
- Installation and verification work in progress. To be concluded middle of 2023.

Challenges and opportunities:

- „green field” and in-kind based facility,
- semiconductor market crisis.

Thank You