Controller Latency Improvements at REGAE

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Abstract

REGAE is a facility for ultrafast electron diffraction (UED) experiments based on a normal conducting S-band gun and buncher cavity. Their RF regulation is performed by a single cavity controller, implemented by an FPGA firmware and operating at 125 MHz. With a variant of the Struck SIS8300-KU controller board that is equipped with 250 MSps ADCs we were able to increase the frequency of the complete digital processing chain to 250 MHz. This includes the ADCs, field detection, feedback controller and DAC. Doubling the frequency reduced the overall controller latency by almost a factor of two. In the poster we show which firmware components had to be optimized or rewritten to achieve the 250 MHz clock rate.

Background

In a short pulse machine with normal conducting cavities the LLRF controller requires a low latency to regulate the higher cavity bandwidth. REGAE is one example for such a machine that would benefit from a lower controller latency, making it the ideal target for developing the digital LLRF controller enhancements.

The firmware implementation was developed for applications with sampling rates of 81.25 MSps (FLASH, European XFEL) and 125 MSps (REGAE). A prototype digitizer with a sampling rate of up 250 MSps (Analog Devices AD9643), provided by Struck Innovative Systeme, gave us the opportunity to explore the limits of the firmware.

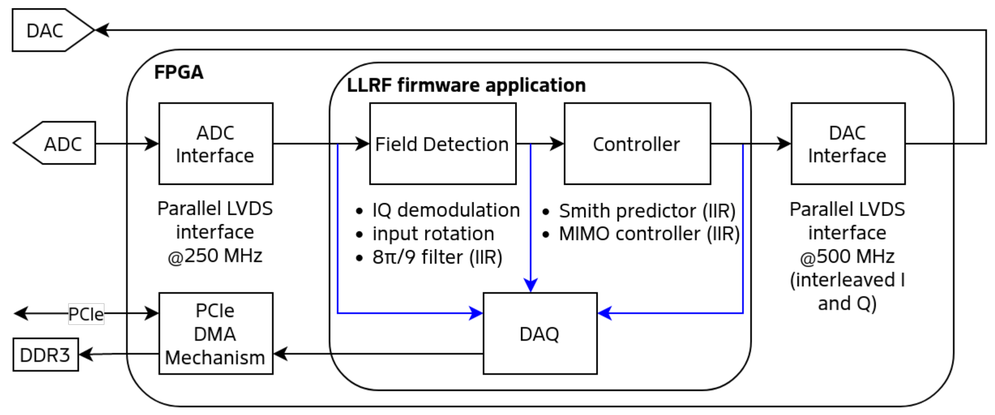

Figure 1: Simplified LLRF controller overview on a Struck SIS8300-KU board (MicroTCA.4)

Latency Contributions

		# clocks, old	# clocks, new	Latency, old @125 MHz	Latency, new @250 MHz
	ADC	12	10	96 ns	40 ns
	Field Detection	≈18	≈18	≈144 ns	≈72 ns
	Controller	≈32	≈32	≈256 ns	≈128 ns
	DAC	9	9	36 ns	18 ns
	Overall estimate	≈71	≈69	≈532 ns	≈258 ns

Table 1: LLRF controller latency contributions

Field Detection DSP chain at 250 MHz

IQ demodulation

- An optimized sliding window implementation with a pipelined multi-stage adder tree allows for the high clock rate
- Improved fixed point handling increases reusability
- New overflow detection increments a counter on overflow for improved diagnostics

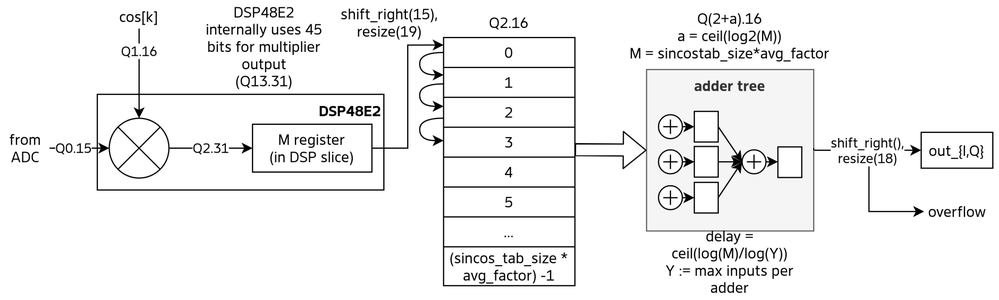

Figure 2: Schematic overview of the IQ demodulation in FPGA firmware

Input rotation

- Optimized use of DSP slices reduces logic and routing in regular FPGA fabric
- New overflow detection increments a counter on overflow for improved diagnostics

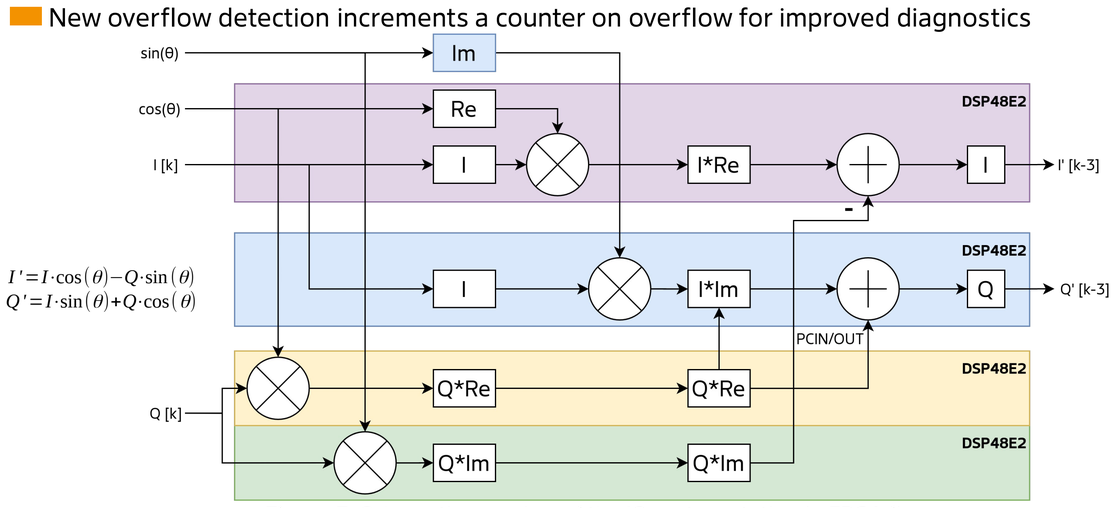

Figure 3: Schematic overview of the IQ vector rotation in FPGA firmware

2nd Order IIR Filter

Used in:

- Field detection (to filter out the 8π/9 mode excitation)
- Smith predictor
- MIMO feedback controller

Implementation:

- Transverse Direct Form II, optimized for max. frequency by using pipeline registers
- DSP48E2 (Xilinx Ultrascale) features a 3-input ALU, making the optimitzed structure possible

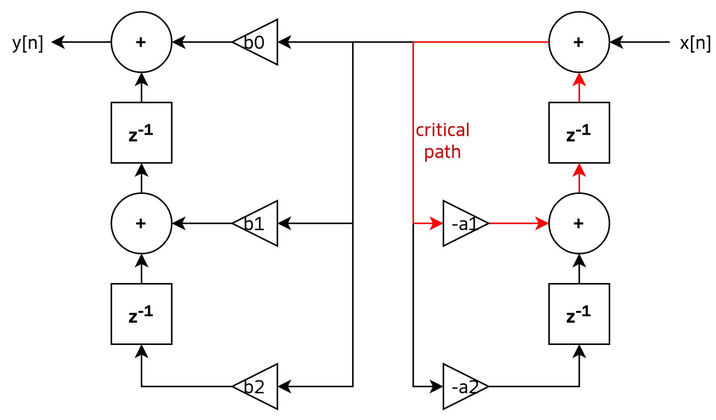

Figure 4: 2nd order IIR filter, transverse direct form II, textbook example

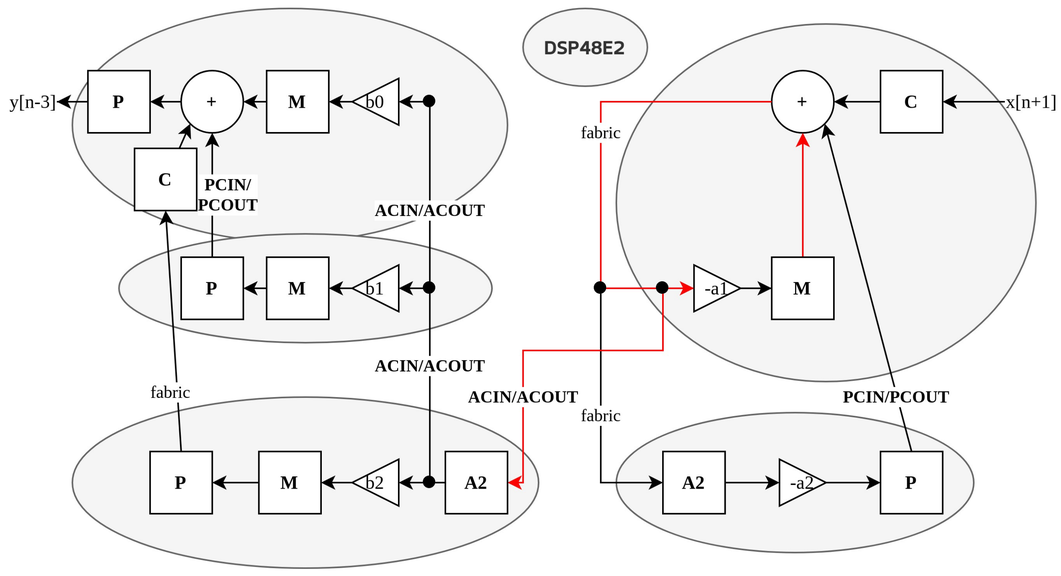

Figure 5: 2nd order IIR filter, transverse direct form II, optimized FPGA implementation

Various firmware-related improvements

- The AXI interface for data acquisition (DAQ) via DDR RAM is now 512 bits wide (instead of 256 bit), so it can provide sample data to the CPU at the full rate
- An improved retrieval of samples from the sin/cos lookup table lead to a reduction in FPGA logic
- The overall utilization shows that the increased frequency of the firmware could be achieved without an increase in FPGA resource usage

Table 2: Comparison of FPGA resource usage

Previous firmware @125 MHz		DSP	CLB/Carry	CLB/LUT	Register
	IQ demodulation	2	10	372	405
	Input rotation	4	6	143	38
	2nd order IIR filter	5	0	26	149
	Field detection	96	2058	20589	23251
New firmware @250 MHz		**DSP**	**CLB/Carry**	**CLB/LUT**	**Register**
	IQ demodulation	2	14	419	650
	Input rotation	4	0	37	39
	2nd order IIR filter	5	2	43	4
	Field detection	88 *	1898	23116	17459

* a new rounding feature was not optimized yet and thus omitted

Summary and further work

This work has shown that with the optimizations demonstrated on this poster, the digital LLRF controller developed by DESY is capable of operating at 250 MHz, reducing the latency by close to 50% compared with a 125 MHz operation. This also resulted in various improvements of the overall VHDL code quality.

Correct controller operation was verified in a test setup with a miniature cavity. As a next step, tests at the REGAE facility could show if there is a positive effect on the controller behavior.

FPGA firmware source code

- Git repositories at https://gitlab.desy.de/fpgafw
- The build environment (fwk) is available as free software under the Apache Licence 2.0
- Example firmware for Struck SIS8300-KU available under the CERN Open Hardware License (CERN-OHL-W-2.0)
- Verification of DSP components was done with CoSimTcp + Python

FWK FPGA firmware framework

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