



# CERN SPS LowLevel RF Architecture & Implementation

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## Acknowledgements:

J. Galindo, G. Kotzian, P. Kuzmanovic, M. Rizzi, L. Schmid, BE-CEM group and SY-RF-CS software team

Oct 11, 2022

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# SPS RF Upgrade project (LIU)

## LHC Injector Upgrade project (LIU)

**Protons:** doubling pre-LIU intensity [1, 2]

- 2.3e11 p+/bunch at extraction
- 25ns spacing, 72 bunches/batch, 4 batches

**Lead ions:** 50ns spacing (100ns pre-LIU) [3]

- 2.5e10 charges/bunch at extraction, 56 bunches
- Fixed-frequency Acceleration (FFA)
- Slip-stacking for 50ns bunch spacing
- Low RF noise (long injection plateau)

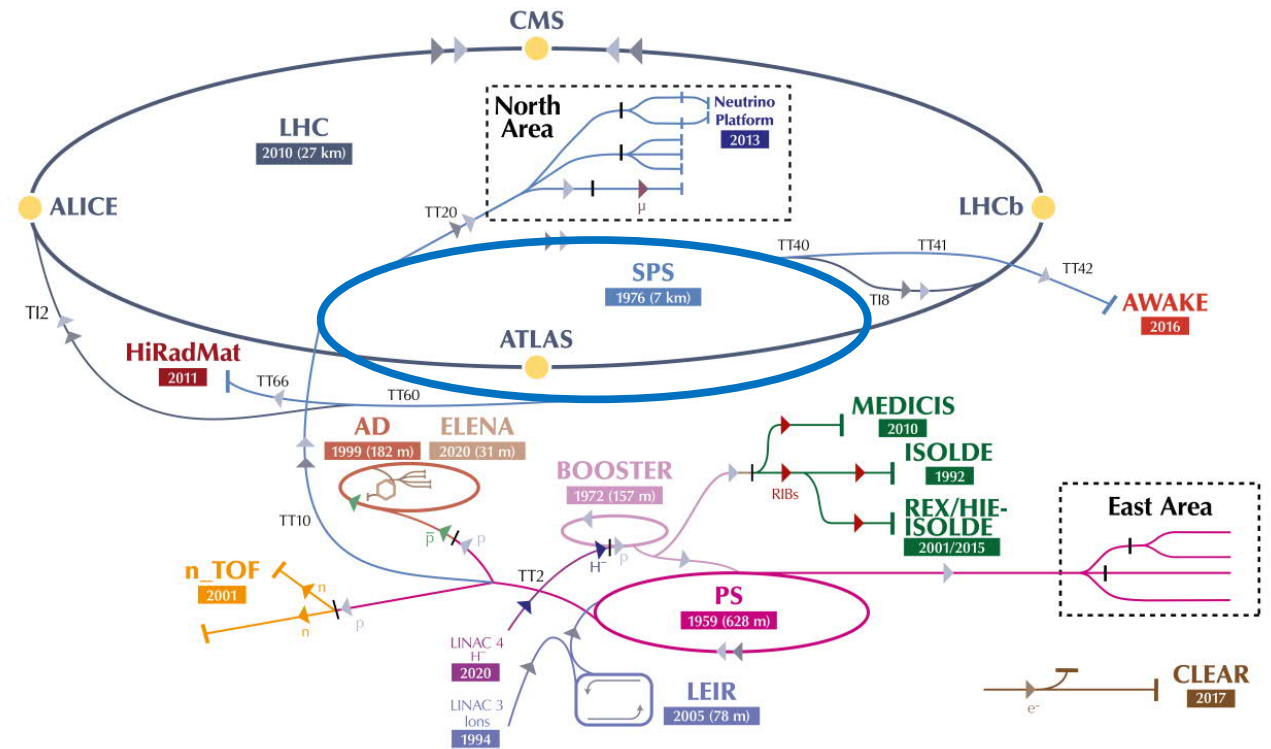


Fig1 – CERN accelerator complex

# SPS RF Upgrade project

## Completely new RF system

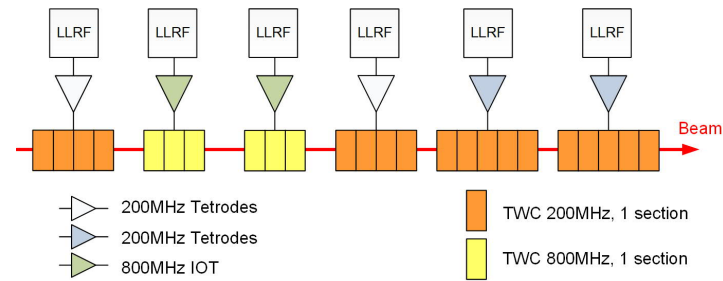
- From 6 to 8 200MHz Cavities
- New 1.6MW solid-state amplifier systems (2x)

## New digital LLRF

- MTCA for 200MHz Cavity-Controllers (RF feedback) [4]
- MTCA for Beam control (beam based loops) [5]

## Infrastructure

- Huge decabling/recabling campaign
- Integration of legacy HW



↓ LS2 (2019-2020)

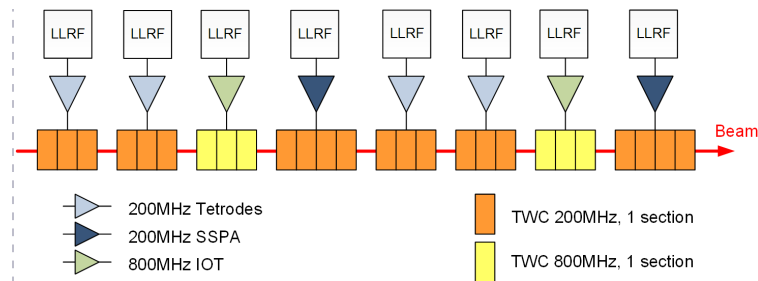


Fig3 – SPS RF Upgrade in Long-shutdown 2 (LS2)



Fig3 – SPS Solid-state amplifier systems (32 towers of 140kW!)

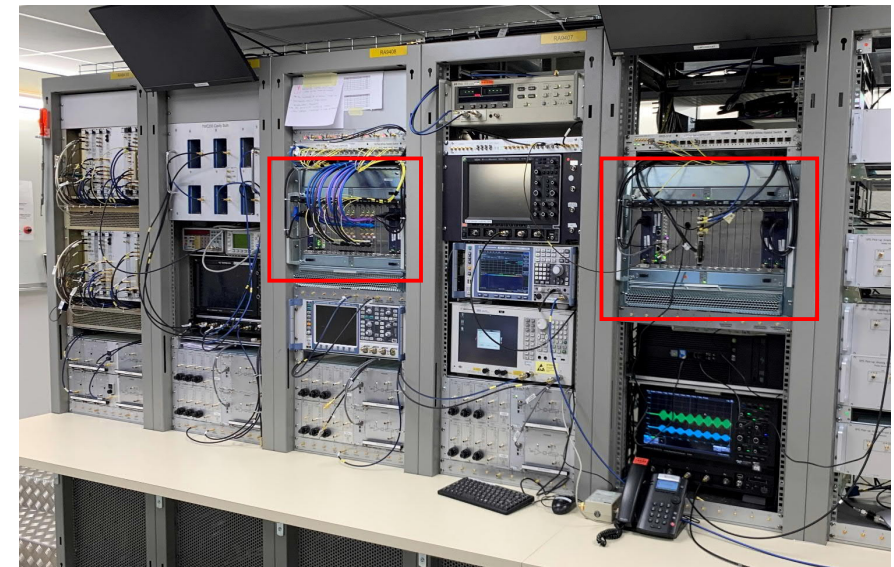


Fig4 – SPS low-level RF system (MTCA)

# SPS RF Upgrade project

## SPS RF cavities

- Four → Six 200MHz travelling wave cavities (LS2)
- Two 800MHz travelling wave cavities (LS1)

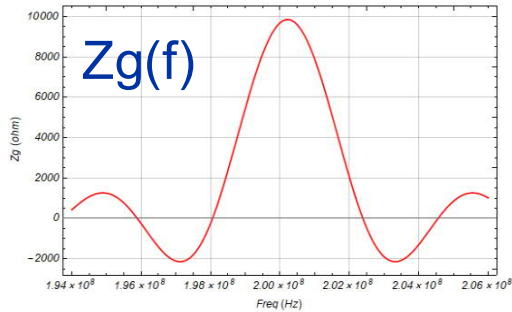


Fig5 – 200MHz 3-sections cavity, Zg(f)

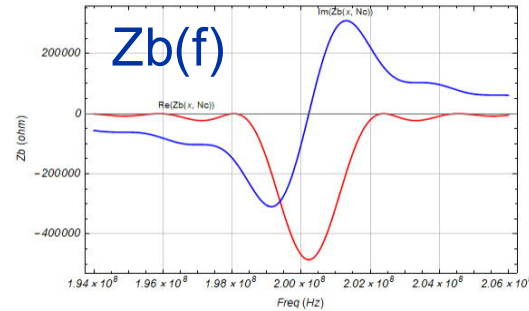


Fig6 – 200MHz 3-sections cavity, Zb(f) real( red), imaginary (blue)

$$Z_g(f) = R_1 \left\{ \text{sinc}[\tau(f - f_0)] e^{-j\pi\tau(f - f_0)} + \text{sinc}[\tau(f + f_0)] e^{-j\pi\tau(f + f_0)} \right\}$$

$$Z_b(f) = -R_2 \left\{ \begin{array}{l} \text{sinc}^2[\tau(f - f_0)] + \text{sinc}^2[\tau(f + f_0)] \\ -j \frac{1 - \text{sinc}[2\tau(f - f_0)]}{\pi\tau(f - f_0)} - j \frac{1 - \text{sinc}[2\tau(f + f_0)]}{\pi\tau(f + f_0)} \end{array} \right\}$$

$Z_g(f) \neq Z_b(f)$

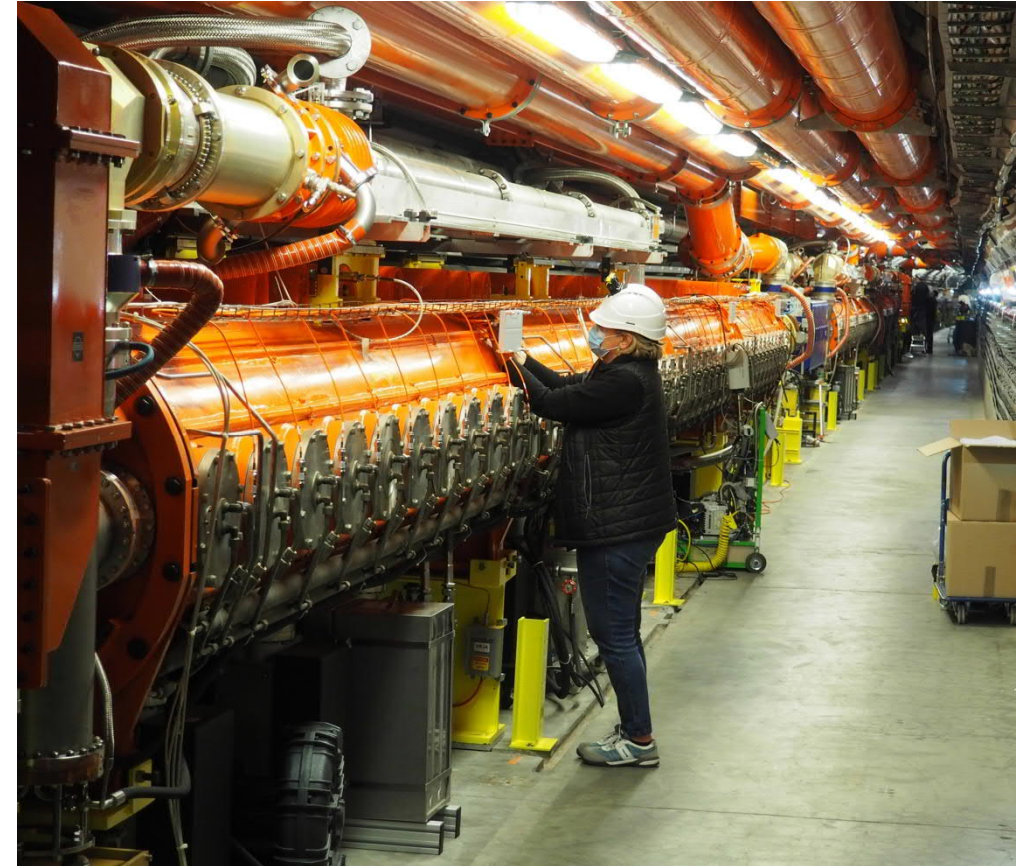


Fig7 – 200MHz travelling wave cavity

Parameter	3-sections	4-sections
Cavity filling time t (ns)	462	621
Resistance driven by generator R <sub>1</sub> (Ω)	9851	13237
Resistance driven by beam R <sub>2</sub> (Ω)	485202	876112

# SPS LLRF Architecture

## Architecture based on White-Rabbit

- White-Rabbit B-Train: Bending field
- White-Rabbit RF-train:
  - RF frequency (FTWs) @  $f_{rev}$
  - Voltage setpoints
- Locked on low noise 10MHz Master clock (GPS receiver)
- Fixed latency, link stabilization [6, 7]
- Sampling clock re-construction from WR data stream in all RF station/crate (1 fiber link for clock & data)

## Direct sampling at 125MSPs of 200MHz RF

- Fixed frequency sampling & processing clock (Predictable, low noise clocks, easier for HW)
- Higher complexity for DSP (Resampler, variable fractional delay - VFD)

## 10Gbits links

- Cavity voltages → Beam-Control (200MSPS)
- Long Damper → Cavity-Controllers (20MSPS)

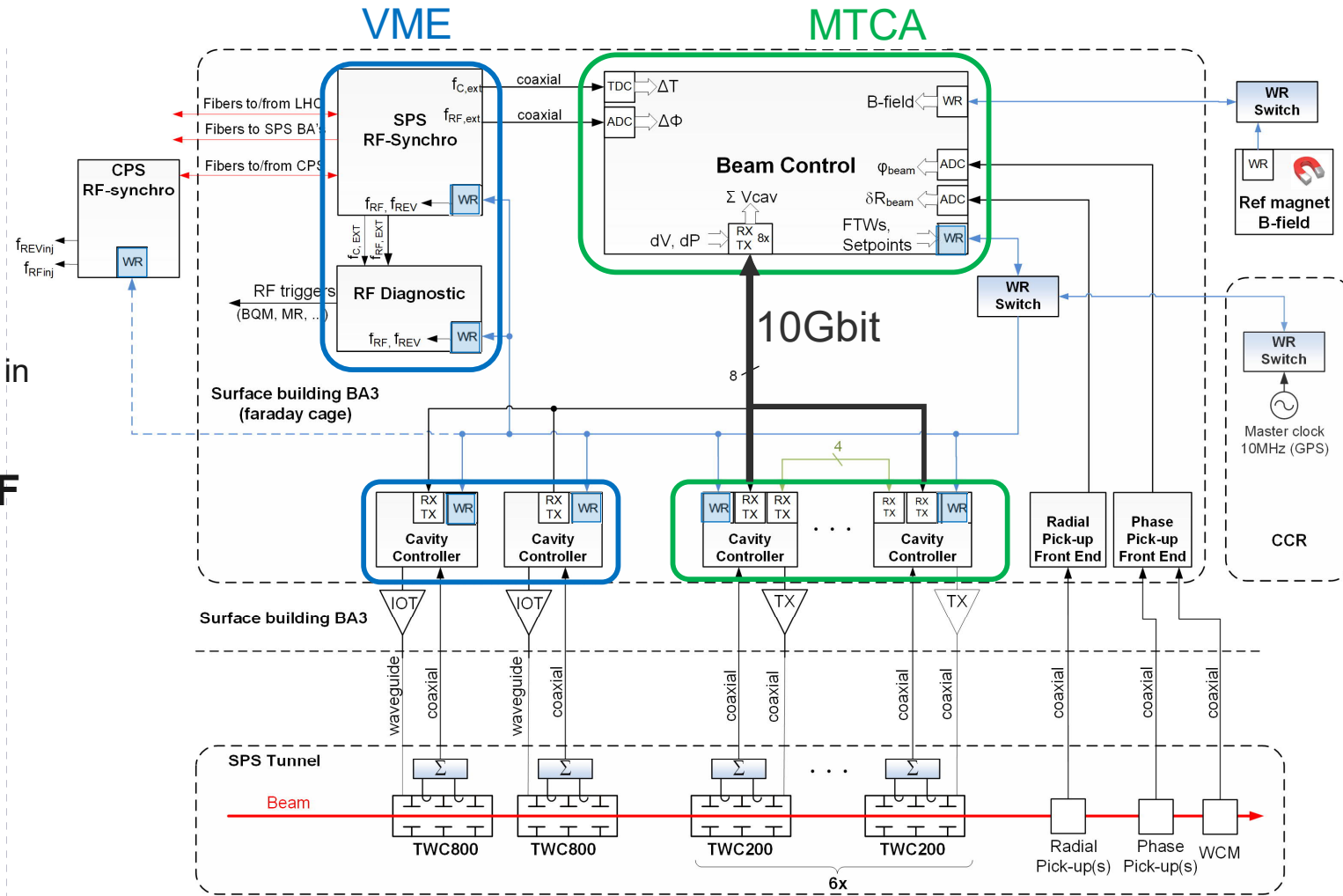


Fig8 – SPS low-level Architecture - platforms

# SPS LLRF Architecture

## Distributed NCO's

- Every node has its own NCO (RFNCO)
- Running on fixed frequency clock (125MHz)
- Synchronous reset through White-Rabbit (WR) (fixed latency)

## RF frequency

- Revolution frequency (FTW) computed in Beam-Control (master)
- FTWs distributed over WR (fixed latency)

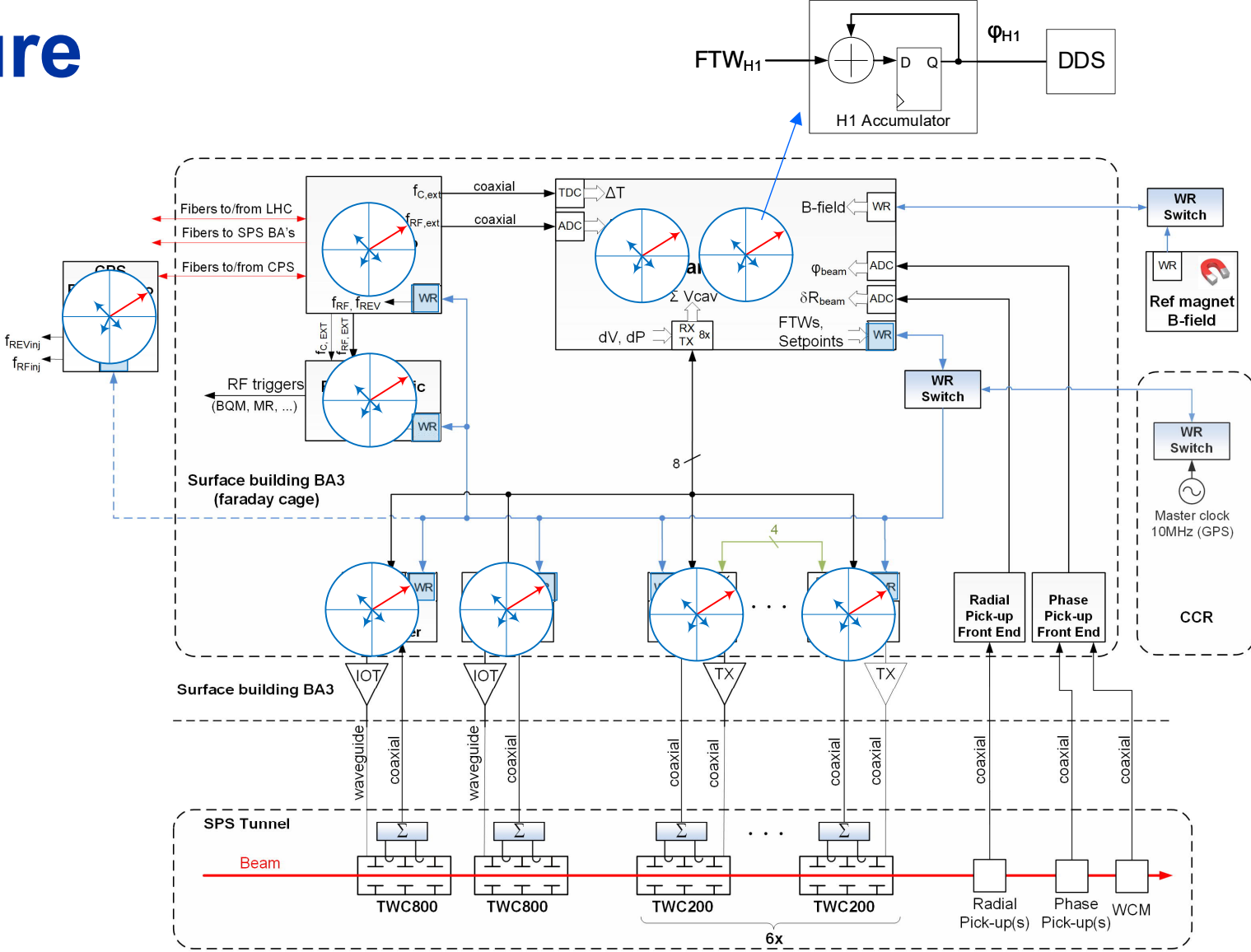


Fig9 – SPS low-level Architecture – distributed NCOs

# SPS LLRF Architecture

## Numerical Control Oscillator (NCO)

- IP Core in all RF stations
- Reference for RF synchronization
- Allow complex RF gymnastics required for ions acceleration:
  - Amplitude & Frequency modulation used for fixed-frequency acceleration, slip-stacking [8]
- 5 Phase accumulators & 5 FTW's
  - Revolution phase
  - Slippage phase (ions slip-stacking)
  - Frequency modulation
  - Demodulation LO
  - Modulation LO

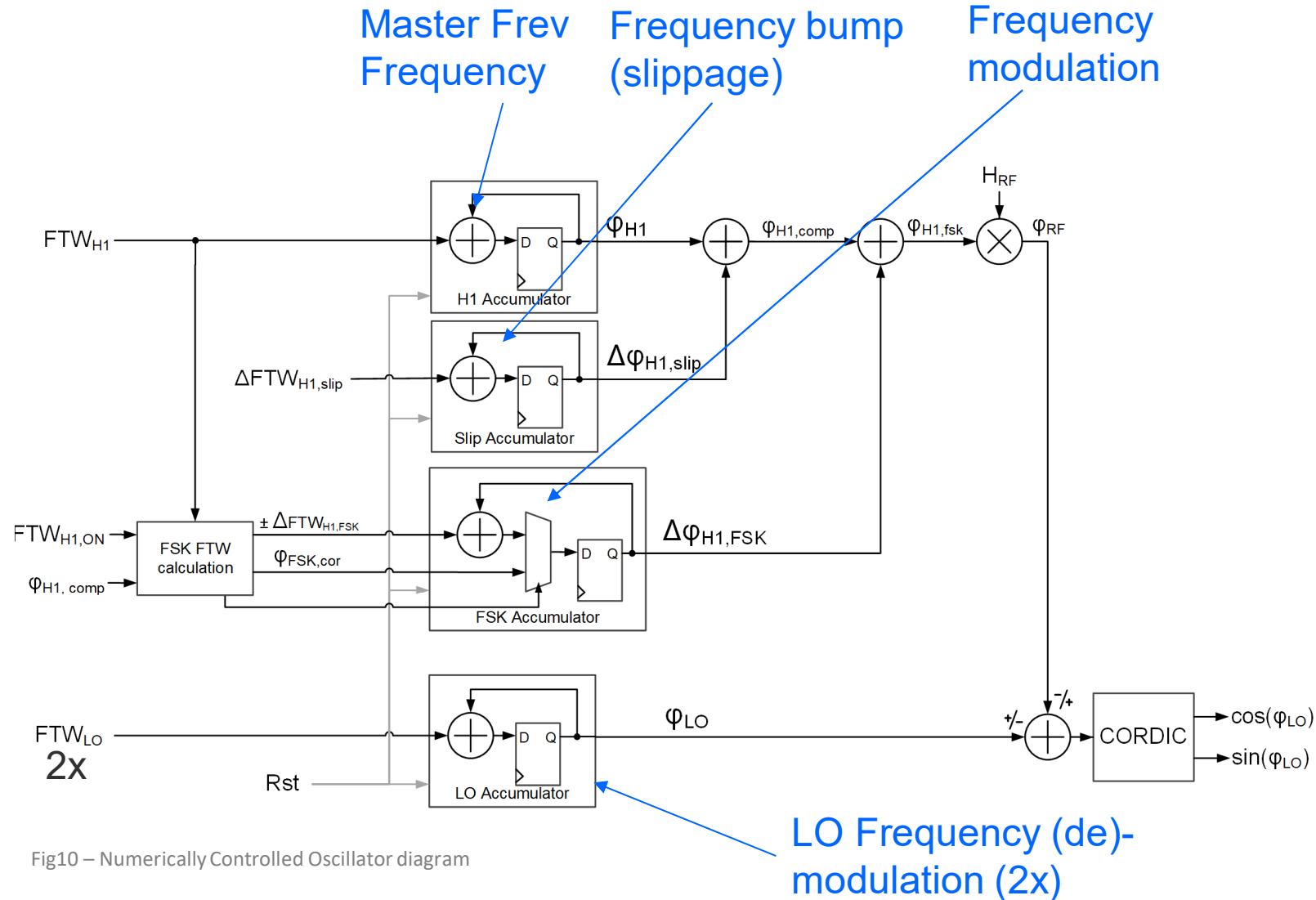


Fig10 – Numerically Controlled Oscillator diagram

# SPS LLRF Signal processing

## Re-sampler

- Required for bunch-per-bunch signal processing
- Change from **clock-synchronous** data rate (125MHz) to **bunch-per-bunch** data rate (200MSPS), and vice-versa
- Synchronized to the NCO
- Phase, radial loops are bunch synchronous
- Farrow based Variable Fractional Delay (VFD) filter with Horner-architecture polynomial interpolation [9]

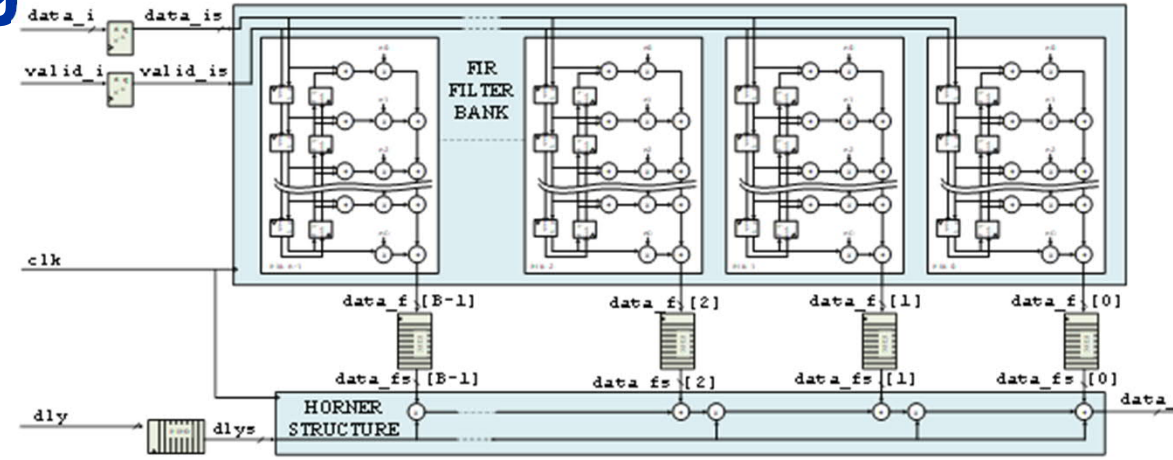


Fig11 – Resampler, Farrow VFD with Horner architecture polynomial interpolation

## Variable delay

- Some loops need an exact one-turn delay
  - One-Turn delay Feedback, One-Turn delay Feed-Forward [4, 10]
- Variable integer+fractional delay
  - Integer delay: addressable shift register
  - Variable delay: FIR, 4<sup>th</sup> order Lagrange polynomial interpolation
- No data rate change (125MSPS)
- Delay computed from FTW (NCO)

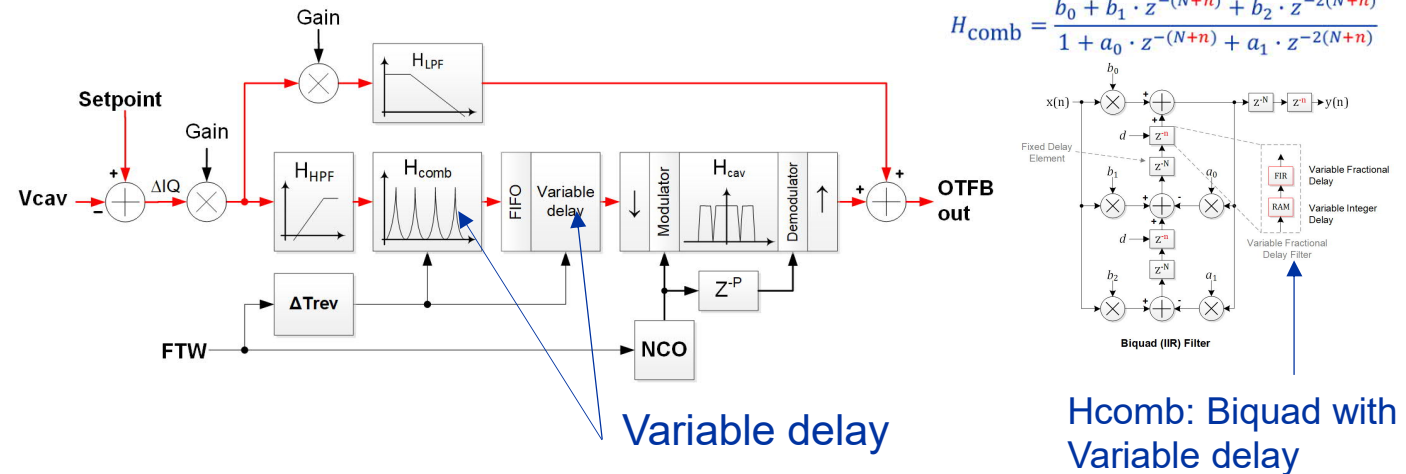


Fig12 – 200MHz RF feedback - Variable delay, Comb filter biquad

# SPS 200MHz Cavity-controller - Hardware

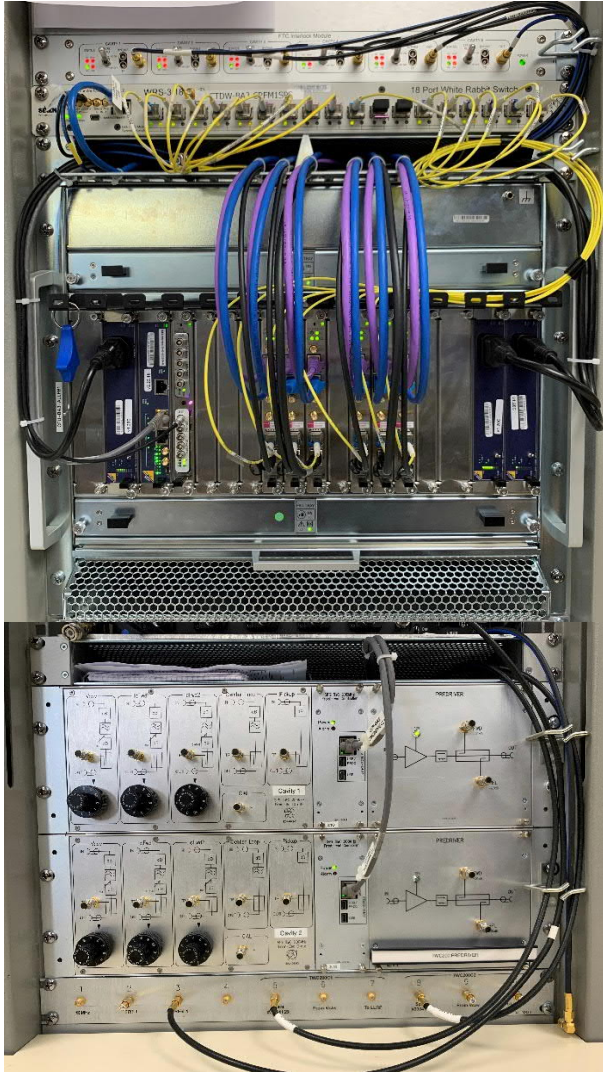
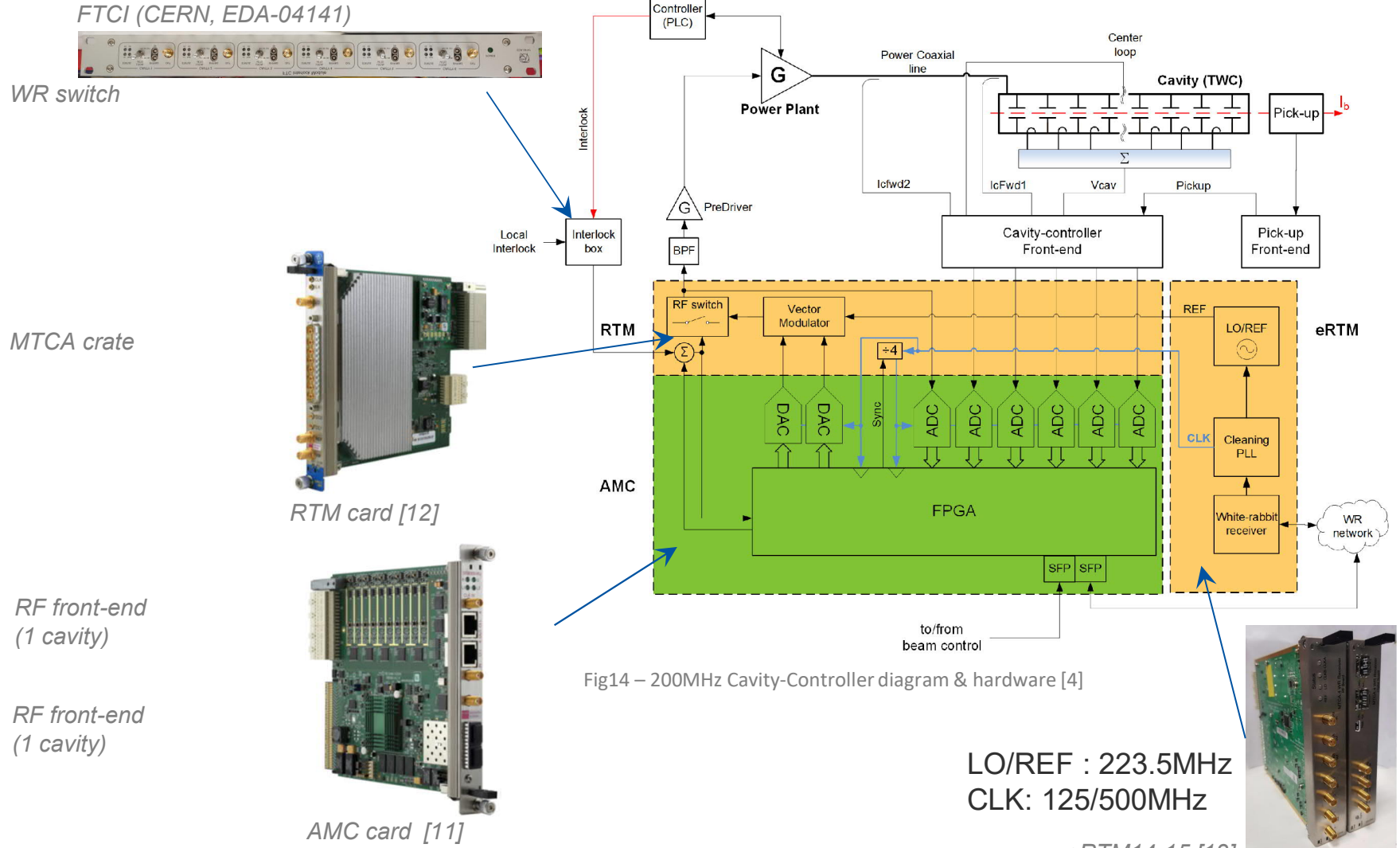


Fig13 – 200MHz Cavity-Controller MTCA crate + Analog Front-end



# SPS 200MHz Cavity-controller - Feedback loops

## 1. Polar-loop

1. Gain & phase loop
2. 20us response time (CL)
3. Reduce amplifier noise
4. Compensate amplifier gain/phase drifts

## 2. RF feedback (OTFB)

1. One-Turn Delay Fdbk, BW  $\approx$  4MHz
2. Reduce transient beam loading

## 3. One-Turn FeedForward (OTFF)

1. Measure beam current
2. Reduce transient beam loading

## 4. Longitudinal Damper

1. Dipole mode (phase modulation)

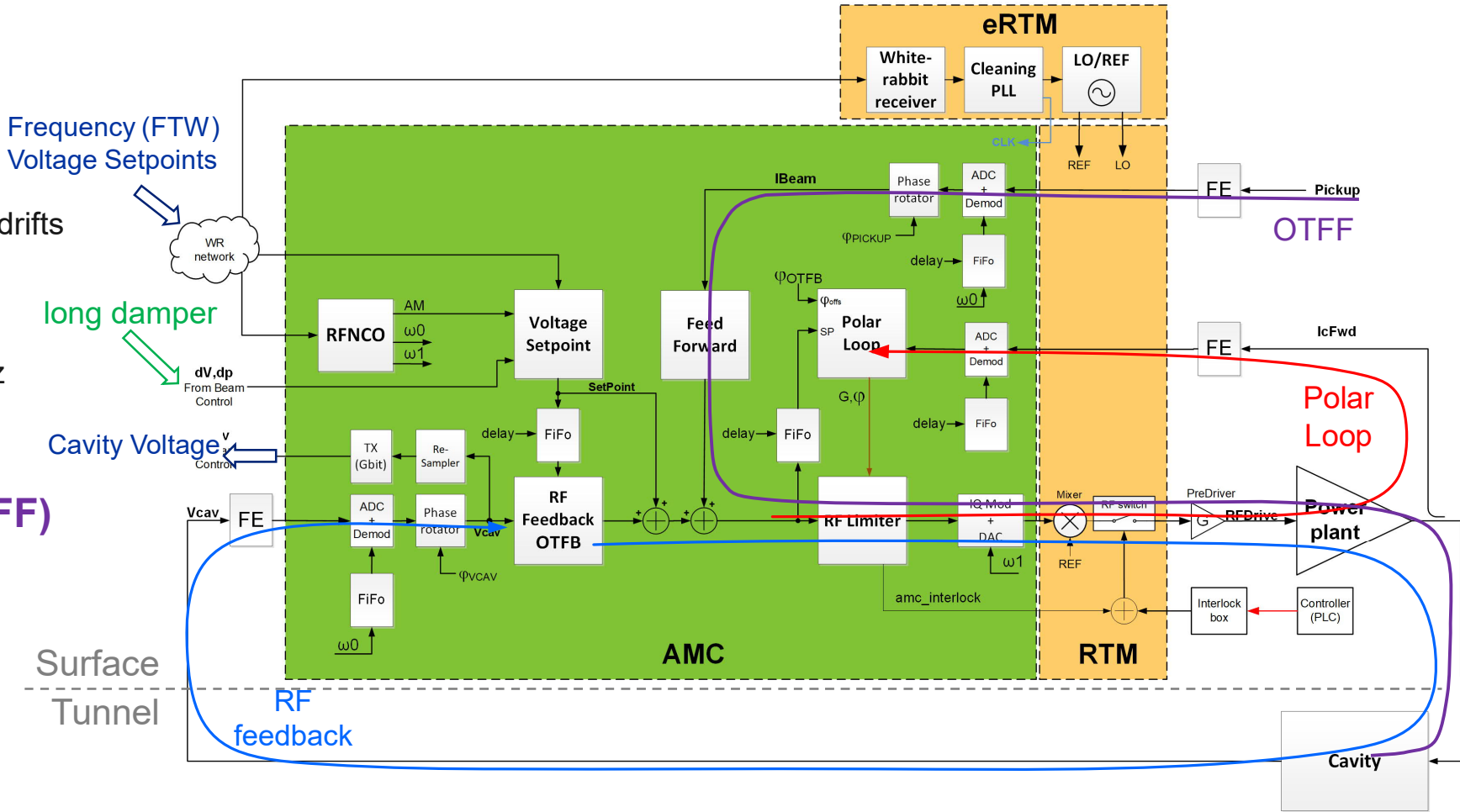


Fig15 – 200MHz Cavity-Controller feedback loops [4]

Cable + amplifier delay  $\approx$  3us

# RF Frequency and RF (de)-modulation

## Synchrotron → RF ramp

- Sweeping RF (avg) = 200+/-2 MHz, BW ≈ 4 MHz
- AM & FM modulation for ions accelerations

## RF demodulation (input)

- Direct sampling of 200MHz RF at 125MSPS (fixed frequency)
- Alternative with down-mixing with LO at ~223.5MHz (LO fixed freq, optimized for IF harmonics aliasing)

## RF modulation (output)

- Single-side band transmitter scheme
- REF=LO at ~223.5MHz, IF at ~23.5MHz +/-2MHz
- External BPF on VM output to remove LO leakage and image frequencies

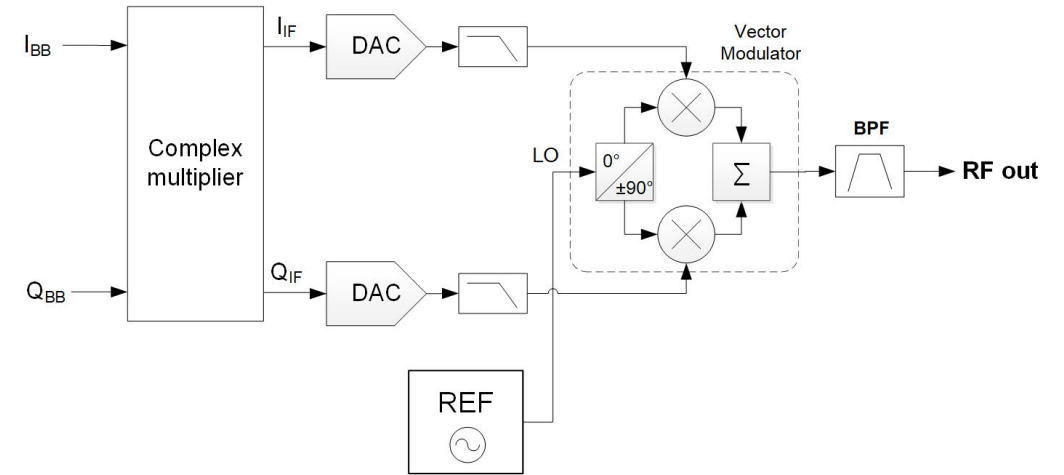


Fig16 – 200MHz Cavity-Controller Vector modulator



Fig17 – 200MHz Cavity-Controller vector modulator spectrum

# SPS 200MHz Cavity-controller - Phase noise

## RF Phase noise is critical for ions acceleration

- Long injection plateau (>20s)
- injection synchrotron frequency ~1kHz
- Goal: fs=300Hz to 2kHz, <-120dBc/Hz

## LO/REF (223.5MHz)

- -127dBc/Hz @ 1kHz
- 63fs (100Hz to 10MHz)

## Voltage Sum of 6 cavities (close loop)

- -128dBc/Hz @ 1kHz
- 140fs (100Hz to 10MHz)

## HL-LHC requirements are ~20dB lower @8kHz

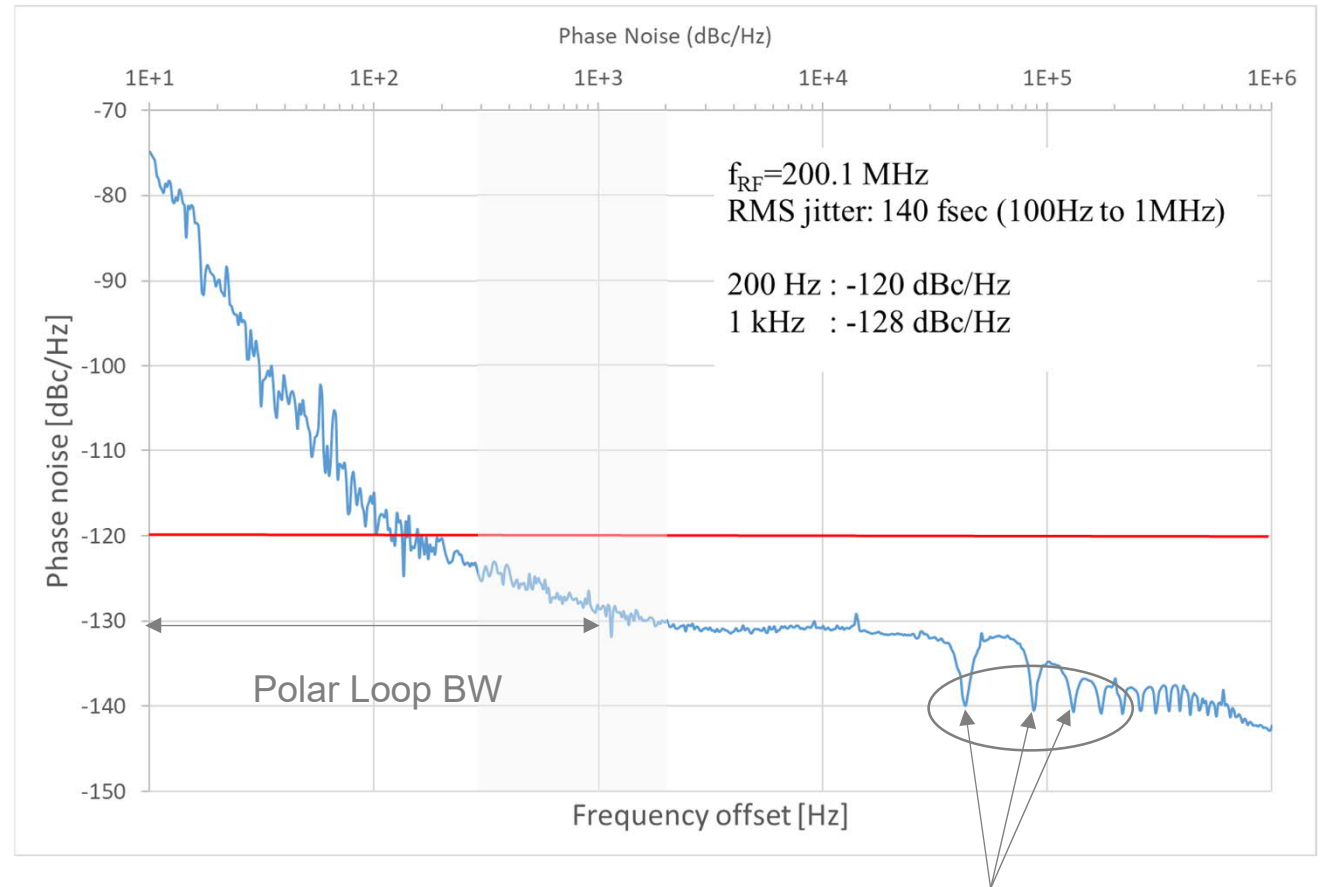


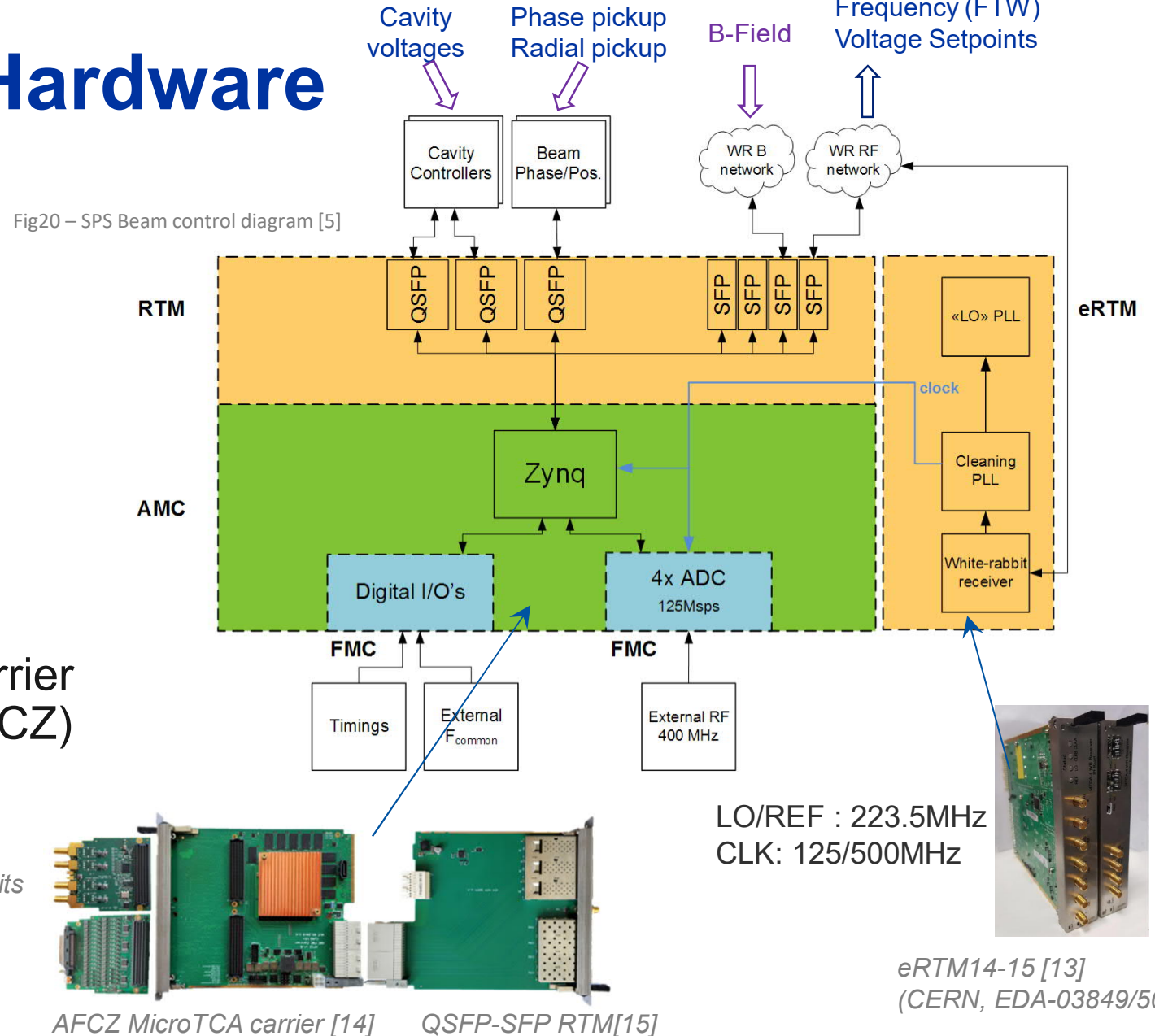
Fig18 – 200MHz Cavity phase noise (without beam)

# SPS Beam-Control - Hardware



Fig19 – SPS Beam control crate

1. MicroTCA Advanced Mezzanine Carrier (AMC) with a Zynq UltraScale+ (AFCZ)
2. Beam-based loops
3. Frequency program



# SPS Beam & results

## Protons

- Intensity achieved for LHC beam:
  - 1.84e11 p/bunch, 72 bunches, 25ns spacing
  - 1.4e11 p/bunch, 4x 72 bunches, , 25ns spacing
- **HL-LHC target: 2.3e11 p/bunch**
- 100% Amplitude modulation with OTFB

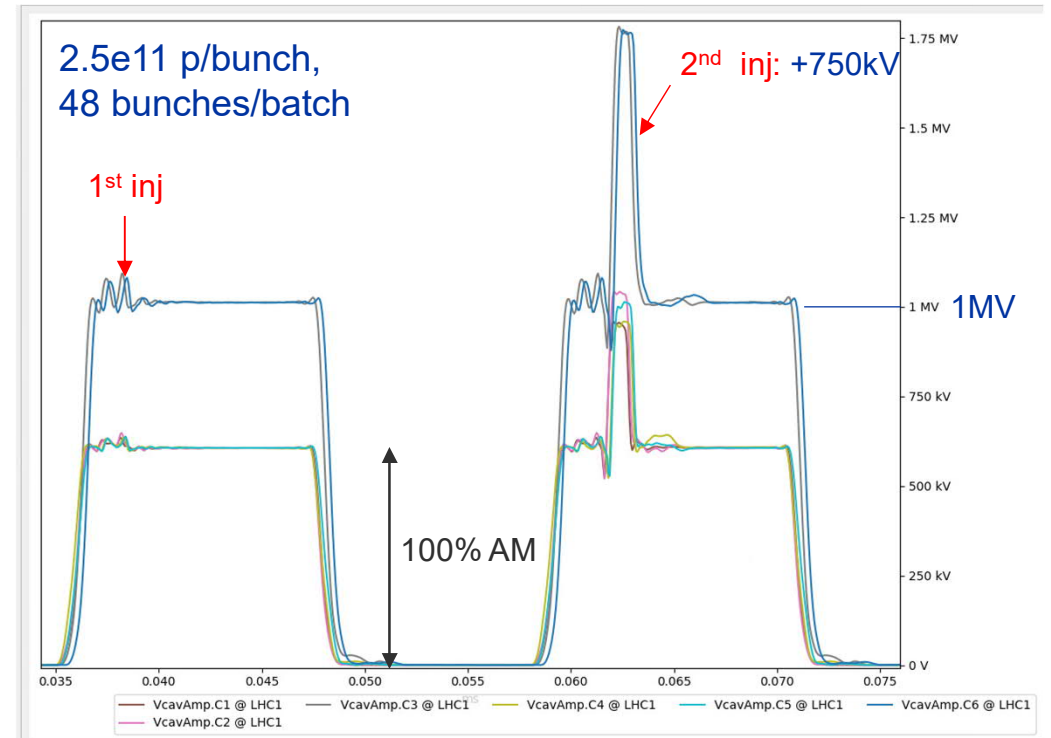


Fig21 – Cavity voltage with Beam loading, 100% AM

# SPS Beam & results

## Ions

- Cavities splitted into two groups (2 RF frequencies)
- Fixed-frequency acceleration with OTFB
  - 100% Amplitude & Frequency modulation
- slip-stacking from 100ns to 50ns bunch spacing [8]
- Beam commissioning on-going

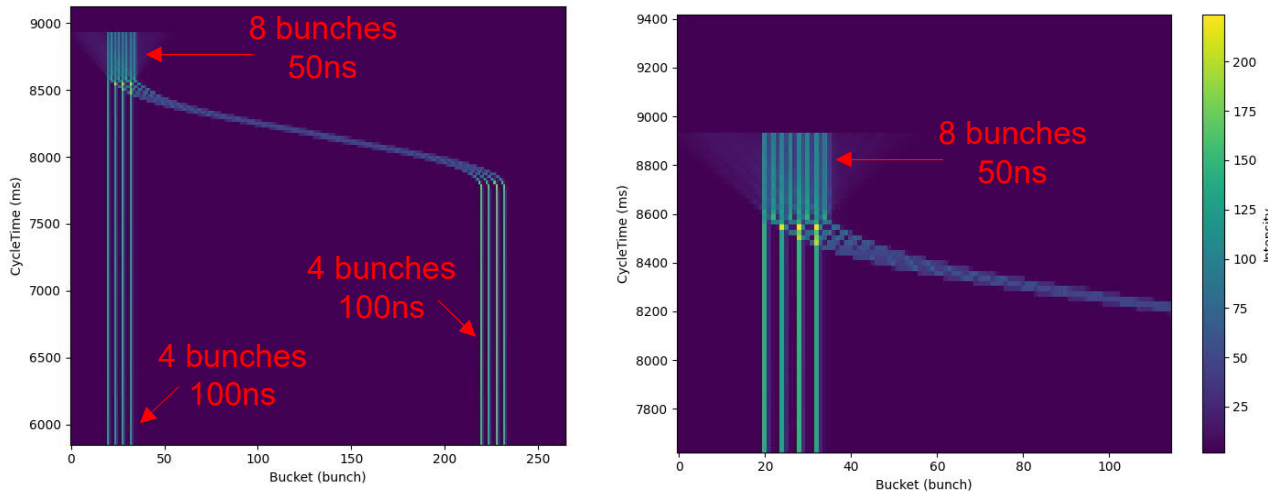


Fig22 – Fast BCT during slip-stacking, 2 batches of 4 bunches

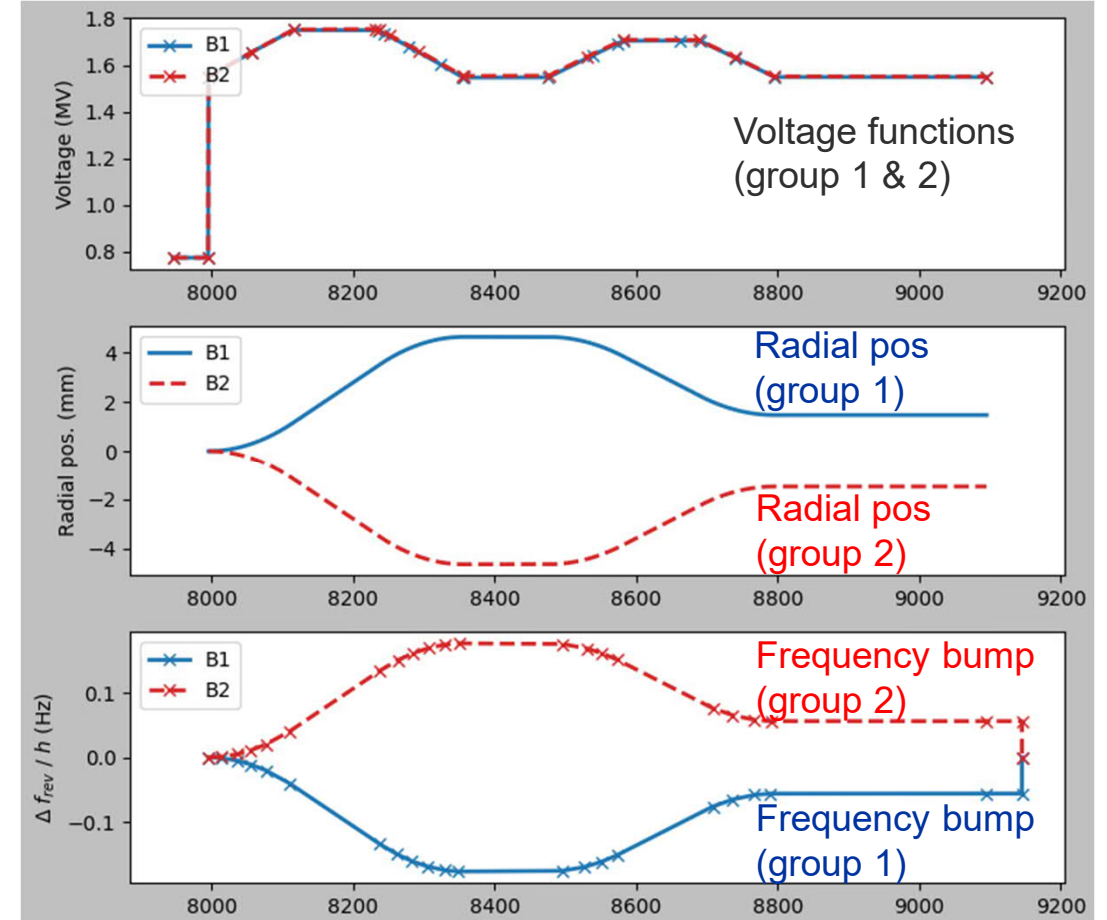


Fig23 – Frequency & voltage functions for slip-stacking

# Conclusion

## Steep learning curve

- MTCA platform
- Fixed sampling & processing clock
- Resampler, fractional variable delay

## Good architecture choices

- Fixed frequency clock, RFNCO flexibility
- White-rabbit for clock and data transmission

## We benefit from MTCA (PCIe)

- Fast bus bandwidth (Long acquisition buffer for troubleshooting)
- Compactness, diagnostics, HW hot-swap, Redundancy (PM)
- Use of COTS (Home-made HW in LHC or L4)

## Almost two years of operation

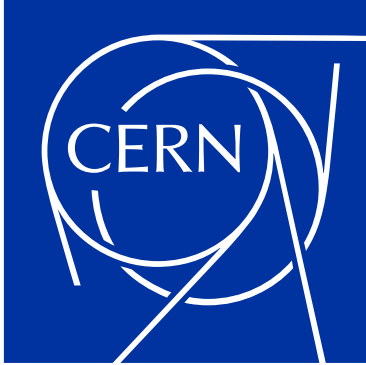
- Pre-upgrade performance exceeded
- Ramping up towards HL-LHC intensity

## Future CERN LLRF projects on MTCA

- High-Lumi LHC (crab-cavities)  
=> much high RF noise requirements
- PS 200MHz Cavity-Controllers
- AWAKE2 (S and X-band linacs)

## White-rabbit

- Much improvements to achieved the clock phase reproducibility, target < 13ps (1deg @ 200MHz)  
Achieved:  $\sigma=16\text{ps}$ , and few erratic jumps of 75ps under investigation (GTXE2, Kintex), but none with GTXE1 (spartan 6)
- In depth WR/clock performances under characterization



[home.cern](http://home.cern)

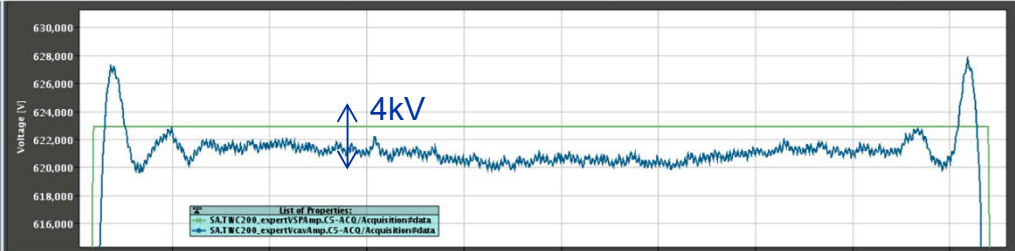
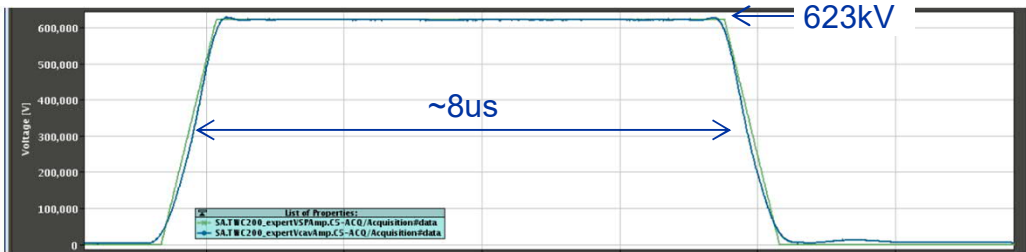
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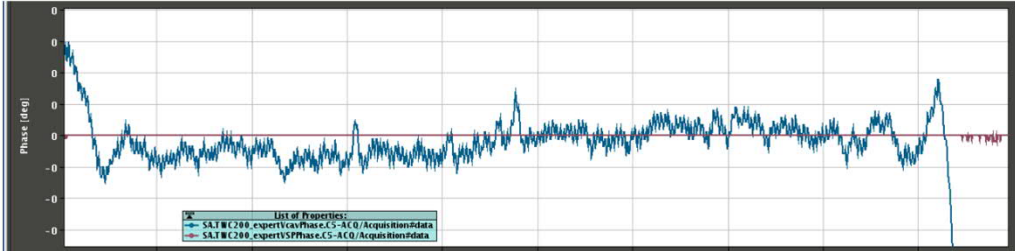
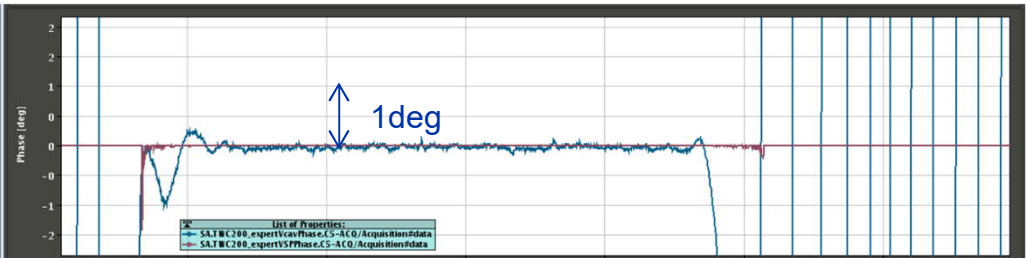
# Spare slides

# Cavity voltage in AM (3-sections, no beam)

Amplitude:



Phase:



- Frf\_inj = ~198.5MHz
- Frf\_on = 200.2MHz
- RF ramp on/off 1us
- Modulation at 1\*Frev
- Pulse ~11us
- Polar loop + OTFB closed

Fig24 – Cavity voltage in Amplitude modulation, no beam, 3-sections cavity