FPGA implementation of a multi-harmonic cavity controller for the Proton Synchrotron Booster at CERN

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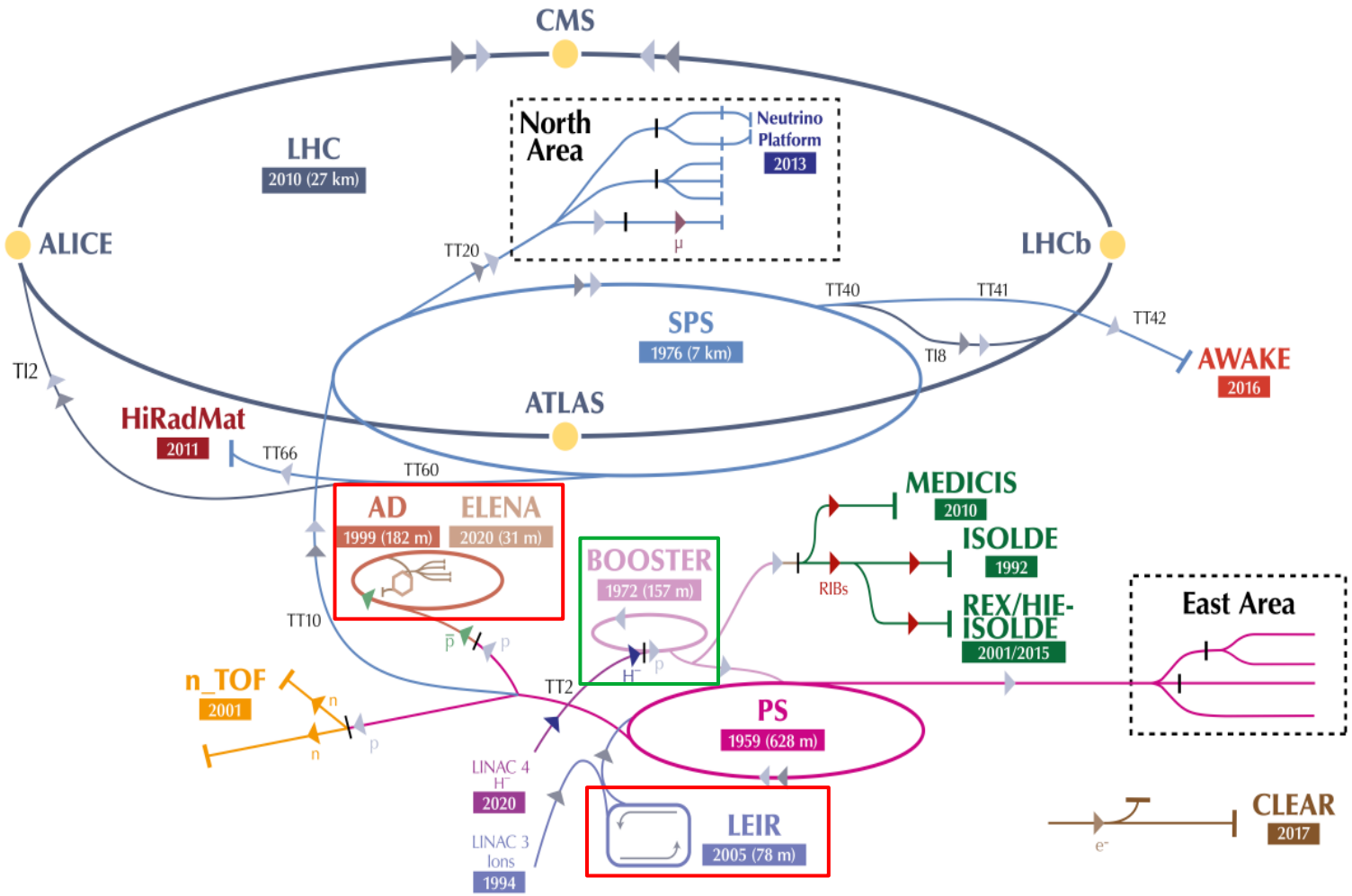
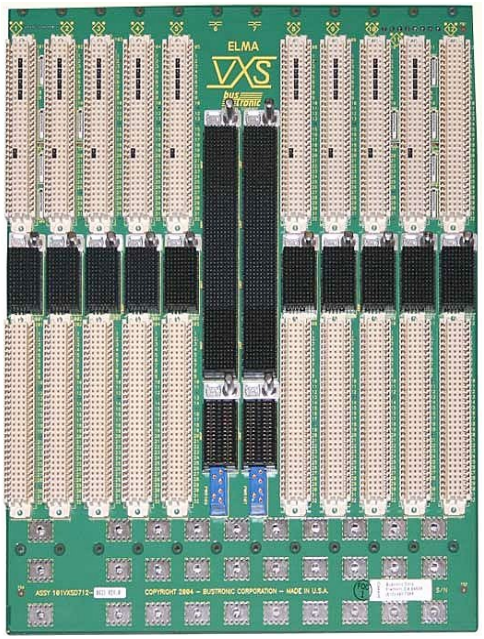
The CERN accelerator complex
Complexe des accélérateurs du CERN



VXS LLRF architecture

VXS



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DSP

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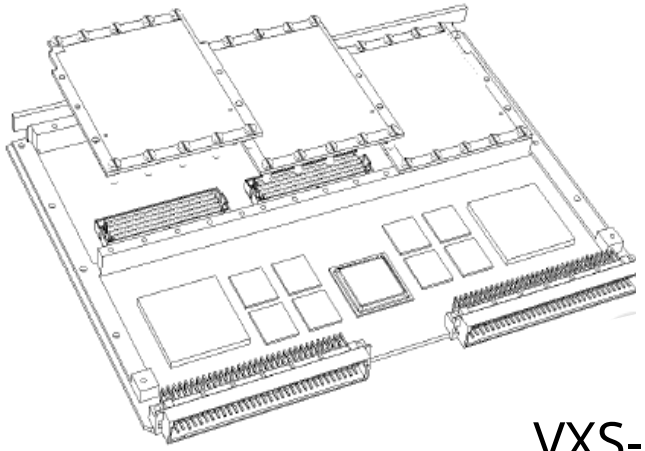
FMC-Carrier



VXS-DSP-FMC-Carrier

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VXS LLRF architecture

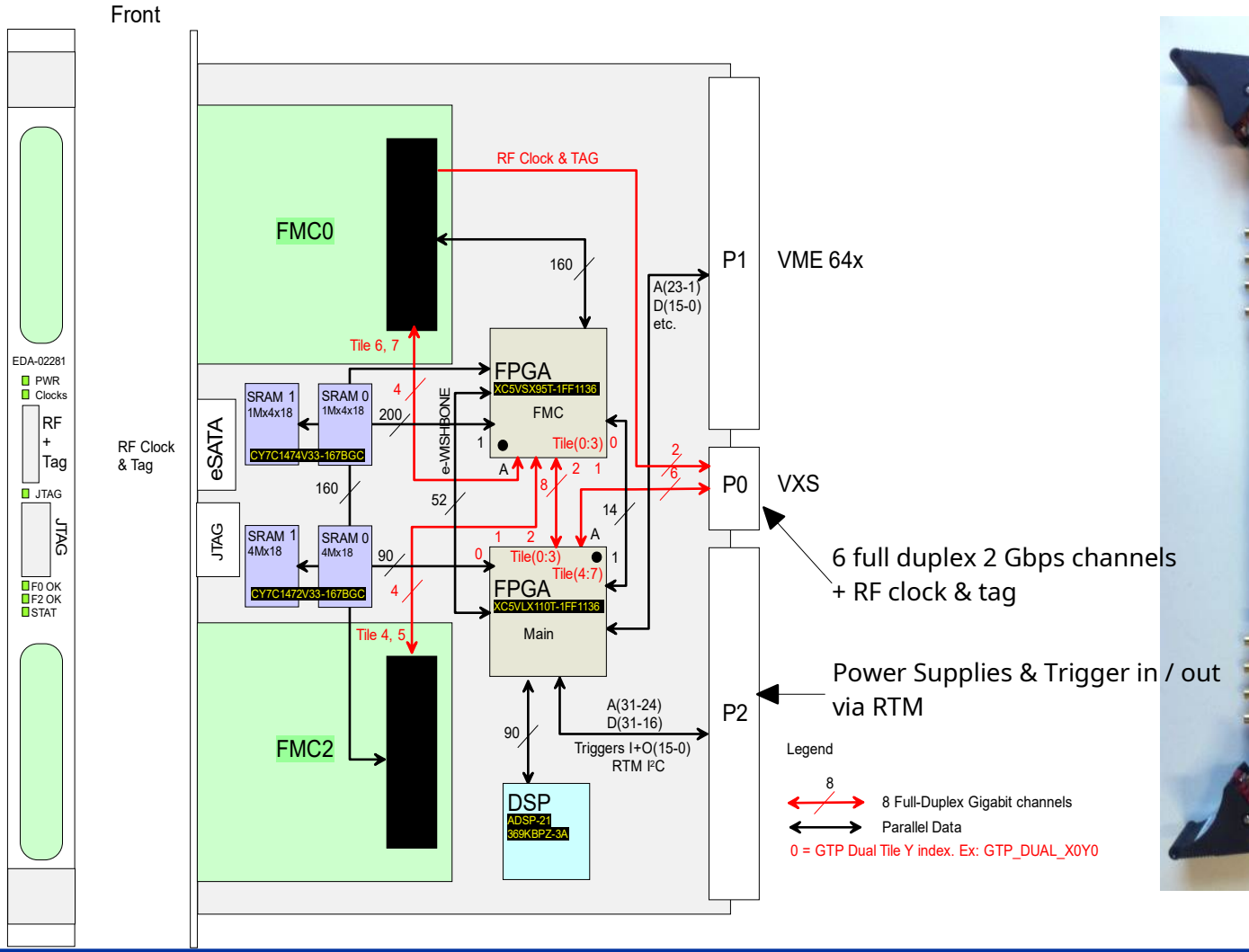
Custom (standard) electronics

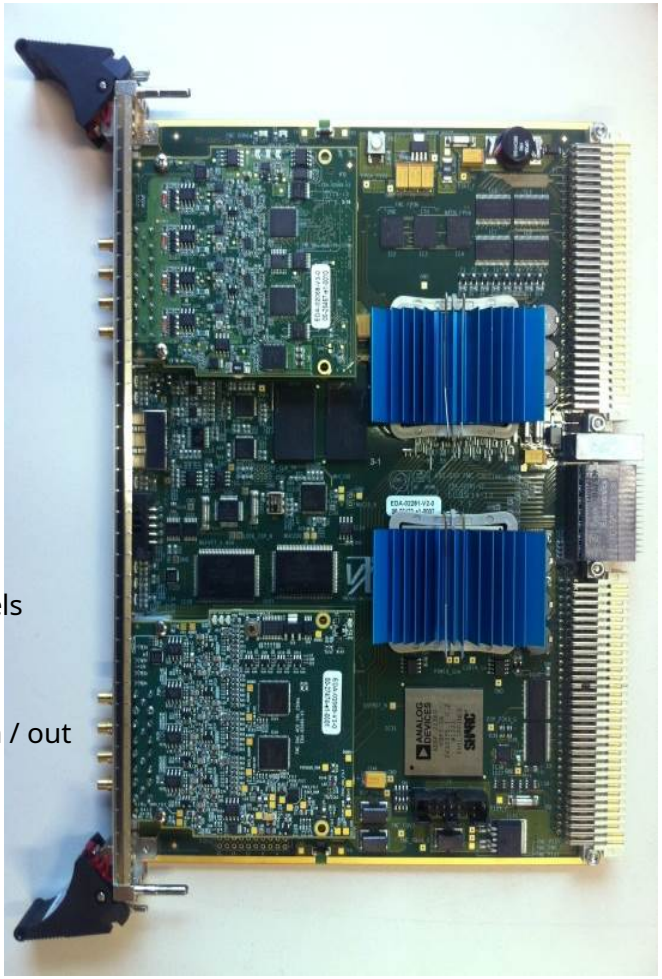
- VXS-DSP-FMC carrier
- VXS switch
- Custom FMCs: 4ch-16b-125MSPS ADCs, 4ch-16b-250MSPS DACs, MDDS…

Custom firmware, software

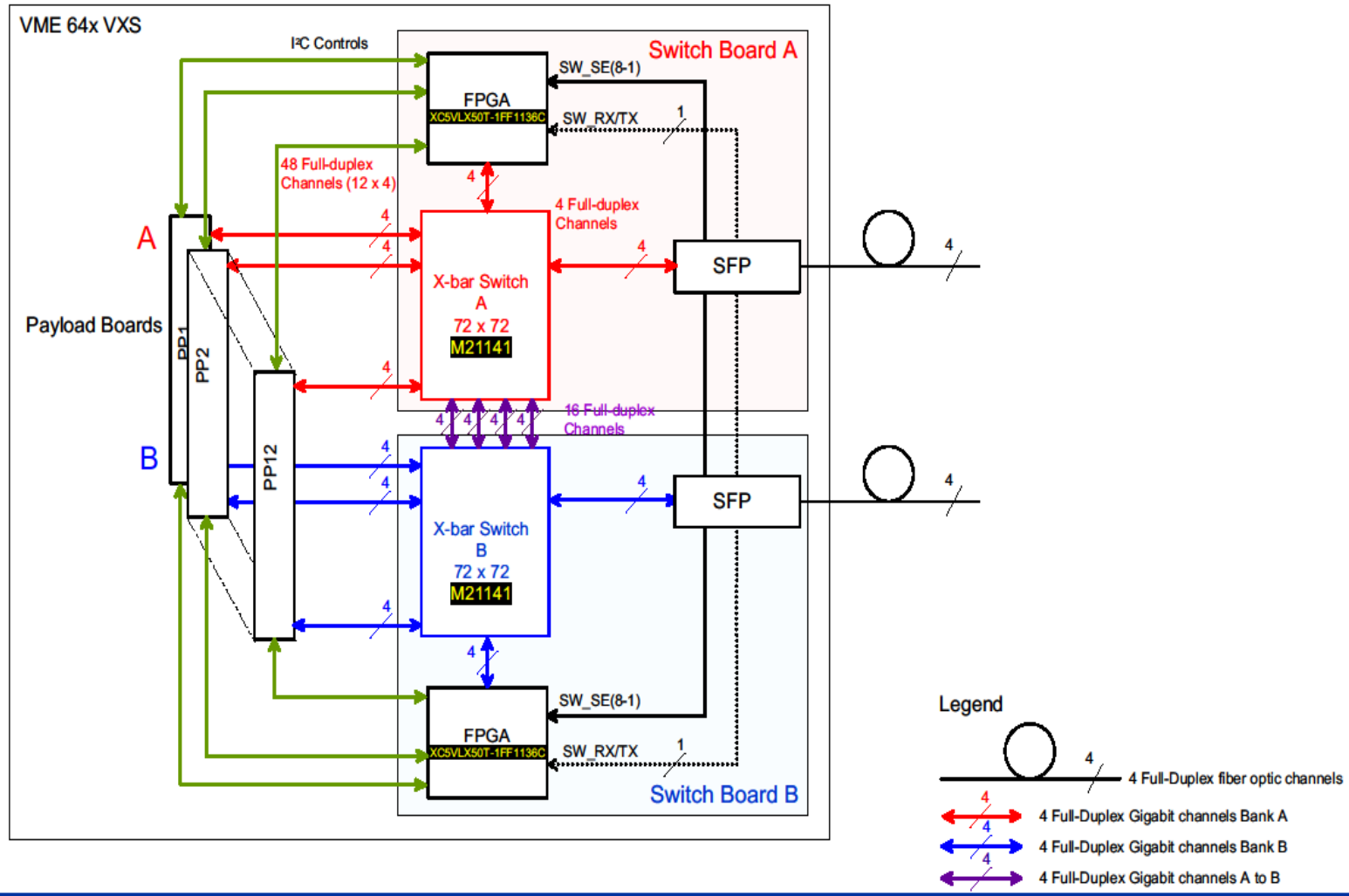
- Intra- and Inter-module communications
- DSP, feedback/feedforward loops
- Diagnostics, management, CERN control system integration...

VXS-DSP-FMC carrier



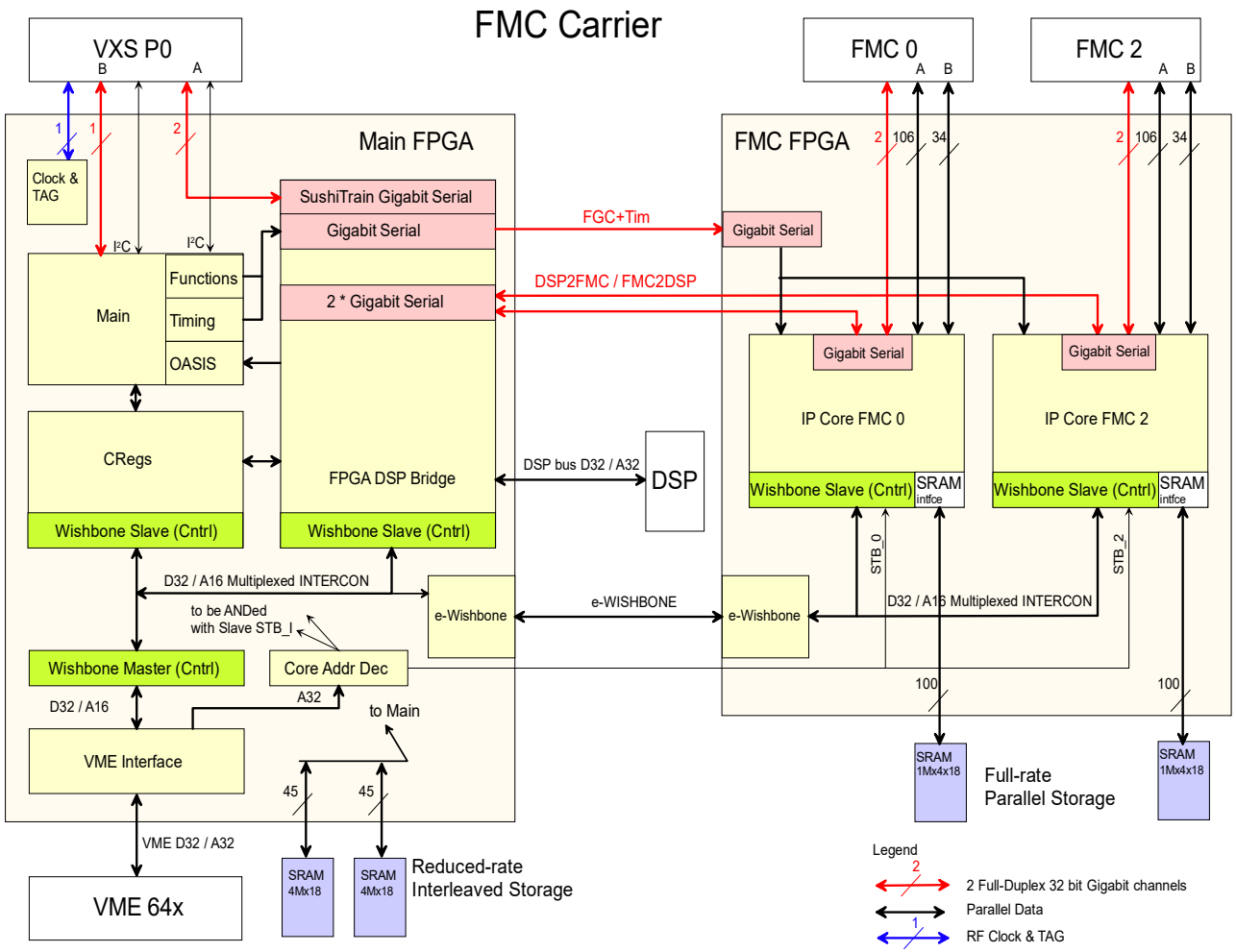


VXS switch


VME 64x VXS
I²C Controls
Switch Board A
FPGA
XC5VLX50T-1FF1136C
SW_SE(8-1)
SW_RX/TX
1
48 Full-duplex Channels (12 x 4)
4 Full-duplex Channels
A
Payload Boards
PP1
PP2
PP12
X-bar Switch A 72 x 72 M21141
SFP
16 Full-duplex Channels
B
X-bar Switch B 72 x 72 M21141
Switch Board B
Legend
4 Full-Duplex fiber optic channels
4 Full-Duplex Gigabit channels Bank A
4 Full-Duplex Gigabit channels Bank B
4 Full-Duplex Gigabit channels A to B


2.07
2.07

Firmware: Communications



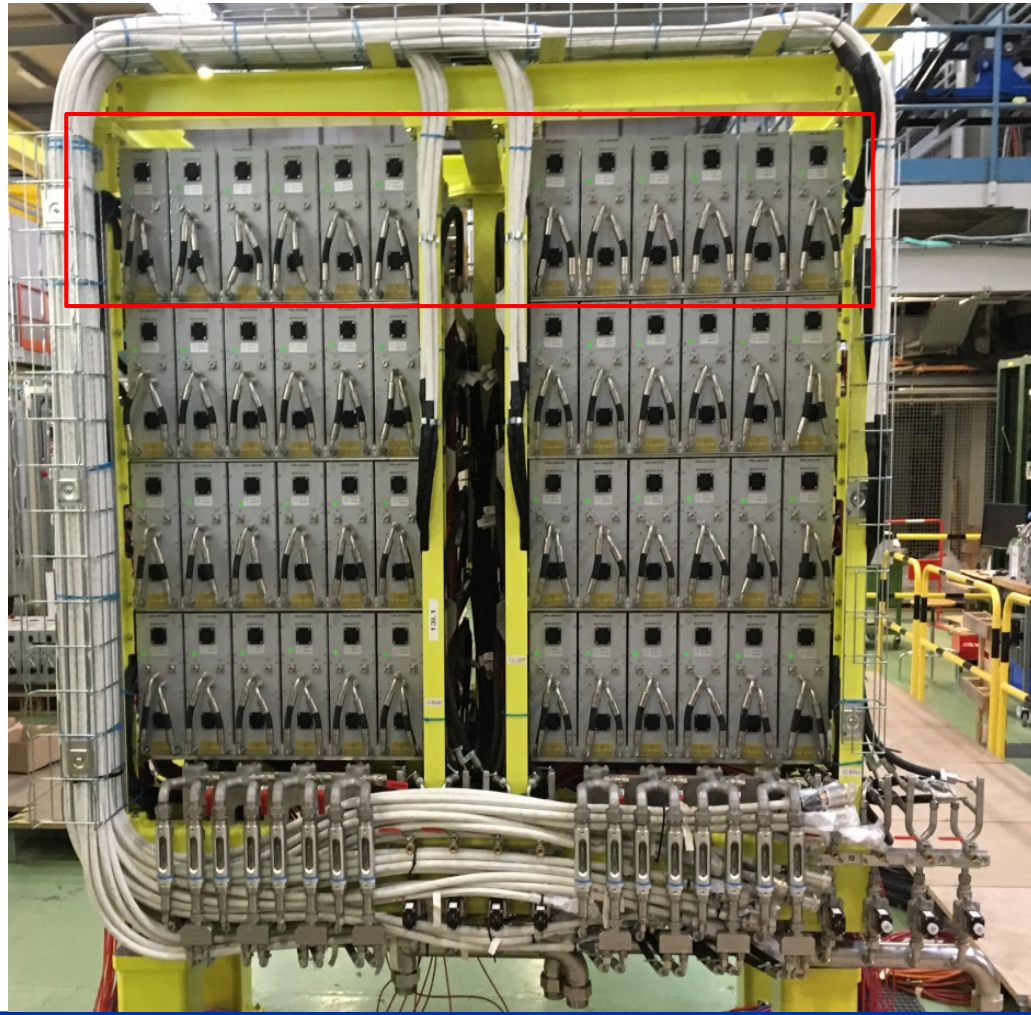
Proton Synchrotron Booster post LS2

Hardware configuration

- 4 rings → 3 sectors → 12 cells
- Per sector: up to 8 kV_{pk}
- Per ring: up to 24 kV_{pk}
- One cell redundancy

LLRF cavity controller

- 1 VXS-DSP-FMC carrier per sector/ring
- ADC + DAC FMCs

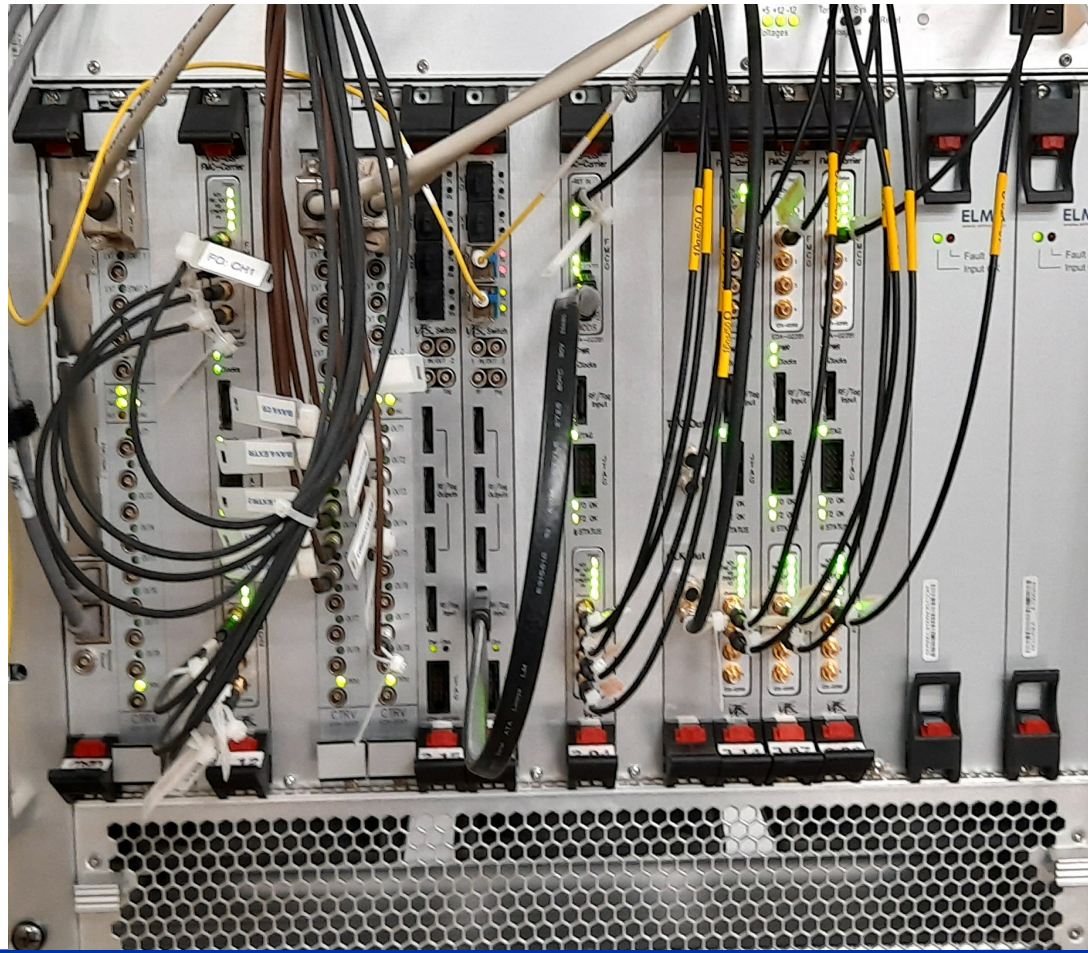


Proton Synchrotron Booster post LS2

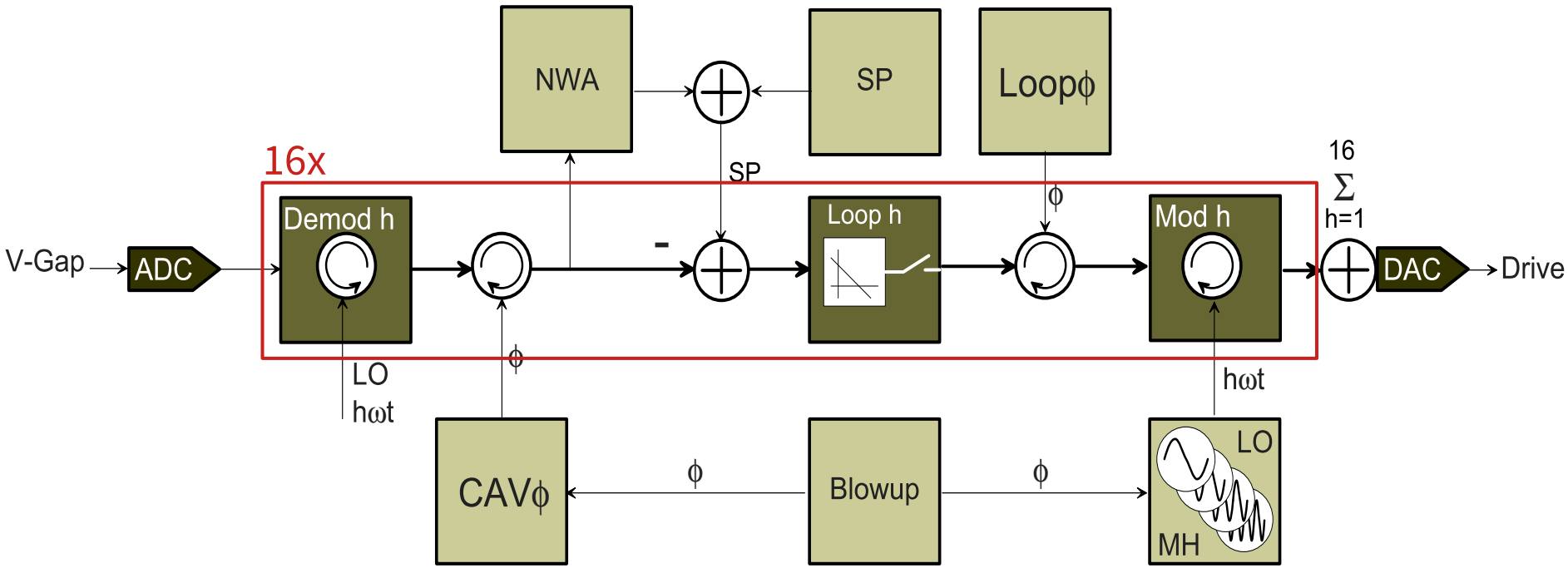
Proton Synchrotron Booster post LS2

LLRF system

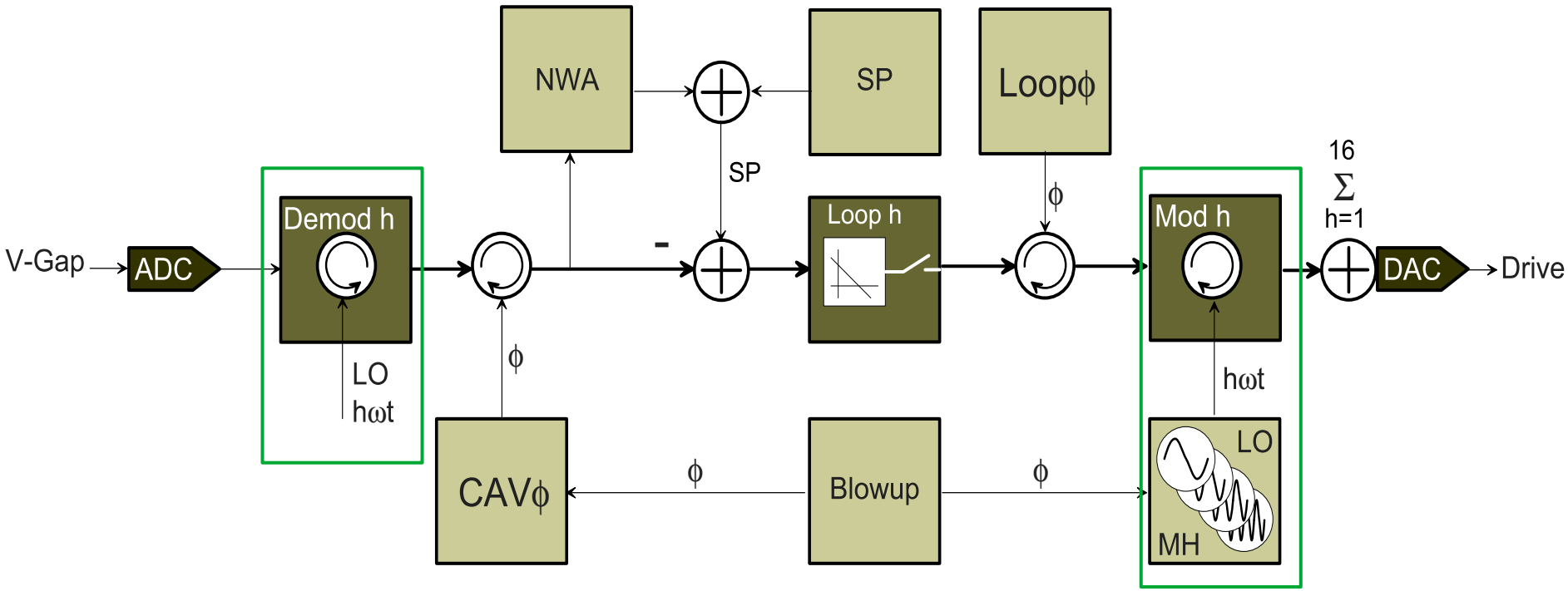
- 1 VXS-DSP-FMC carrier:
  - Radial loop, frequency program
- 1 VXS-DSP-FMC carrier:
  - Phase loop, synchro loop
- 3 VXS-DSP-FMC carrier:
  - Cavity controllers (1 per sector)
- Timings, diagnostics...



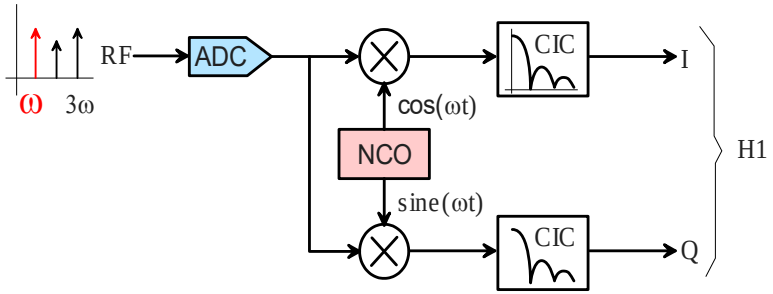
Multi-harmonic cavity controller



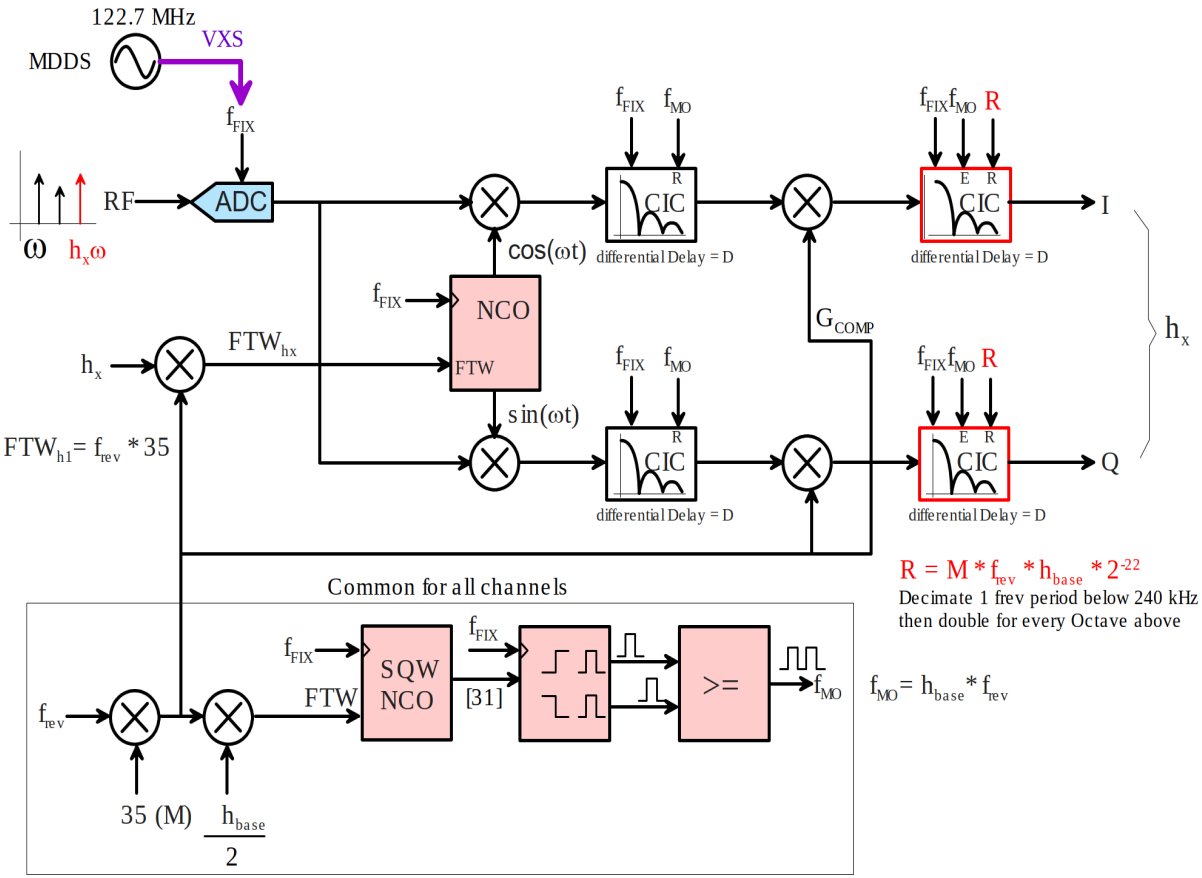
Multi-harmonic cavity controller



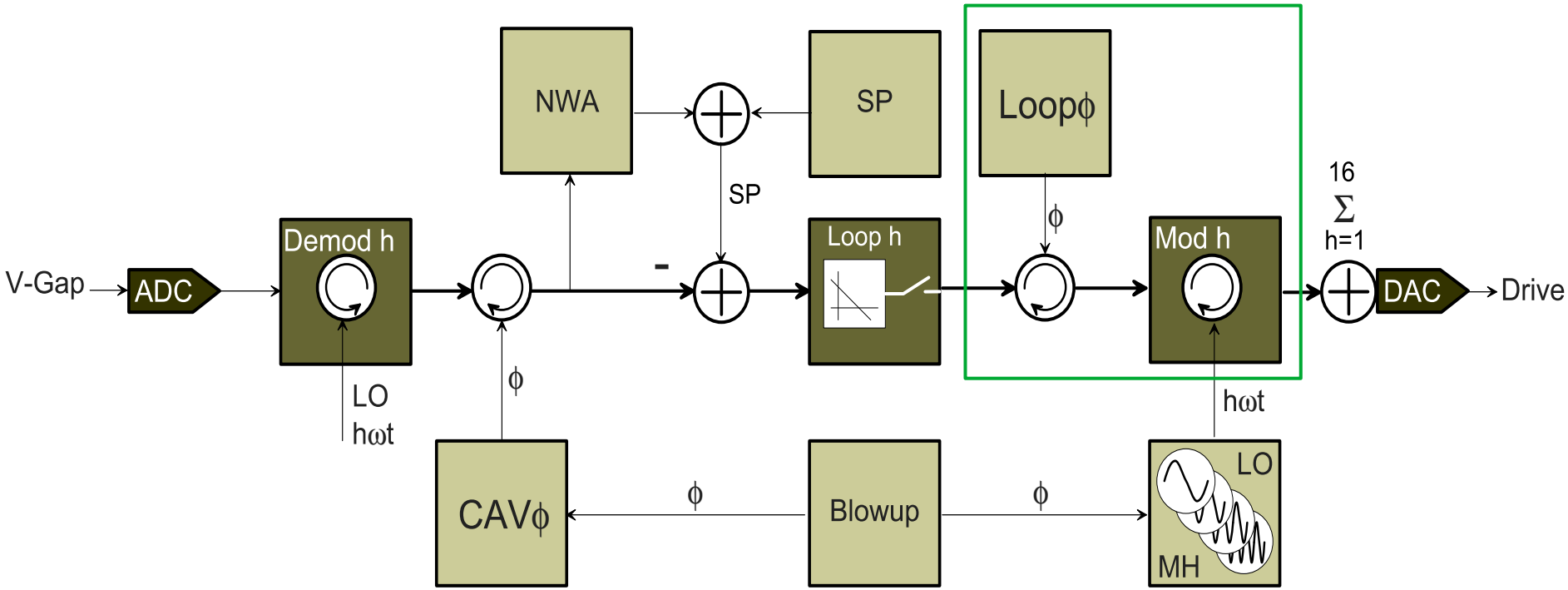
Fixed frequency clock: demodulator



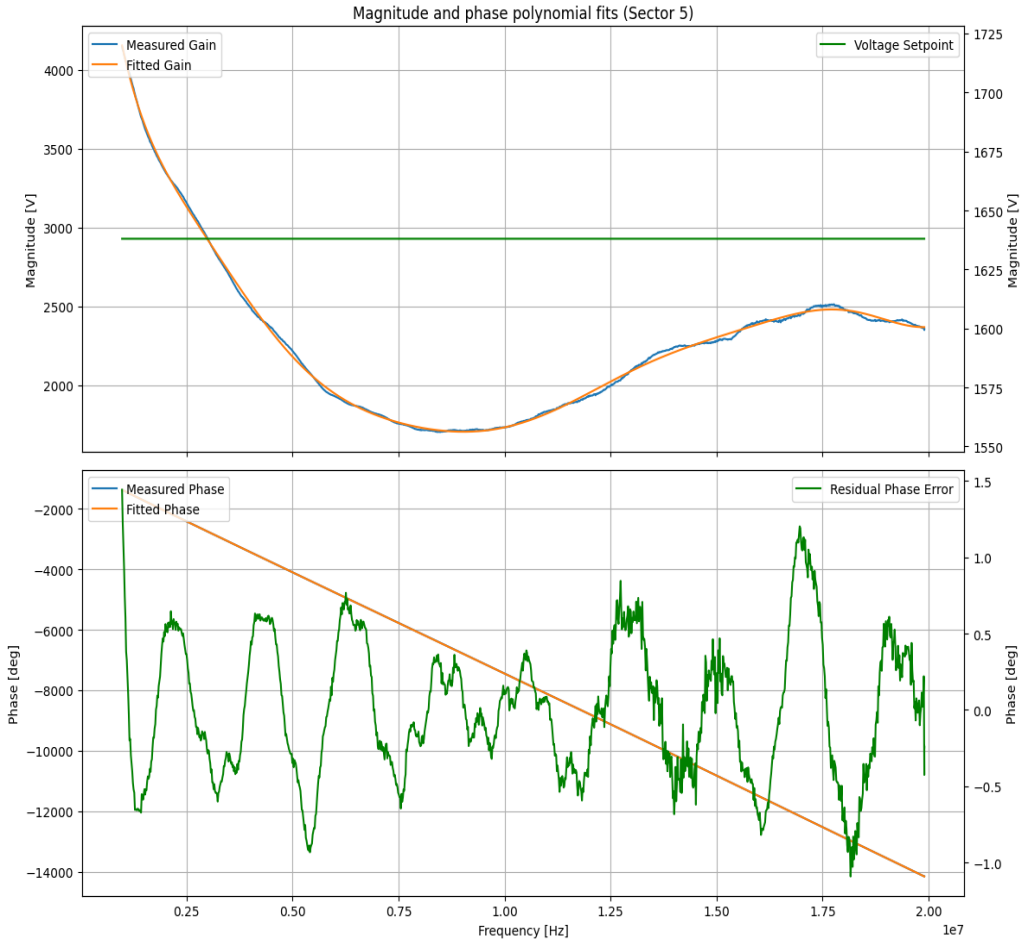
- No need of complex DDS schemes
- ADC/DACs at optimum frequency
- Clock, synchronization and FTW distribution over backplane

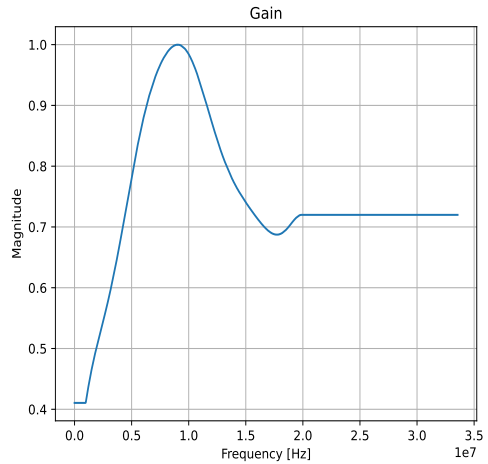


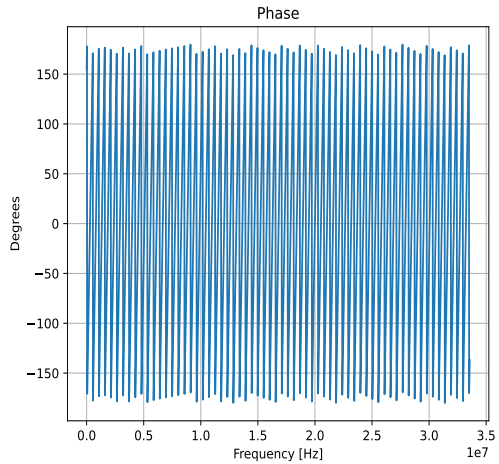
Multi-harmonic cavity controller

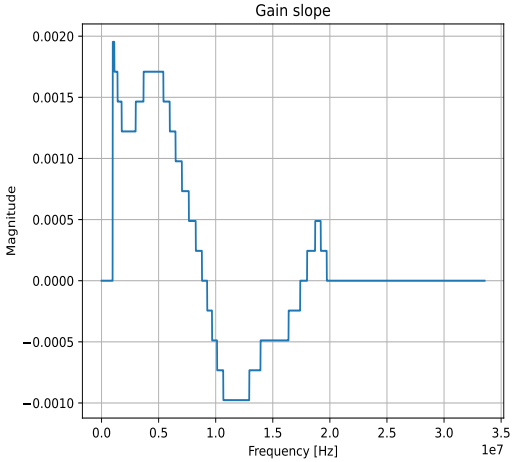


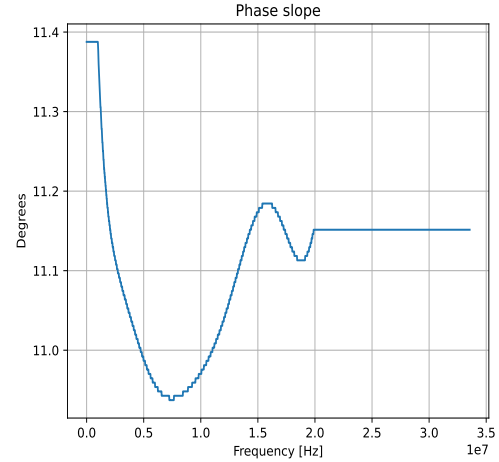
Feed-forward compensation



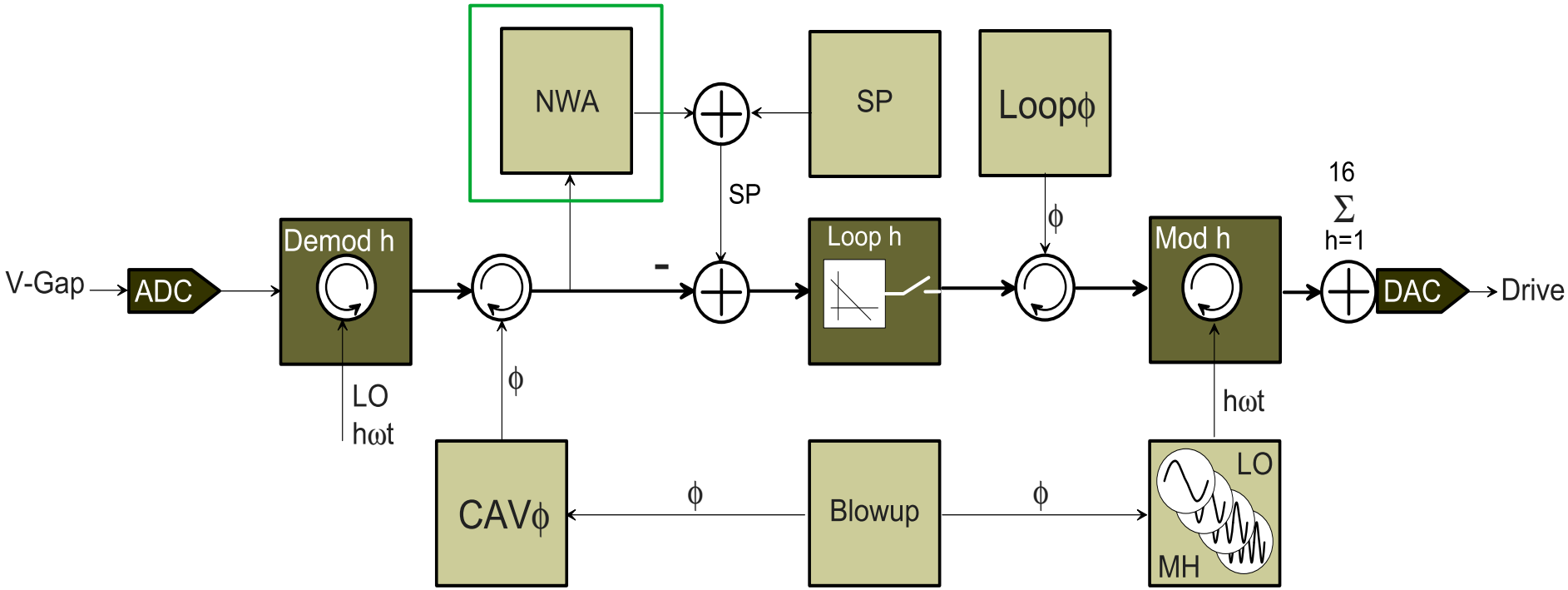




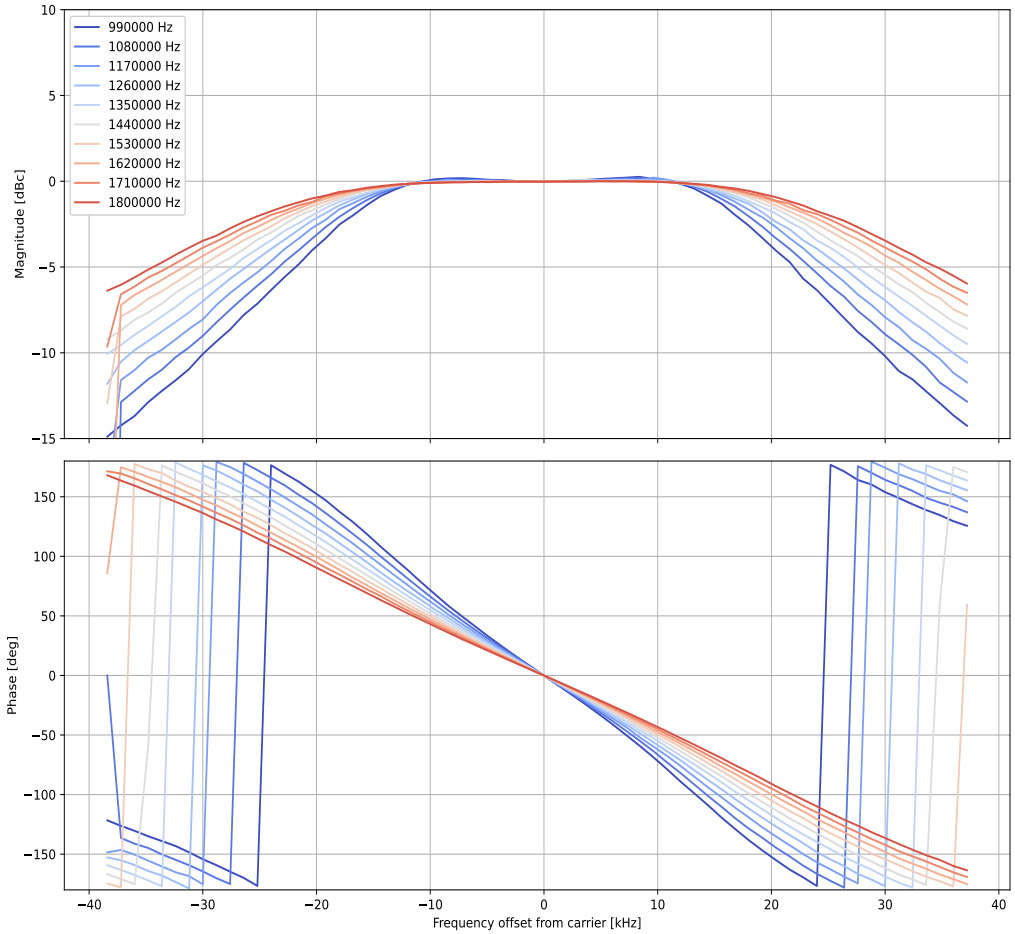


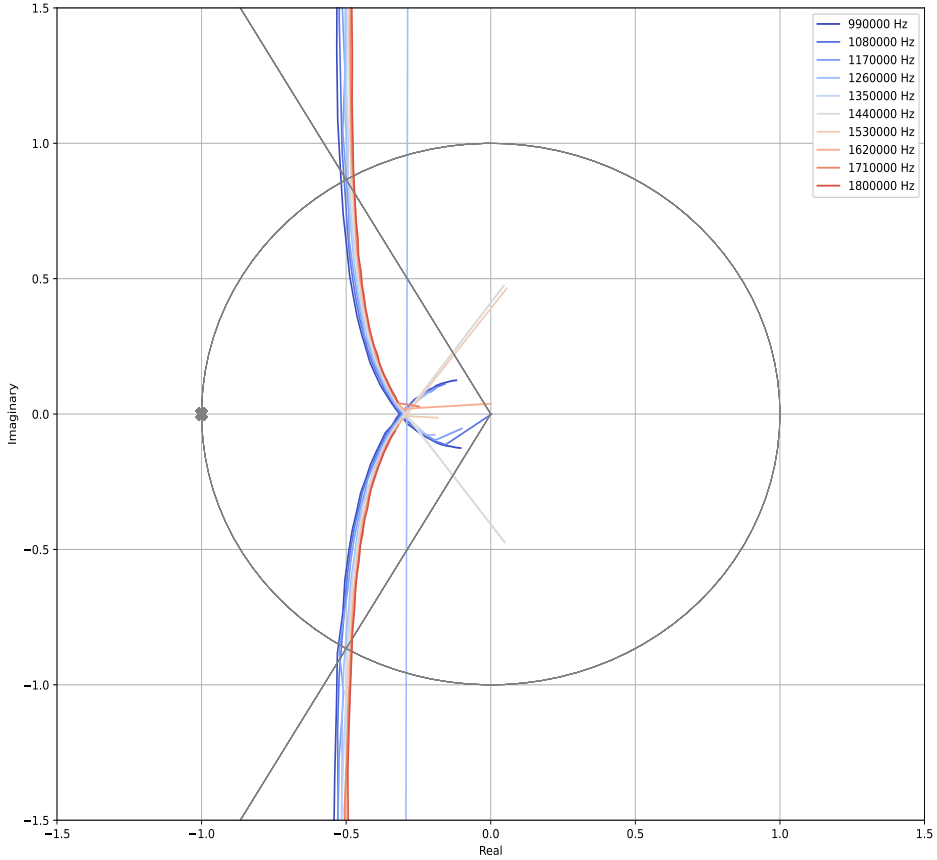


Multi-harmonic cavity controller

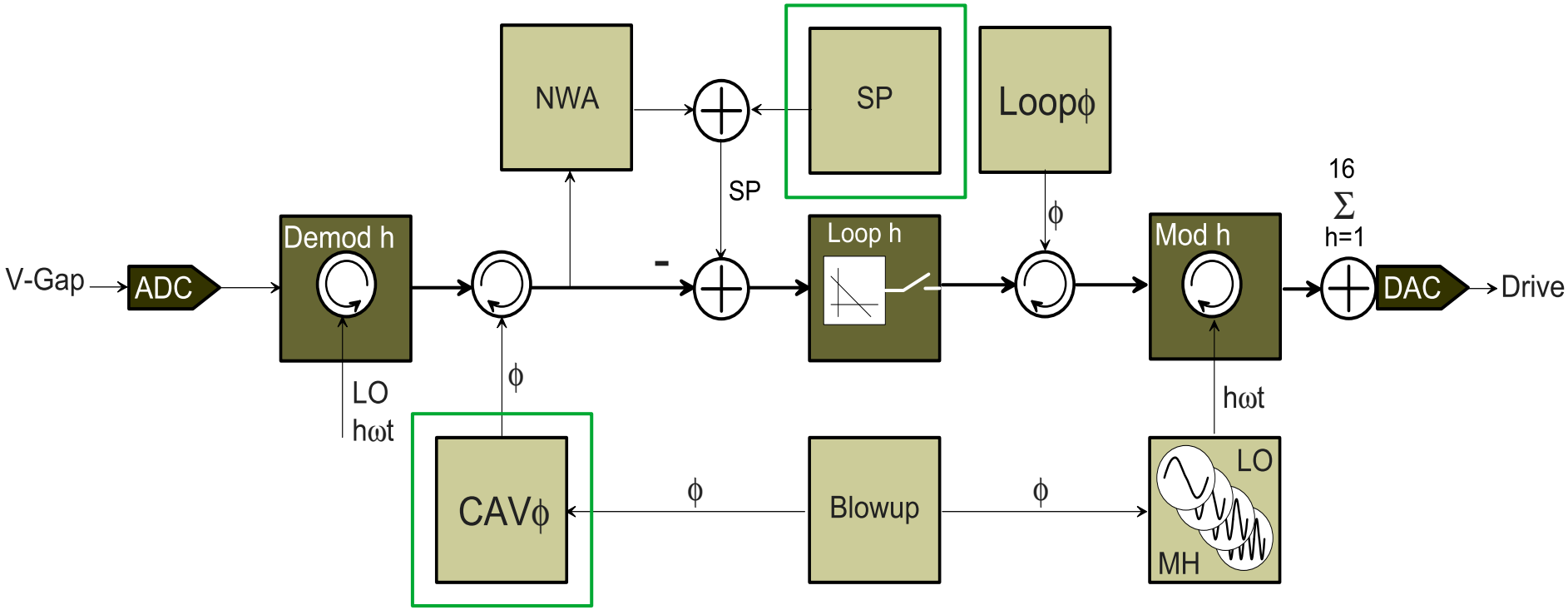


Embedded network analyzer

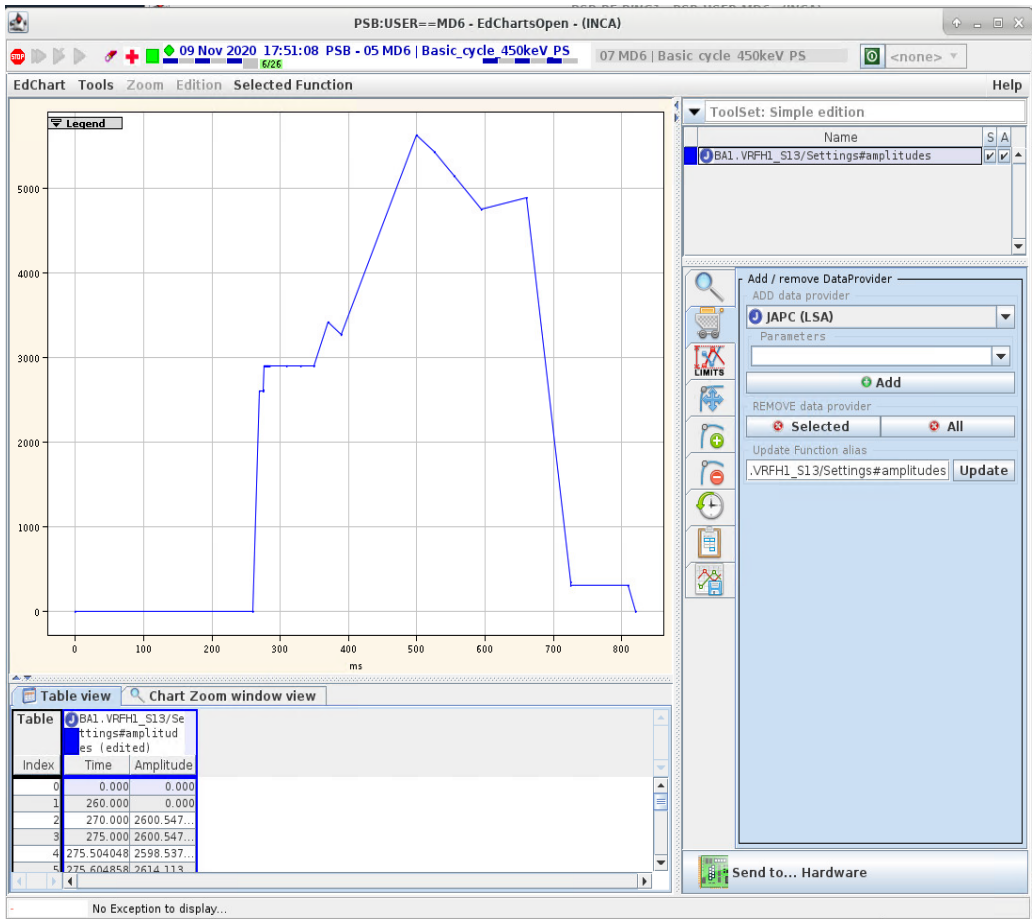


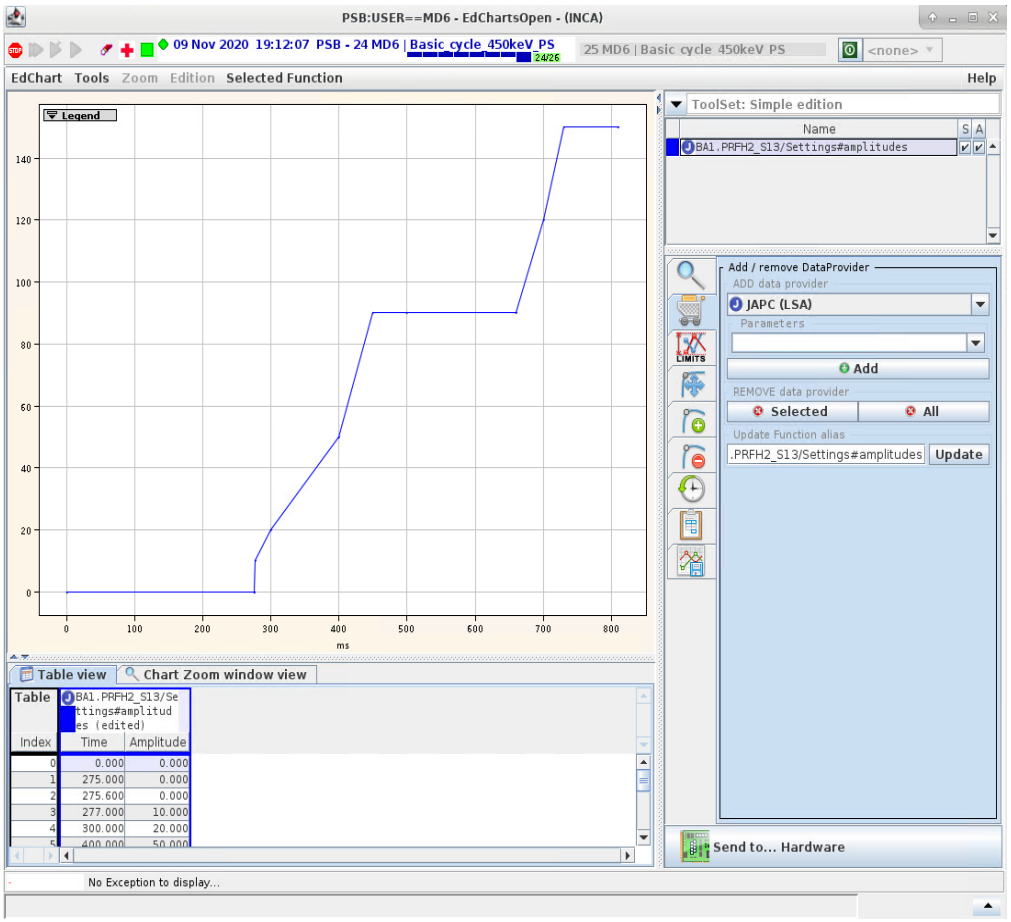


Multi-harmonic cavity controller

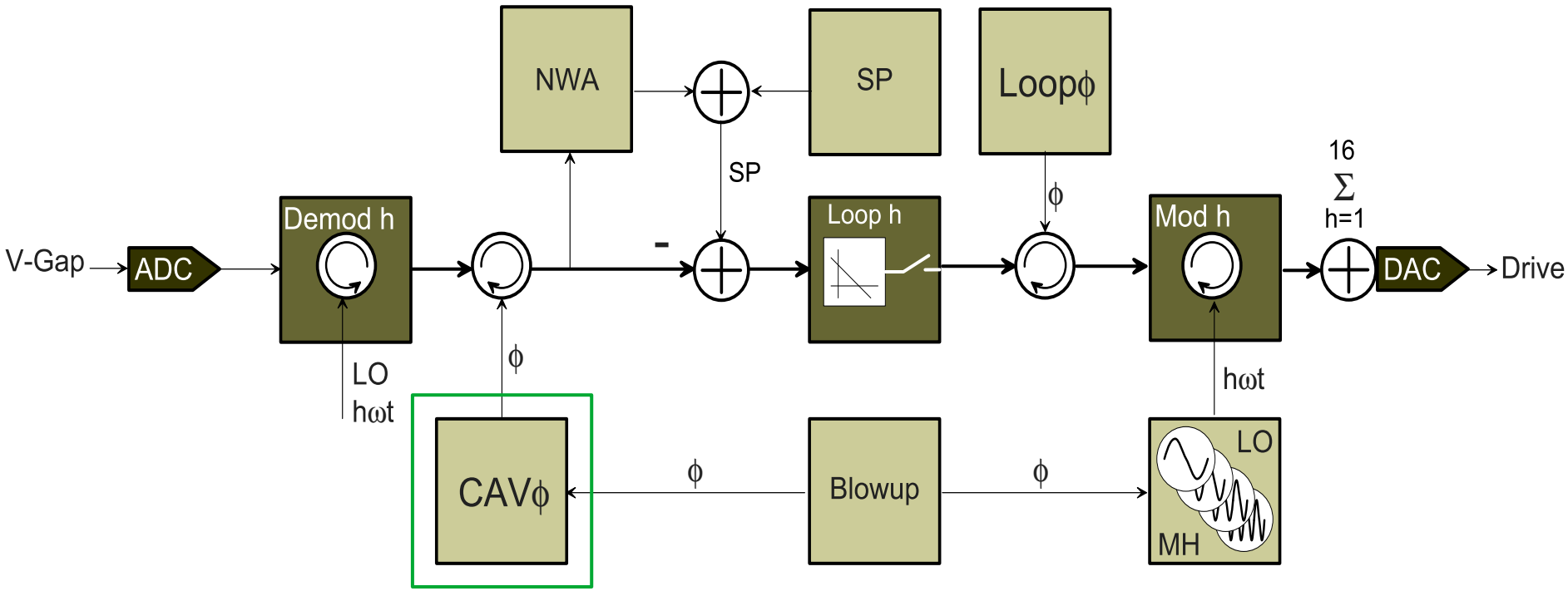


Voltage/phase setpoint for each harmonic

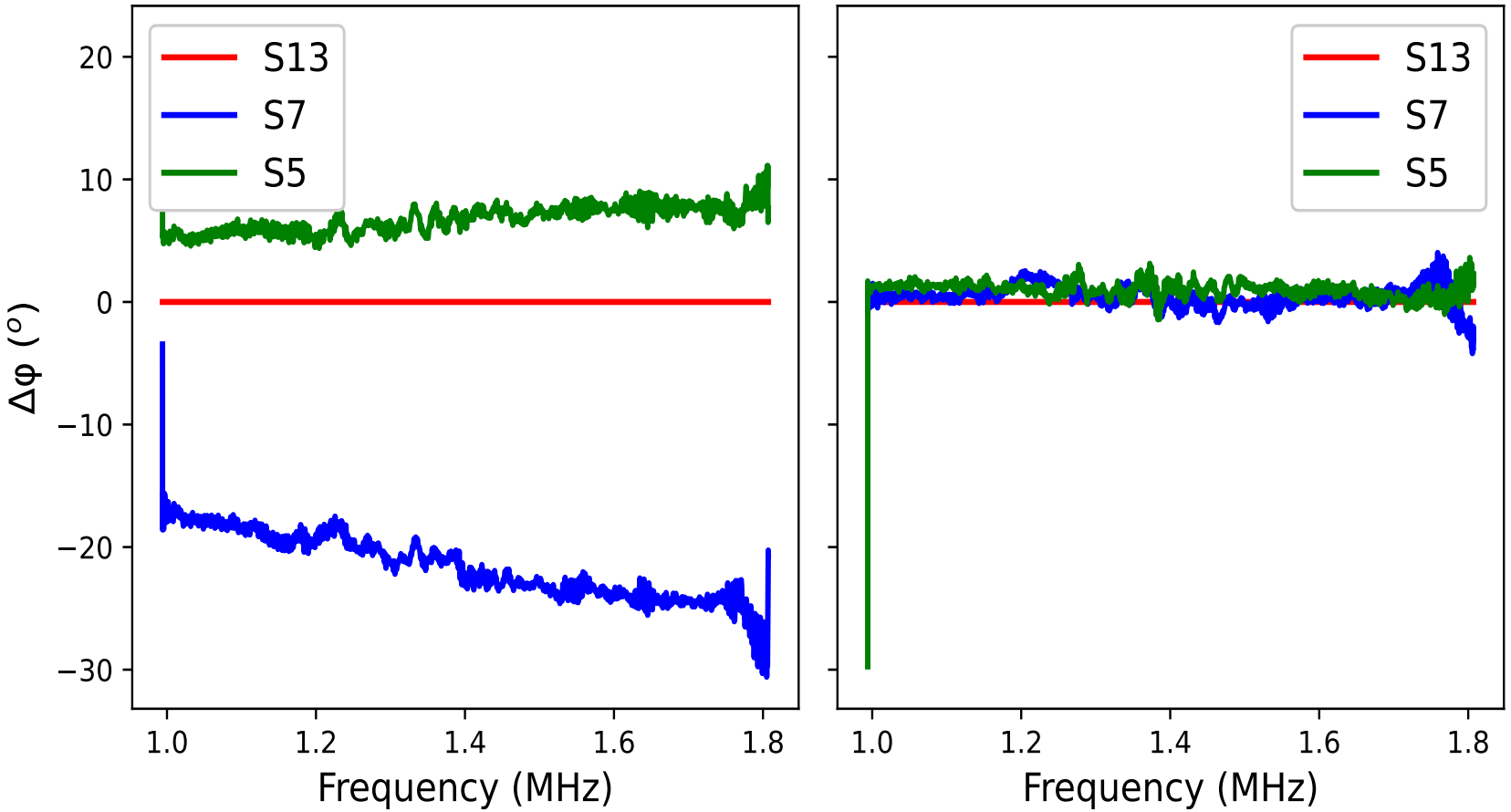




Multi-harmonic cavity controller

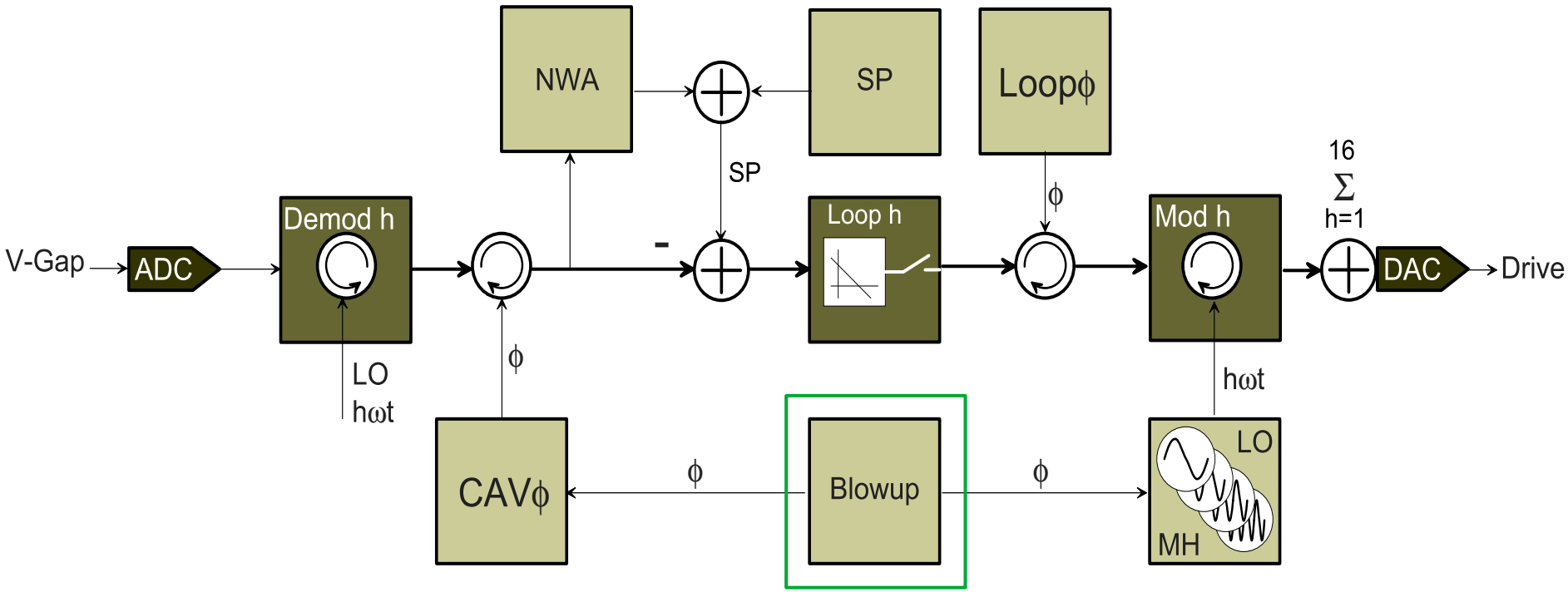


Sectors alignment

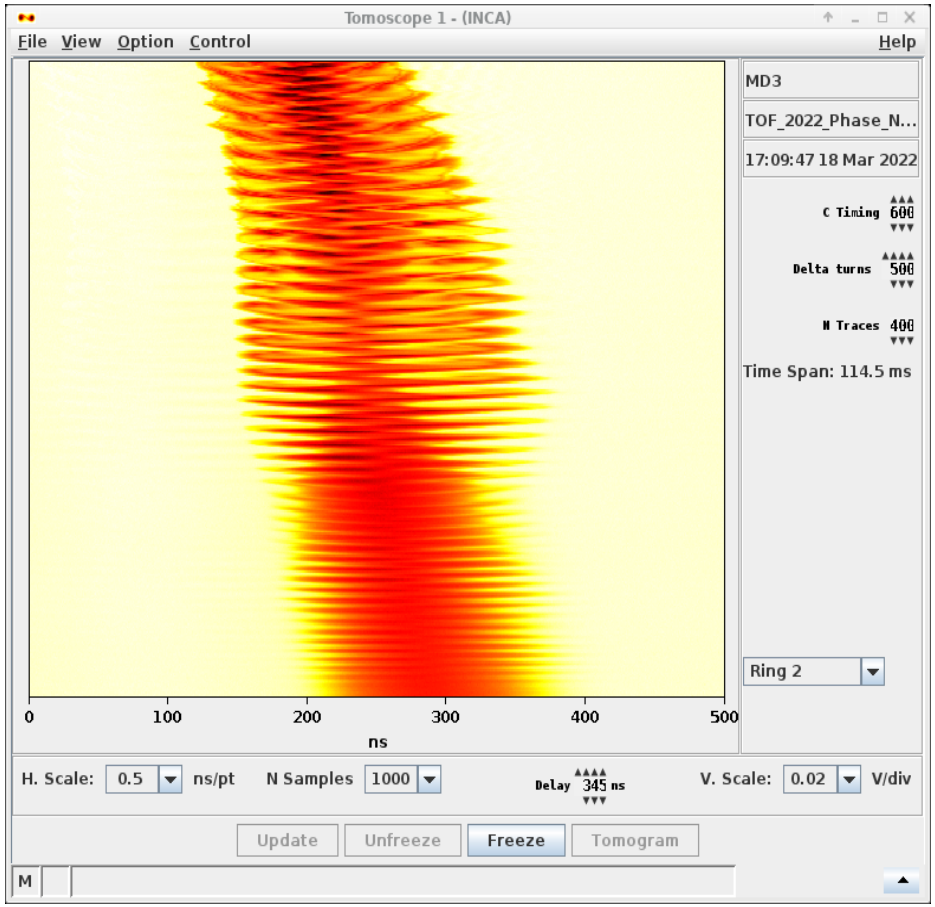


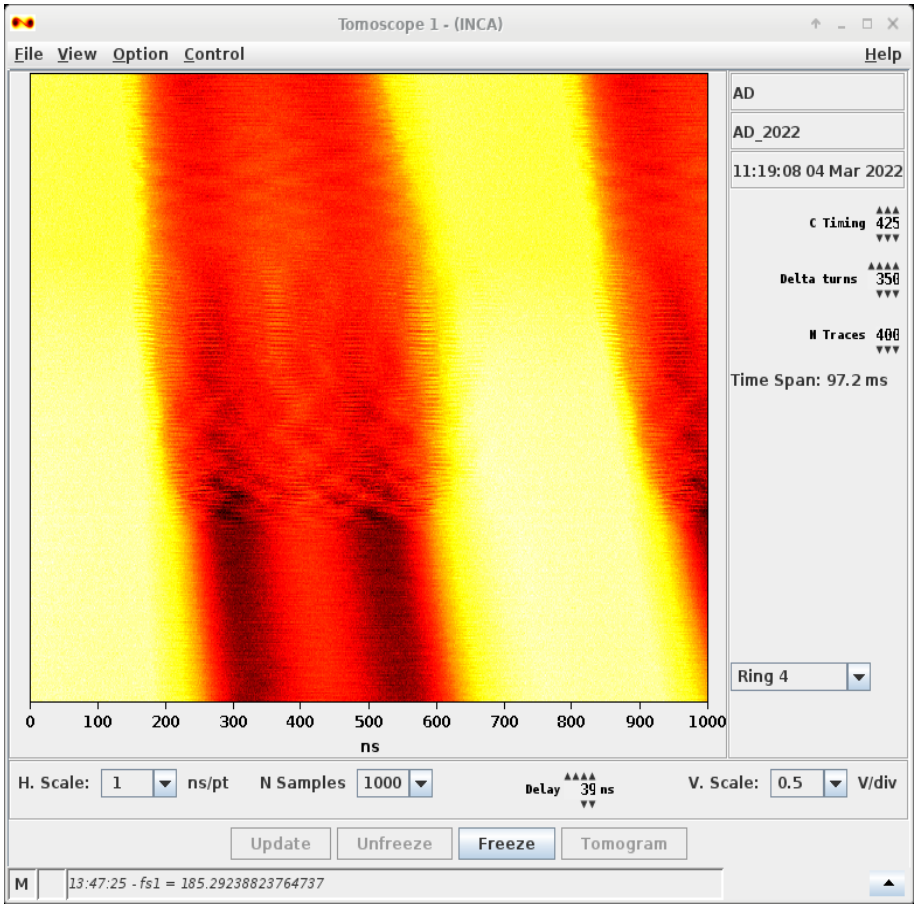
Induced voltage

Multi-harmonic cavity controller

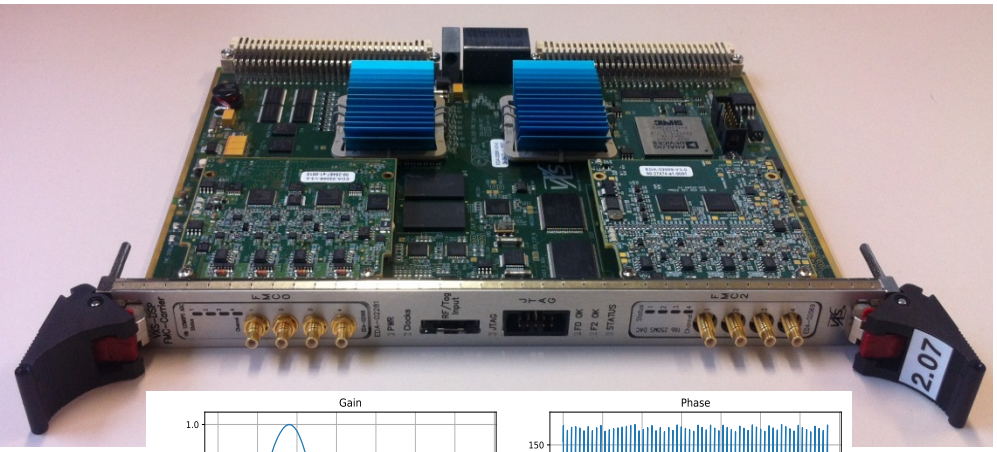


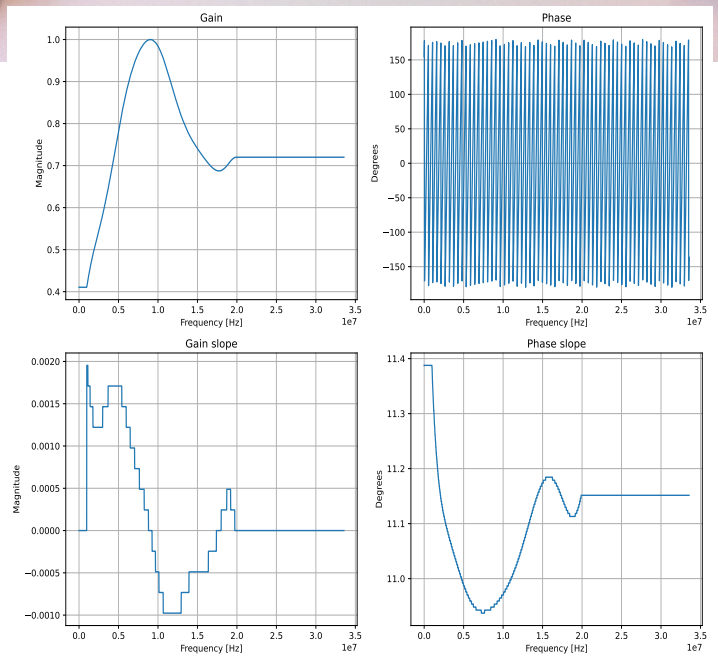
Longitudinal blowup: Phase noise / higher harmonic

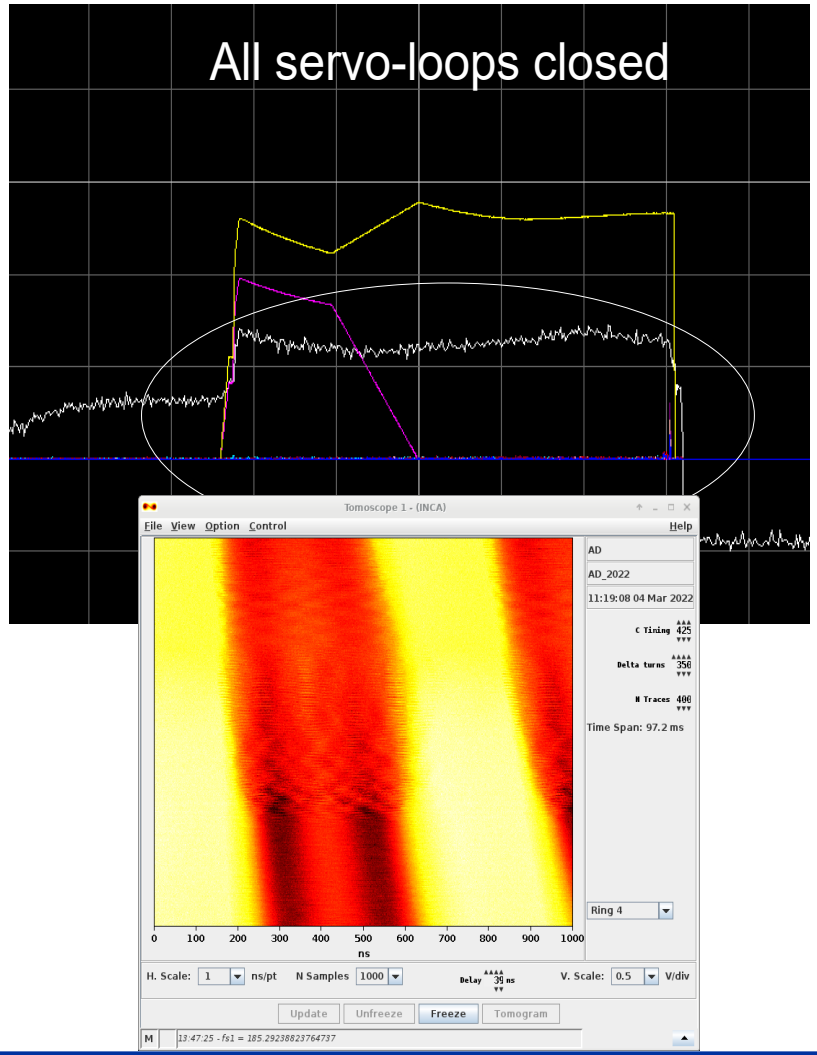




Multi-harmonic cavity controller in FPGA







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