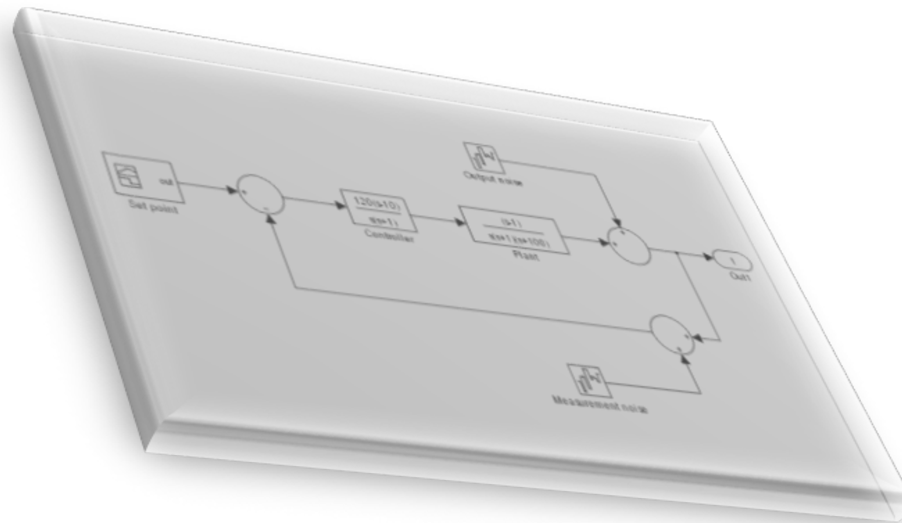
Operational Experience of the SELAP Algorithm for LLRF Control at JLAB



Rama Bachimanchi – Jefferson Lab , Newport News, VA

On behalf of LLRF Group at JLAB

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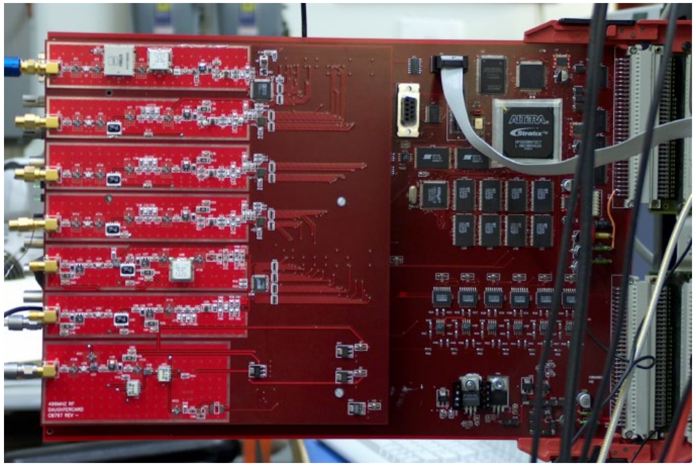
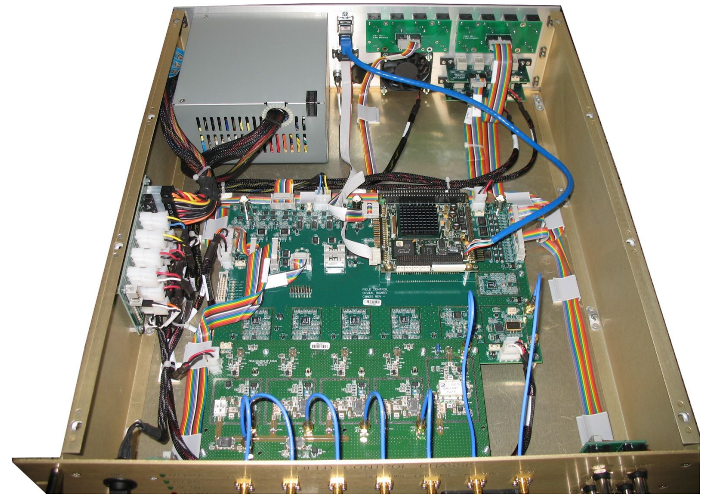
RF Team

- LLRF Team
  - Curt Hovater
  - Rama Bachimanchi
  - Tomasz Plawski
  - James Latshaw
  - Dave Seidman (coordinator)
  - Clyde Mounts (operations)
- Controls/Software
  - Jianxun Yan (ORNL)
  - Scott Higgins
  - Kyle Hesse
- Many more

Where We Have Been …Digital

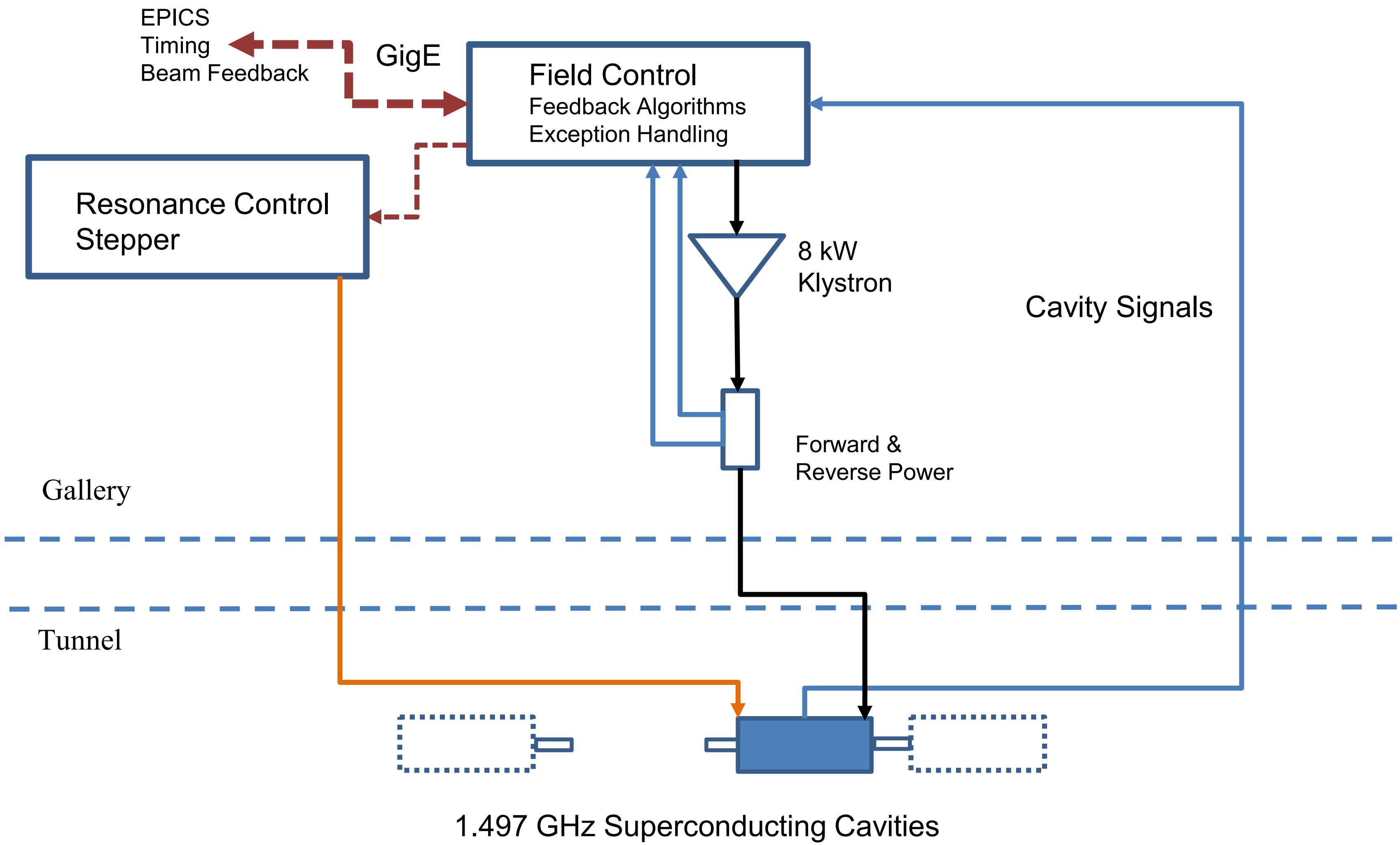


VXI Motherboard & 499 MHz Transceiver



C100 Field Control Chassis (LLRF 2.0)

LLRF 3.0



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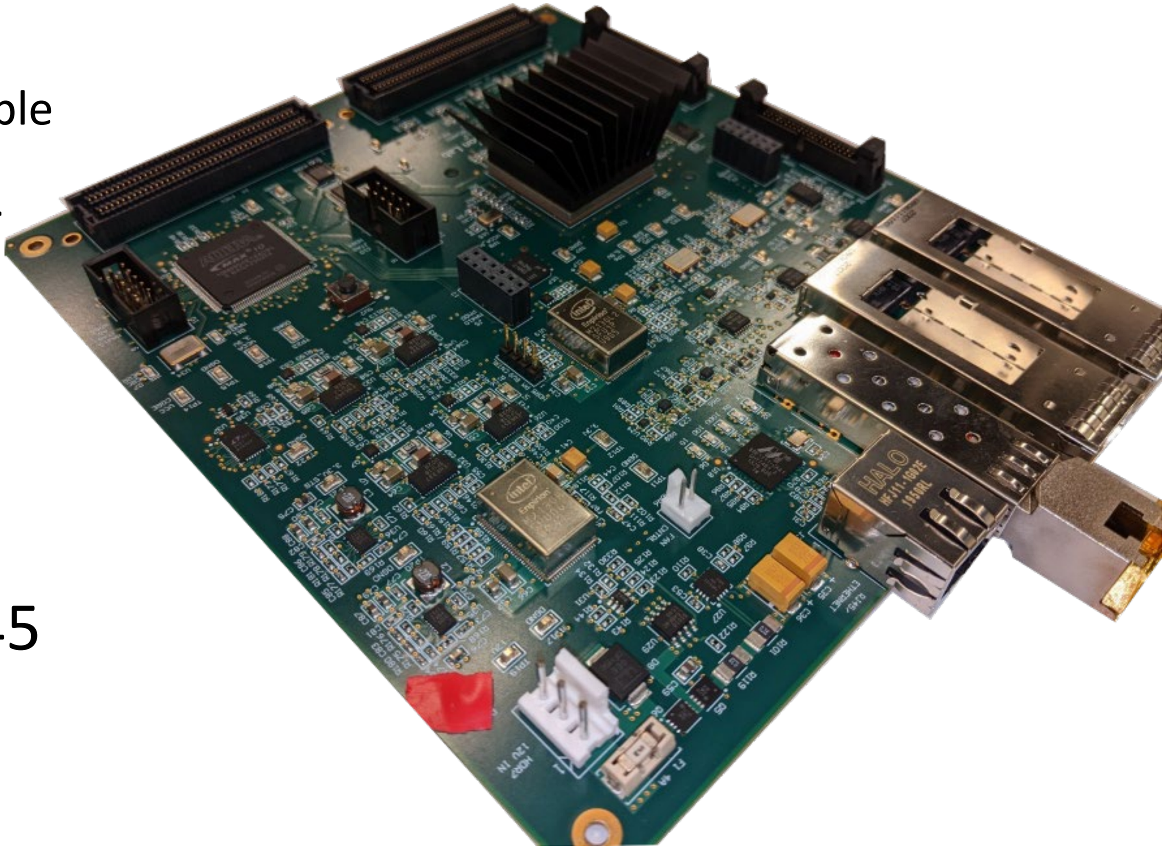
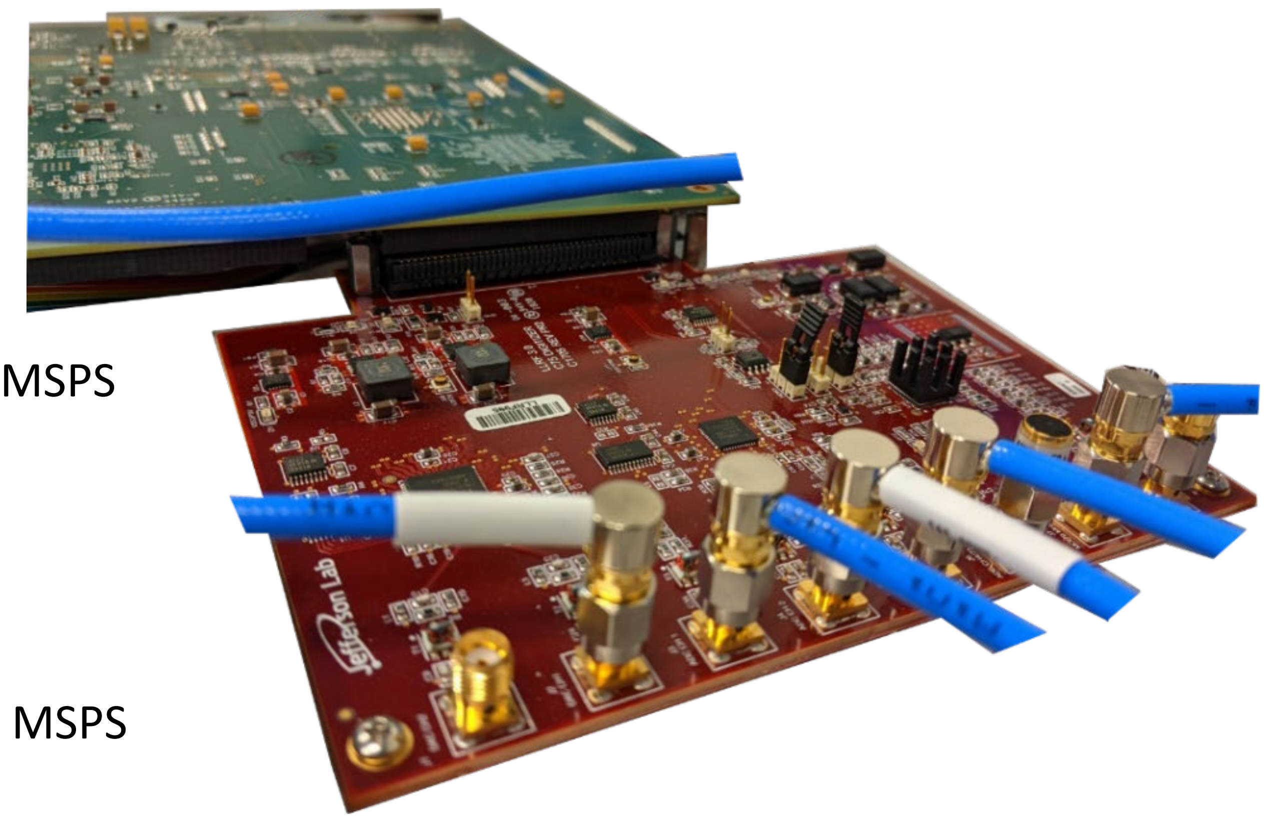
Cyclone 10GX FPGA Carrier

- Cyclone 10GX
  - 10CX105YF672
  - 152,000 FF (pin compatible with 220k FF/320k FF)
  - 10x12.5Gbps transceiver
- MAX10 FPGA
  - Power management
- Dual LPC FMC
  - LPC – 34 LVDS pairs
- 2xQSFP, 1xSFP, 1xRJ-45
- GPIO headers
  - 2x40 pin (20 signals)



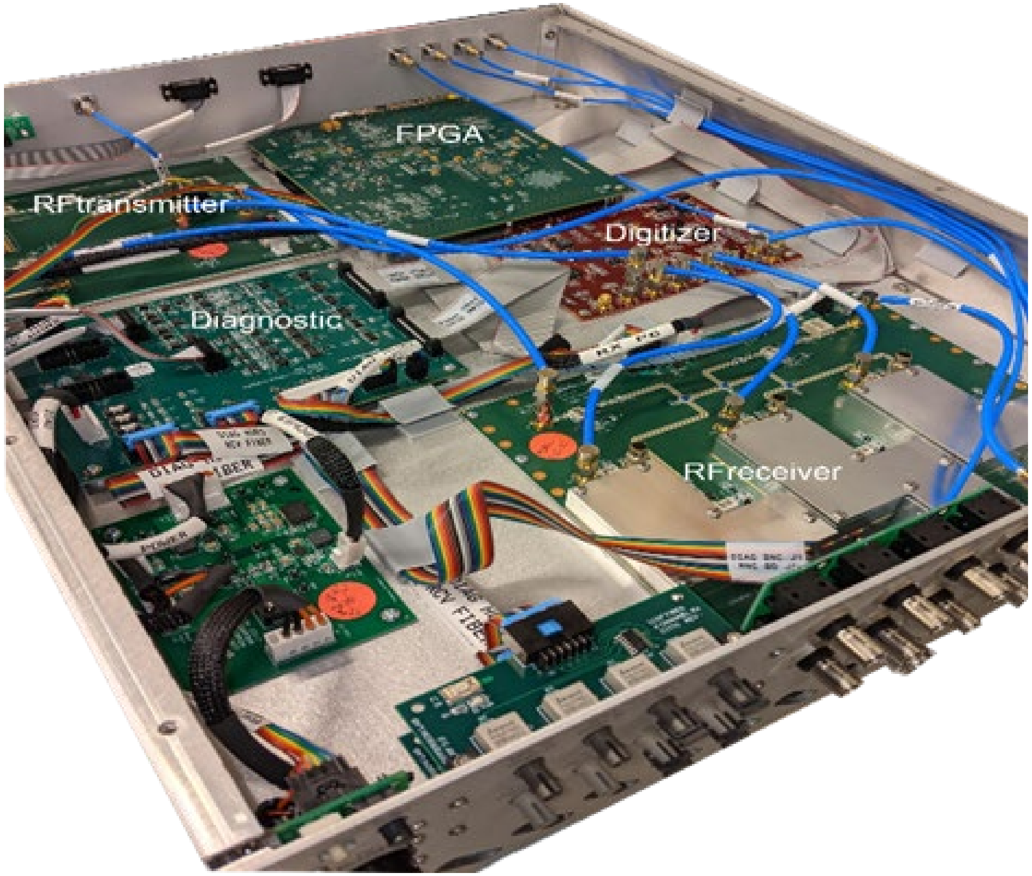
Digitizer

- Based on LCLS-II
- Single LPC FMC
- LMK03328
  - Dual PLL (VCO)
- AD9653
  - 16-bit, 4 channel 125MSPS ADC
  - IF – 70 MHz
  - ADC clock – 93 MHz
- AD9781
  - 14-bit, 2 channel 500 MSPS DAC
  - IF - 70 MHz
  - DAC clock – 186 MHz

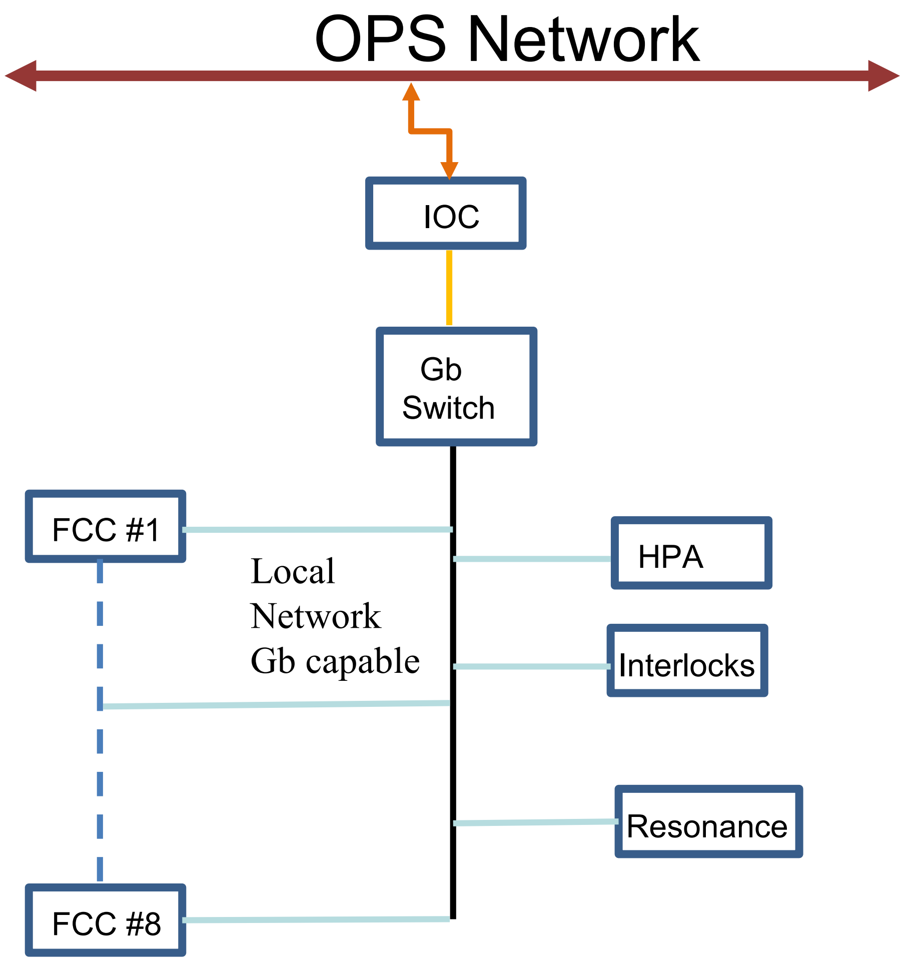


LLRF 3.0

- Cyclone 10GX FPGA carrier
- Modular design
- UDP Ethernet interface (1 Gbps)
- RF Downconverter
  - ~80 dB isolation
- One IOC per CM (8 cavities)
  - 8 Field Control
  - 1 HPA controller
  - 1 Interlocks control
  - 1 Resonance control(stepper)
  - All use the same FPGA board



Network Architecture

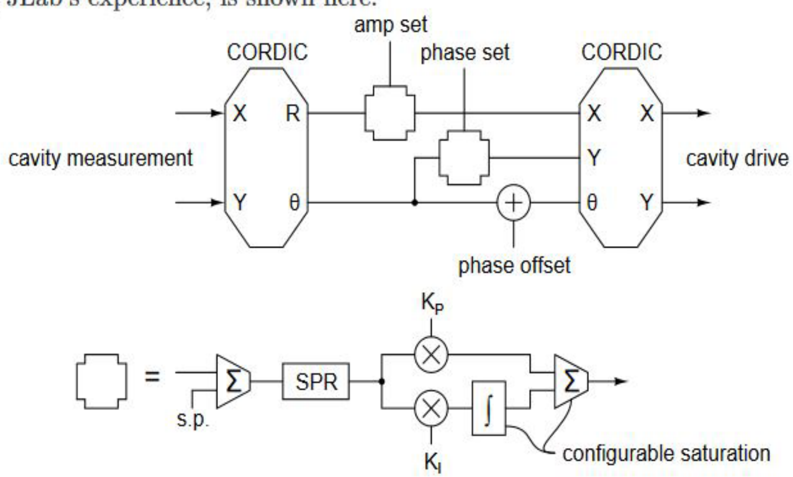


SEL and SELAP

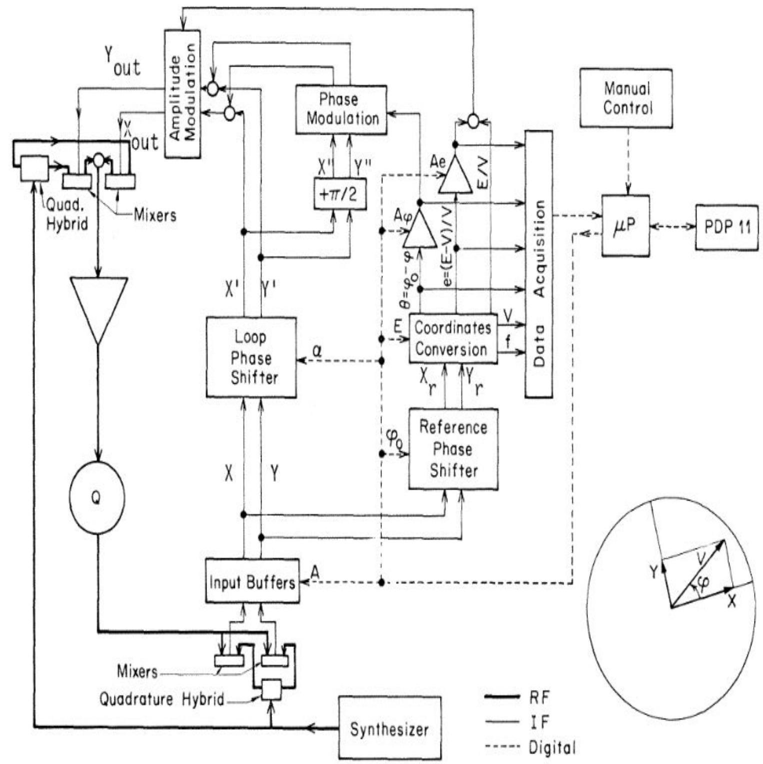
SEL'78 and digital SELAP today

- 1978 J. Delayen, PhD thesis - locked analog SEL concept
- 2012 Digital SEL, US Patent for JLAB LLRF team
- 2014 L. Doolittle

The important features of an SEL data path were clearly laid out in 1978, although using analog terminology. A modern rendition of the block diagram in the digital domain, loosely following JLab's experience, is shown here:



Where SPR stands for stateful phase resolver, and it is only used in the phase channel.



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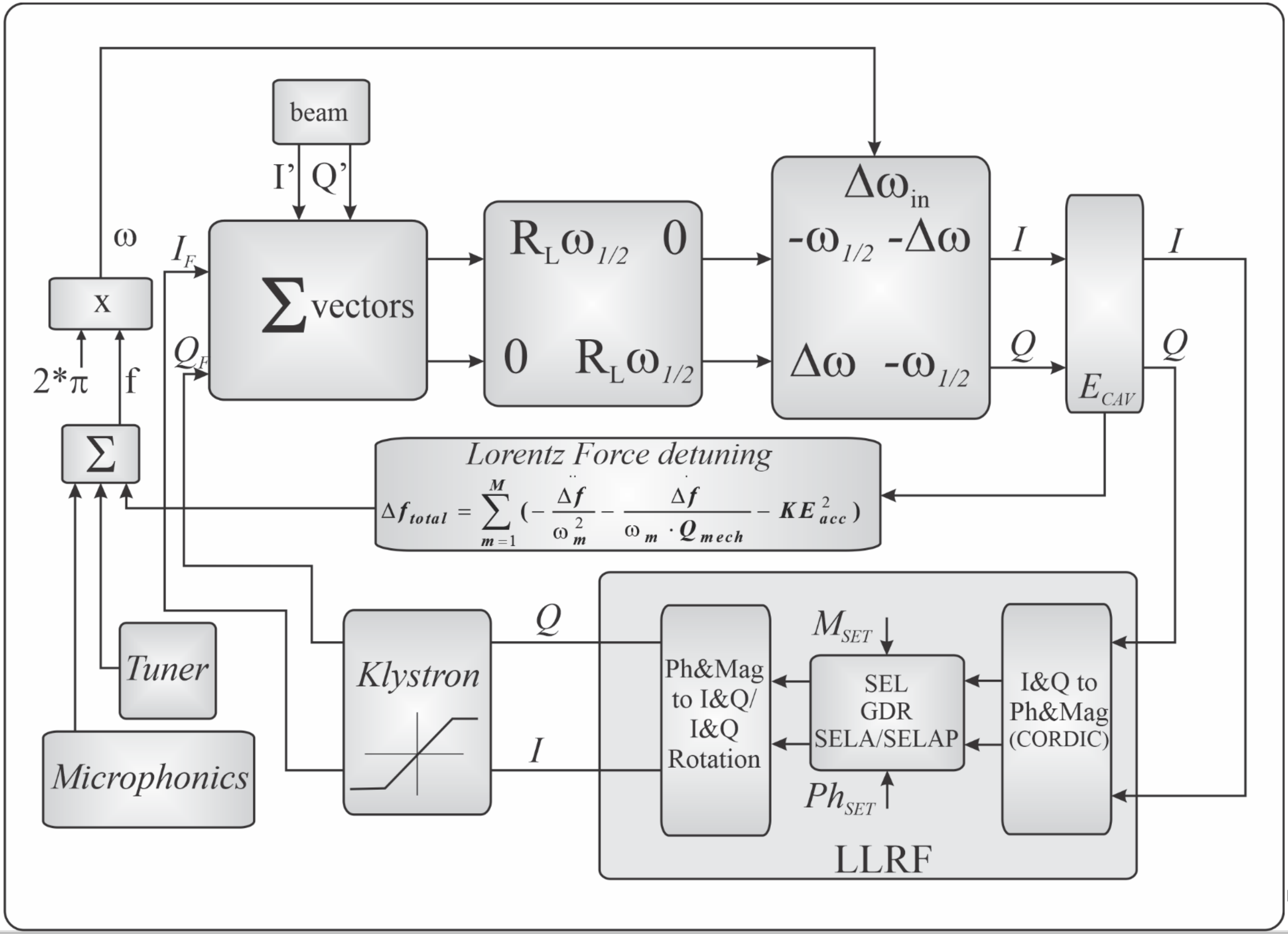
SELAP Algorithm Test on UITF



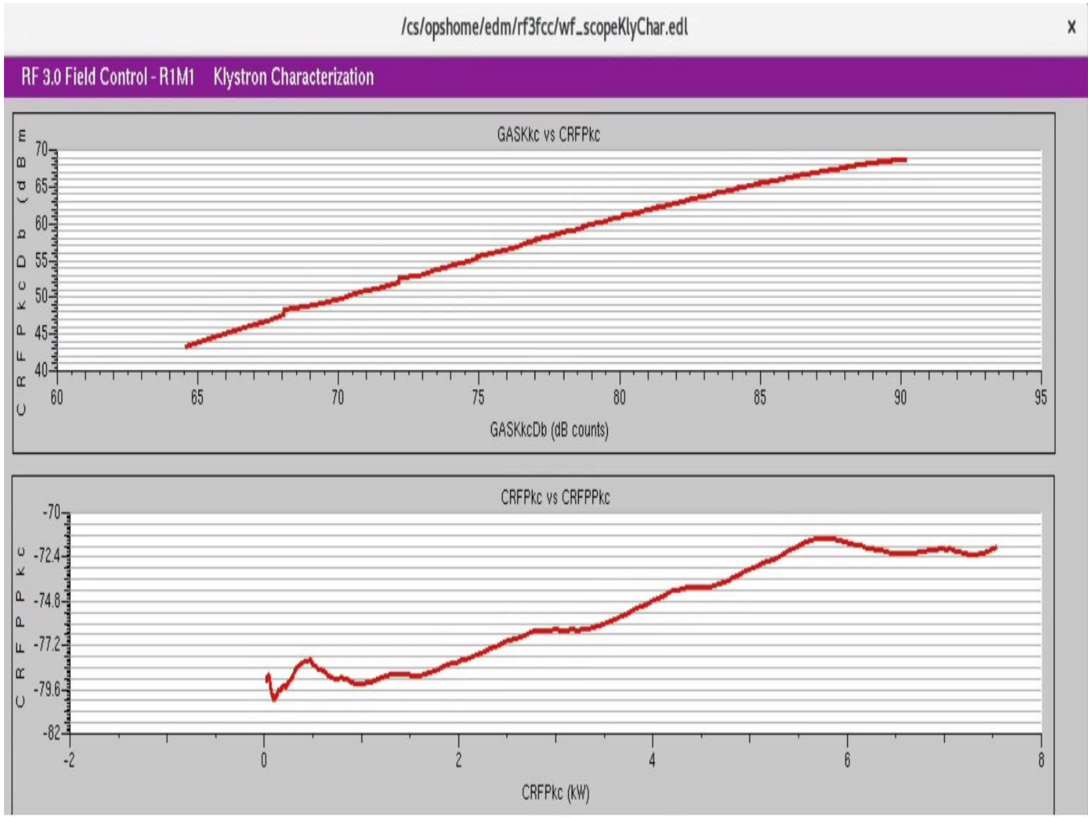
nd

SELAP Algorithm Test on UITF

- SEL (self excited loop)
  - Amplitude is not regulated
- SELA
  - Amplitude is regulated
- GDR
  - Amplitude and phase are regulated
- SELAP
  - Amplitude is regulated
  - GDR alike, if detuning is within the power limits
  - Phase spins at residual frequency if detuning is outside the power limits

Klystron Characterization

- Ramps the klystron input to max drive in 200 us
- Cavity sees little to no gradient
- Measures the klystron response to input (DAC drive from FPGA)
- Phase response
- Max power



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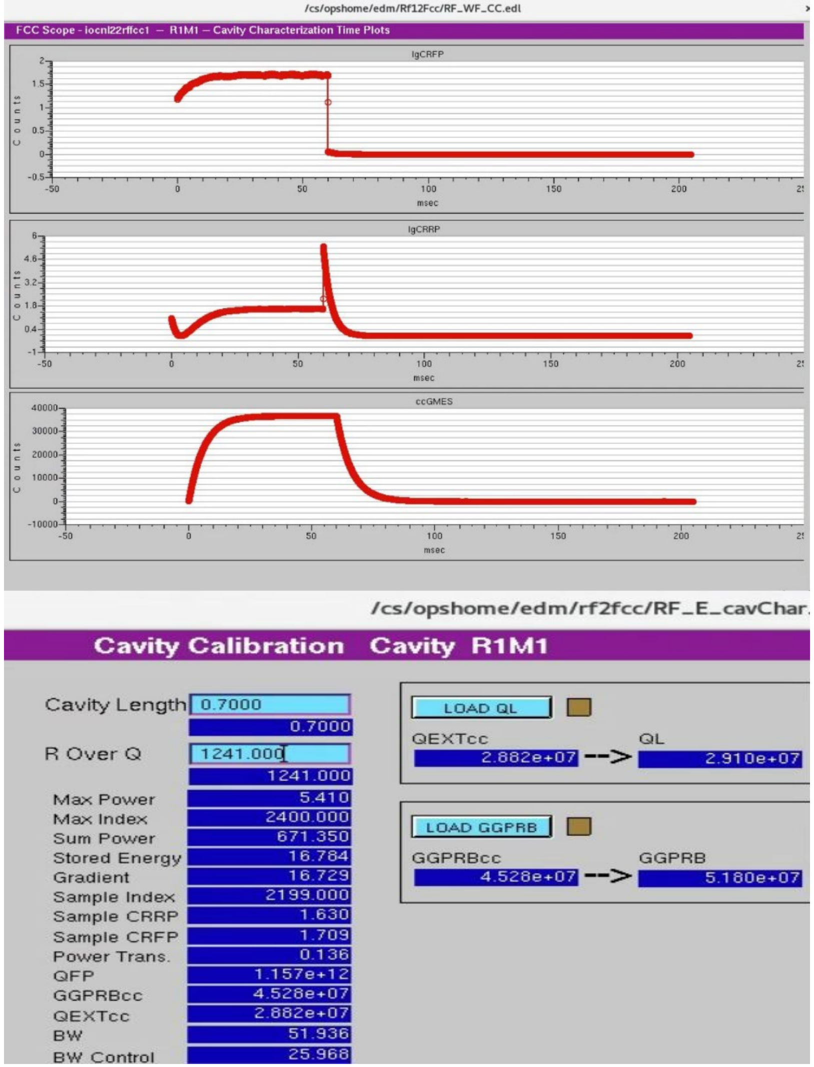
Cavity Characterization

- Cavity in pulse mode
- Stored energy
- Gradient (MV/m)
- Q_{ext}
- Bandwidth
- Q_{FP} (field probe Q)



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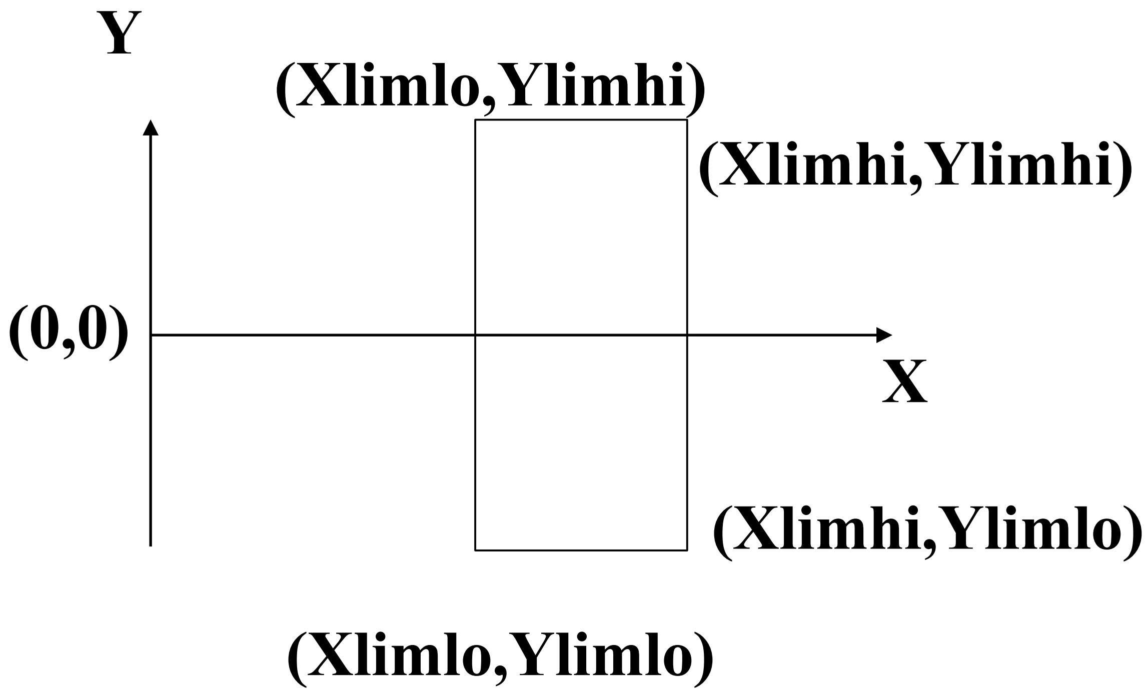
Power requirements for the cavity

- Xpower – power required for gradient
  - $Pkly = (L * E^2/(4*Q_{ext}*r/Q))$
- Xpowerbeam
  - $Pklybeam = L*(E+(I_0*Q_{ext}*r/Q))^2/(4*Q_{ext}*r/Q)$
- Ypower – reactive power available for detuning
  - Pklydf = Pkly * tan(dA) * tan(dA)
- Total power no beam = Xpowerbeam + Ypower ($I_0 = 0$)
- Total power with beam = Xpowerbeam + Ypower (I_0 = beam current)
- Resultant voltage limits for the power

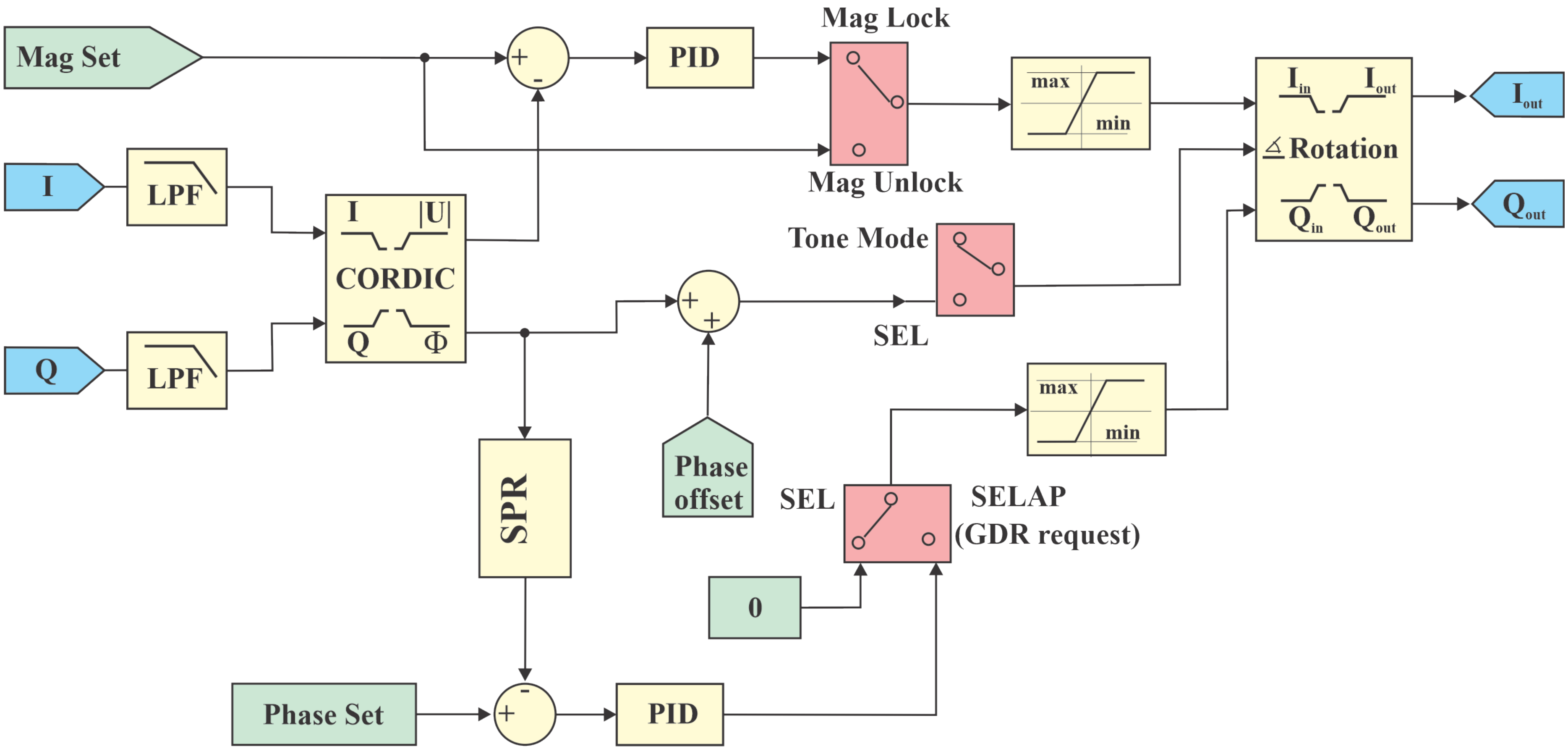
Power limits for the cavity

- Power limits translated to drive voltage for FPGA
- Xlim are the main power
- Ylim are the detuning budget
- Ylimlo is the same as Ylimhi with opposite sign
  - Detuning on either side



New Algorithm Test on UITF

New Controller



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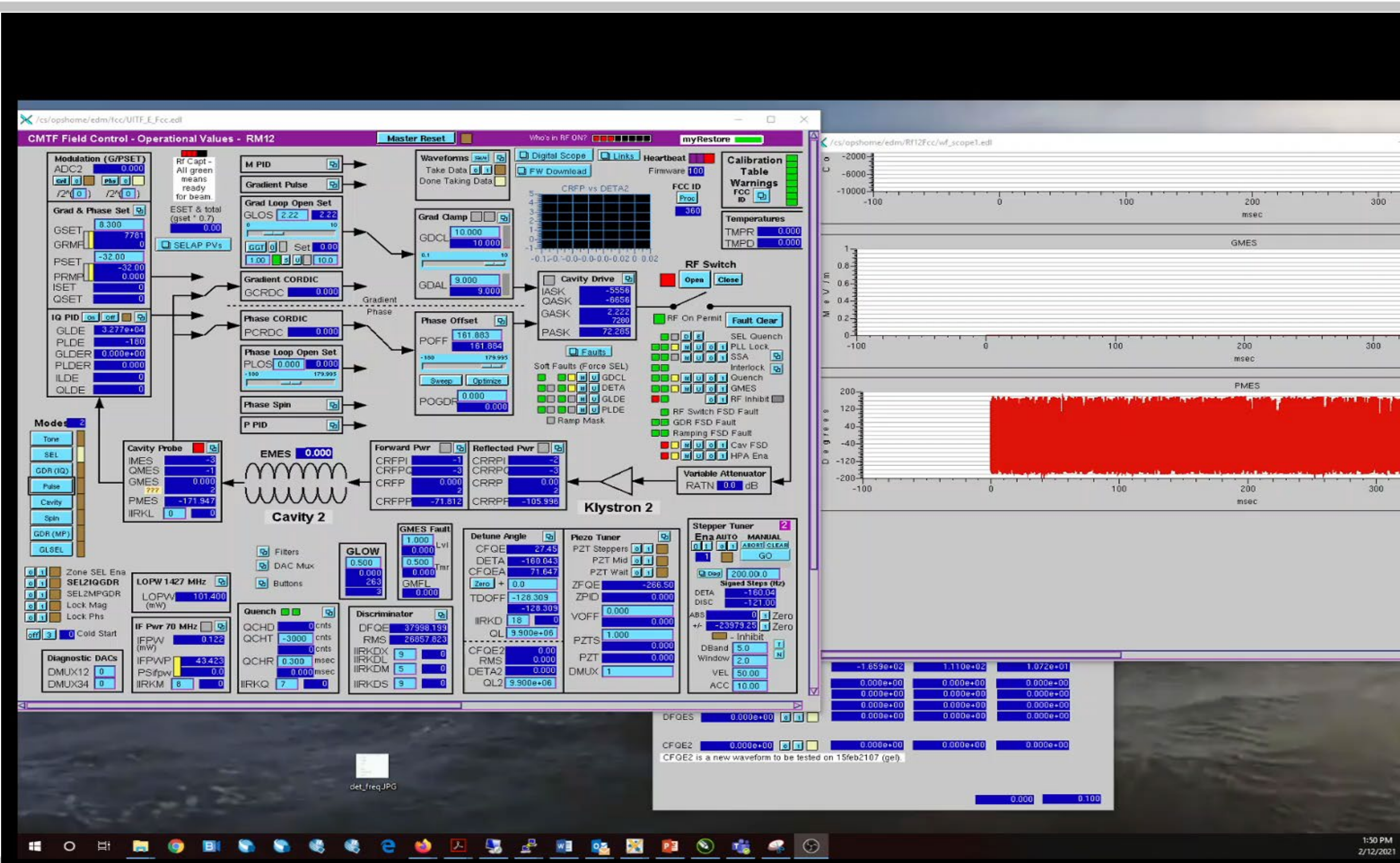
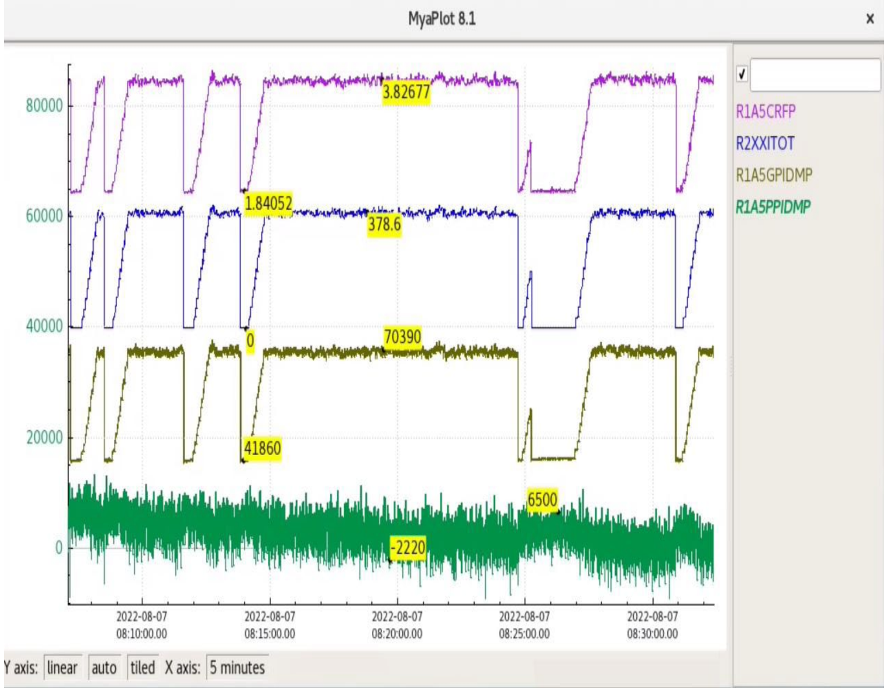
RF Test on UITF Booster 7-cell Cavity



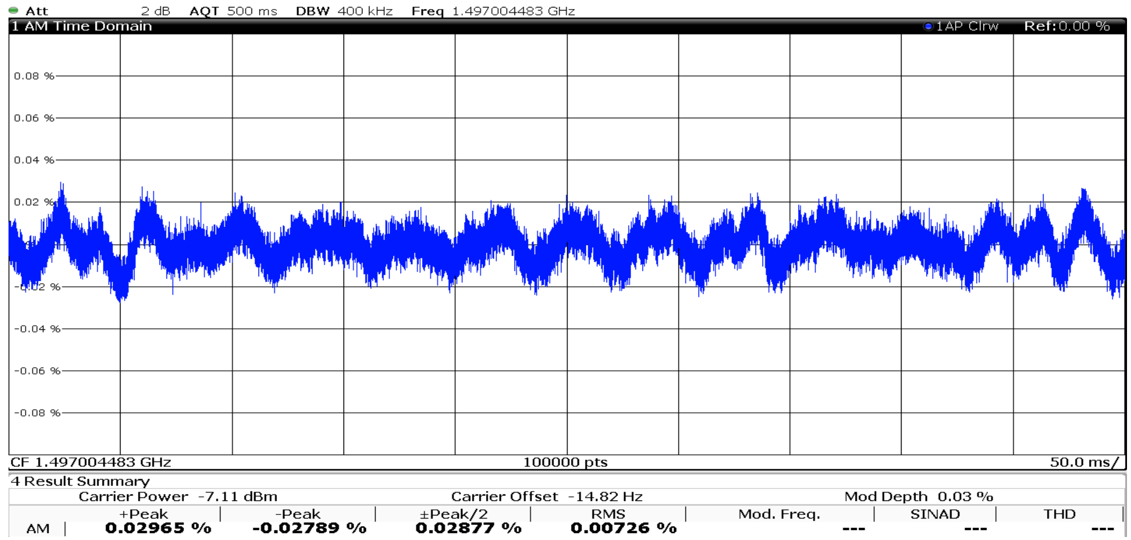
LLRF 3.0 in the LINAC

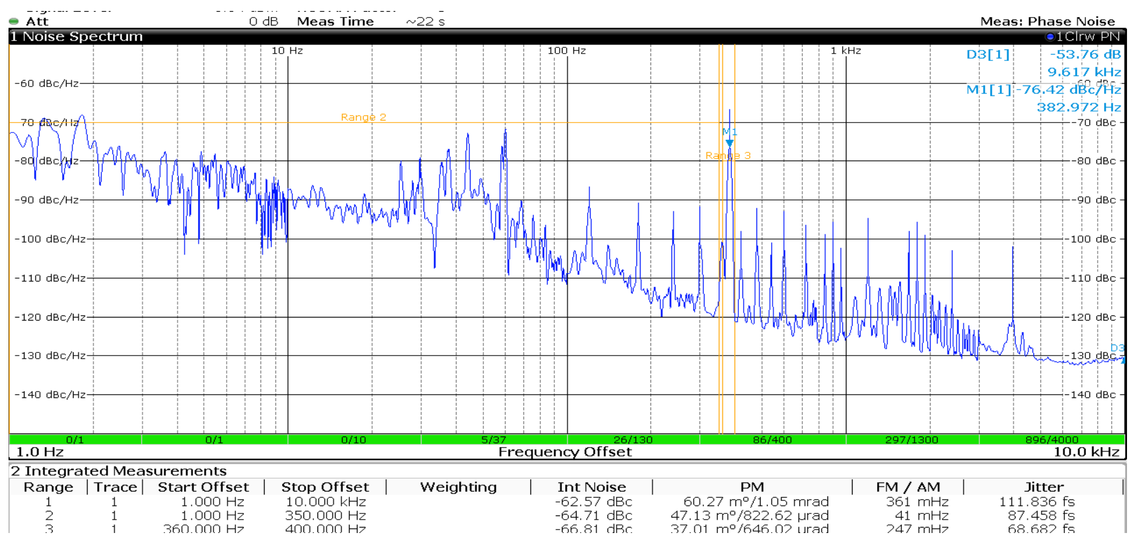
- Installed on two C75 cryomodule(16 cavities)
  - July 2021, May 2022
- Klystron Characterization
- Cavity Characterization
- SRF commissioning
- SELAP without beam
- SELAP with 400 uA beam
- Beam current through EPICS
- Adjust the limits with beam



Field and Phase regulation

- Requirements
  - Gradient
    - .045%
  - Phase
    - .5 deg
- Measured
  - Out of the loop measurement
  - Gradient
    - .007%
  - Phase
    - 60 mdeg
    - 1 Hz – 10 kHz





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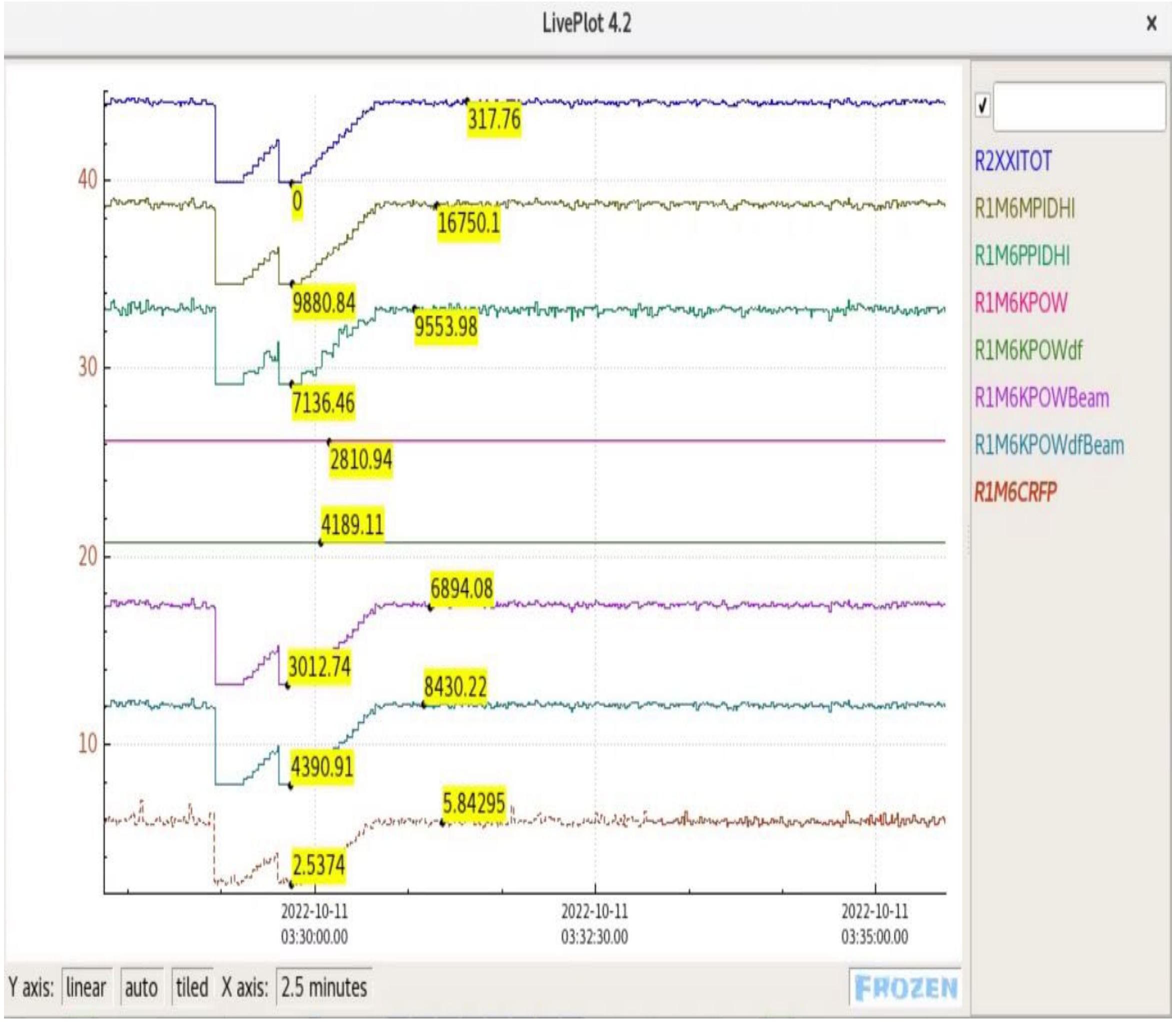
Power Limits with Beam Loading

- R2XXITOT- Beam in uA
  - EPICS
- KPOW –pwr reqd with no beam, no detuning
- KPOWdf – pwr reqd with no beam, detuning
- KPOWBeam – pwr reqd with beam
- KPOWBeam – pwr required with beam,detuning
- MPIDHI - xlimhi
- PPIDHI – ylimhi
- CRFP – fwd pwr in kW
- Limits are as good as calibration
- Initial Beam Current of 50 uA
  - Feed forward is slow
- False trips on beam transients
  - Operating gradient is close to quench limit



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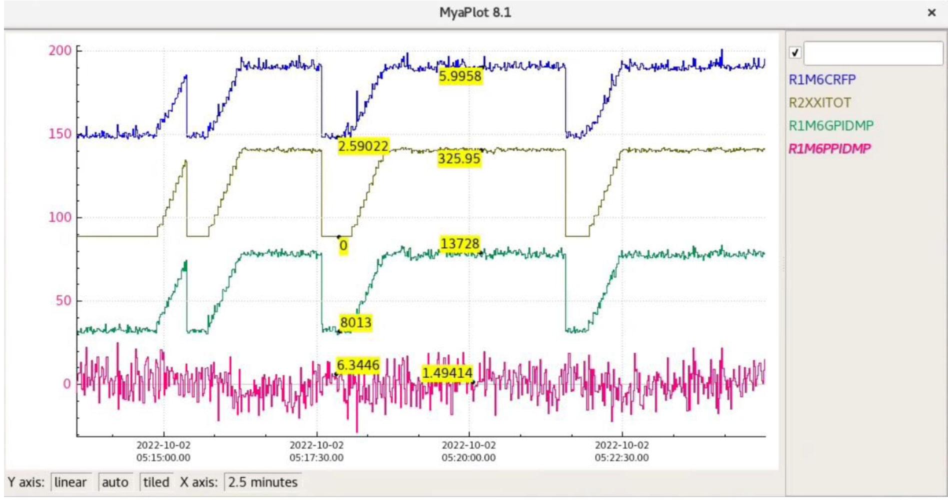
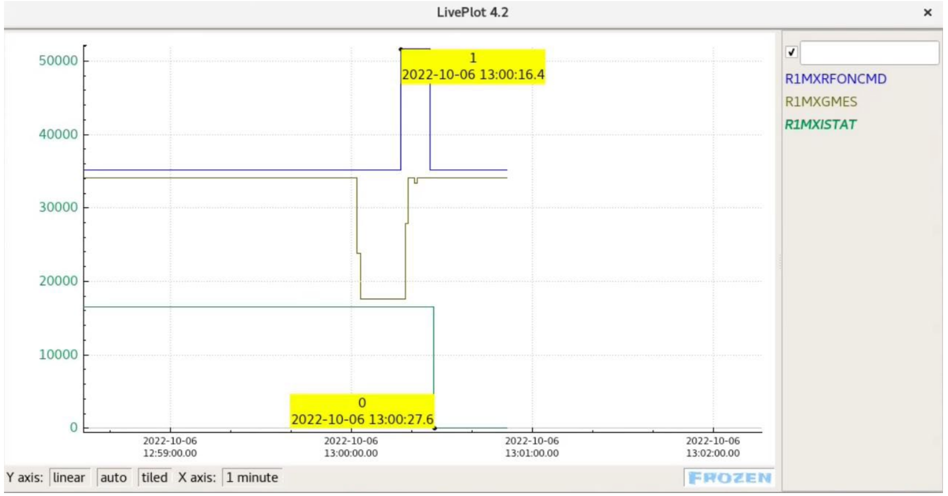
SELAP in LLRF 2.0

- Installed in three C100 cryomodules (24 cavities)
  - May 2022, Sep 2022
- Klystron Characterization
- Cavity Characterization
- SELAP without beam
- SELAP with 400 uA beam
- Eliminated cavity fratricide
  - ~800 Hz Lorentz force detuning
  - 10% mechanical coupling
- Faster recovery
  - 1.5 minutes vs 10 secs
- Channel isolation 55-60 dB
  - Impacts the loop gain





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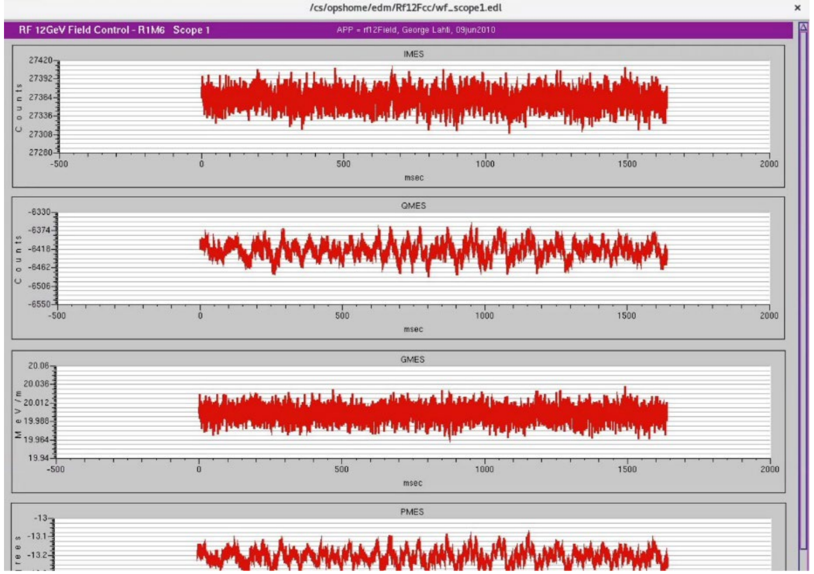
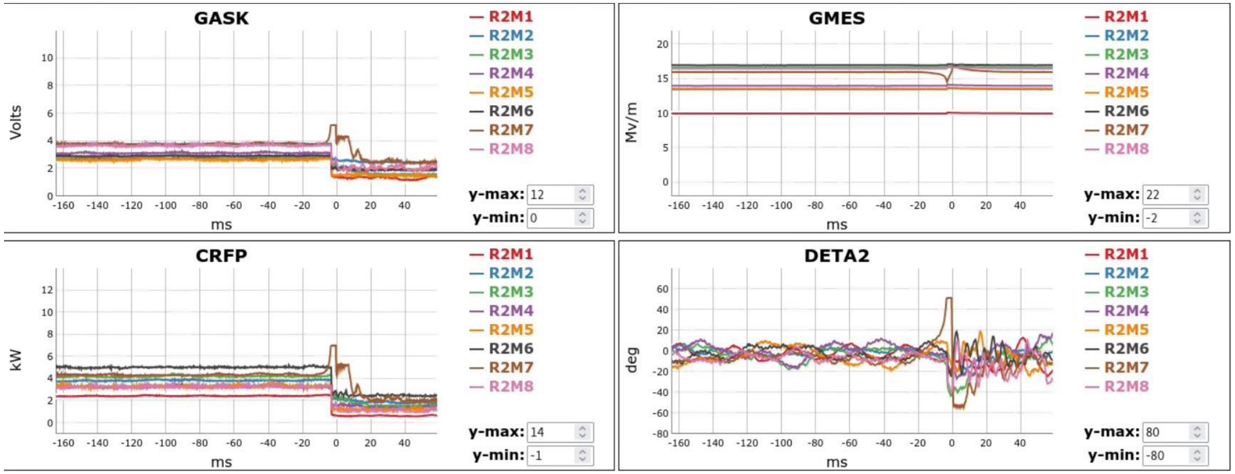
Dual Data Buffers

- Live data for diagnostics
  - Time and frequency domain
  - min, max, rms, stddev
- Fault data for offline analysis
  - Synchronized across the cryomodule
  - AI/ML





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Future Work and Conclusions

- Upgrade all C100 zones with SELAP
  - Nine more cryomodules (72 cavities)
- Fine tune the algorithm to eliminate any false trips
- Data acquisition on beam trip
  - Capture the data in digital LLRF zones
- SELAP is an efficient algorithm to operate the srf cavities
  - Gradient is regulated, phase gets unlocked
  - Eliminates cavity fratricide
  - Doesn't saturate the amplifier
- Faster recovery
  - Whole zone is recovered in ~5 sec
  - Recovery can be instantaneous
- Collaborations are great
  - LCLS-II collaboration
- Special Thanks to L. Doolittle