The Self Excited Loop Cavity Field Controller and The Cavity Simulator Implemented in MTCA.4 System

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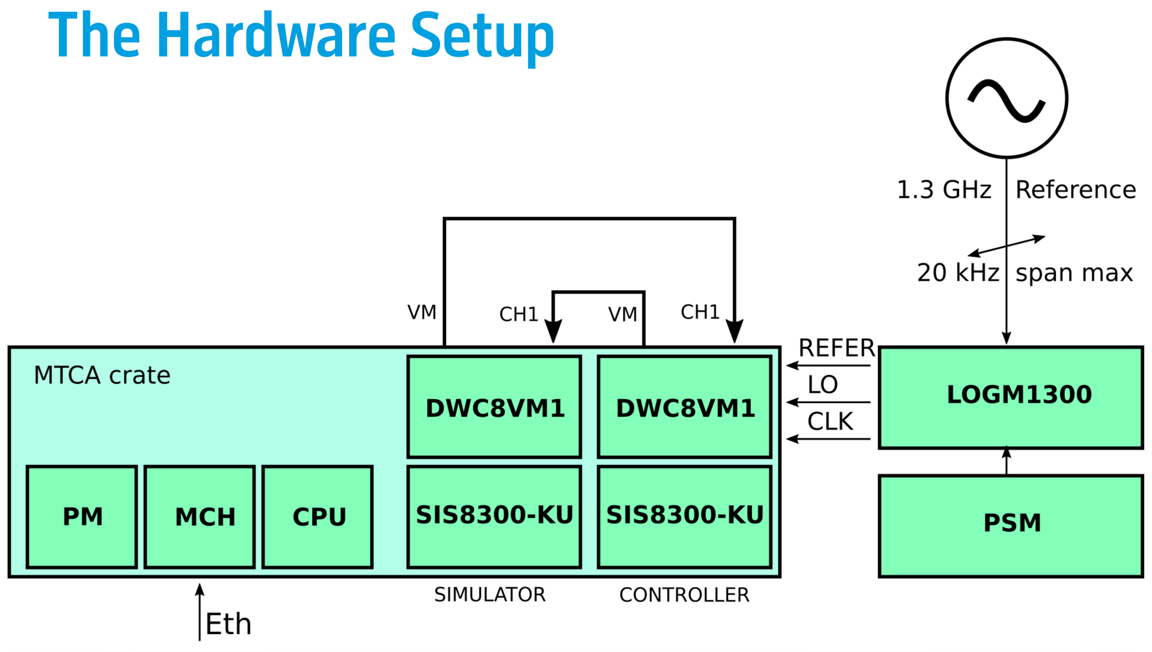
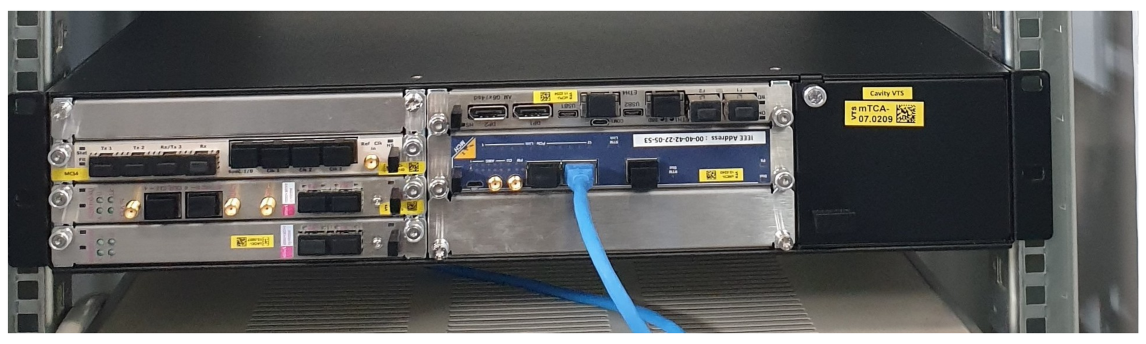
Introduction

The superconducting cavity vertical test stand at DESY is going to be updated with the MTCA.4 based system. The digital self exited loop (SEL) LLRF controller has been developed to fulfill the requirements for the controller to drive the cavity with high Q_L up to 1e10 and high cavity detuning up to 10kHz. In order to test the SEL controller, additionally the real-time cavity simulator (SIM) has been developed. The electrical and mechanical model of a cavity represented by a differential equation, is implemented inside the FPGA. The model takes the forward power as an input and produces a probe signal based on given detuning and half-bandwidth parameters of a cavity. The microphonic disturbance is also added to simulate the high Q_l operation.

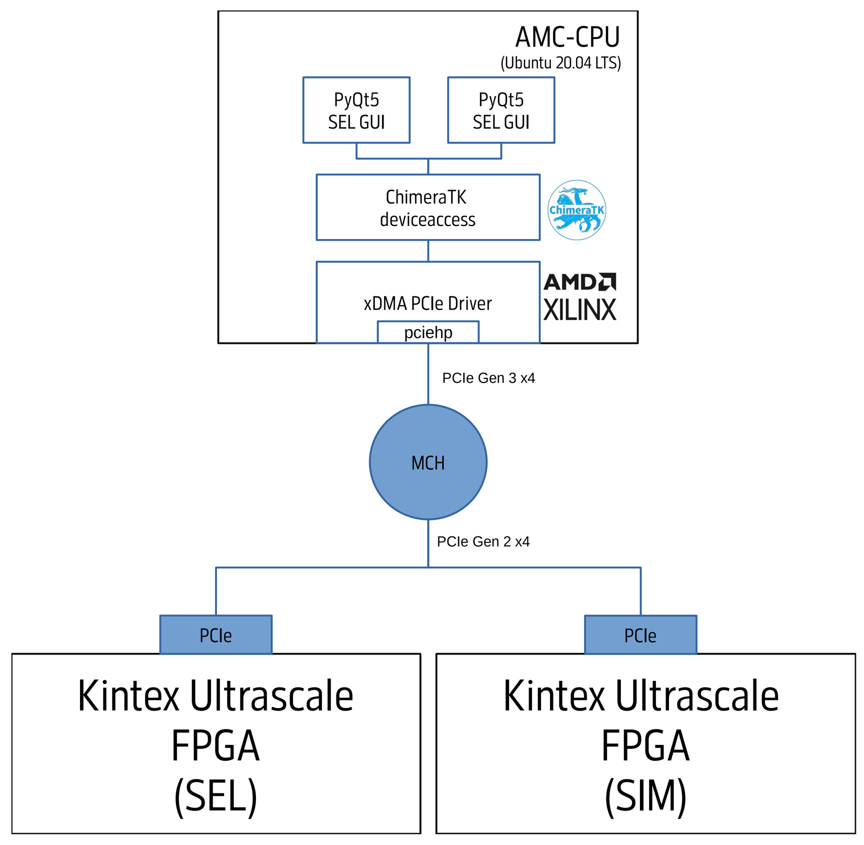
Both, the cavity simulator and the SEL controller has been implemented in the SIS8300KU, DRTM-DW8VM1 pair boards based on MTCA.4 Standard

The Hardware Setup



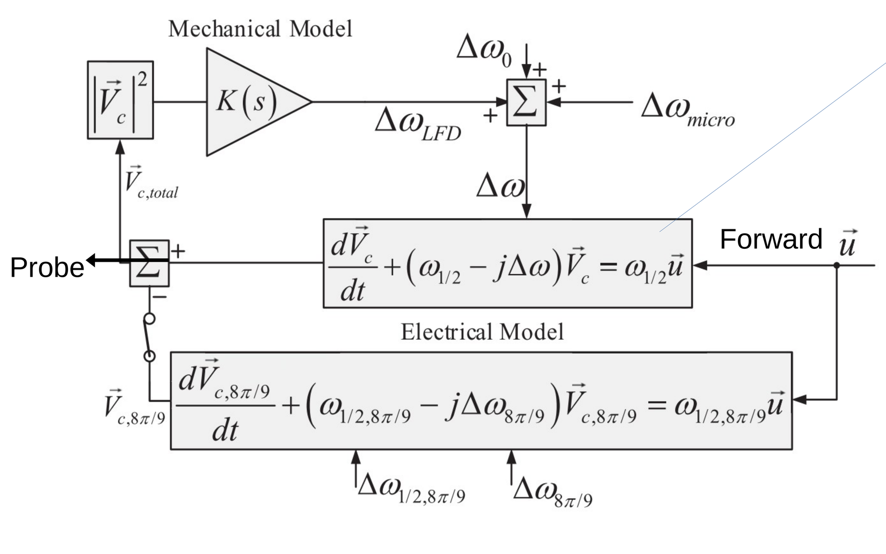


The Software Setup



Cavity Simulator

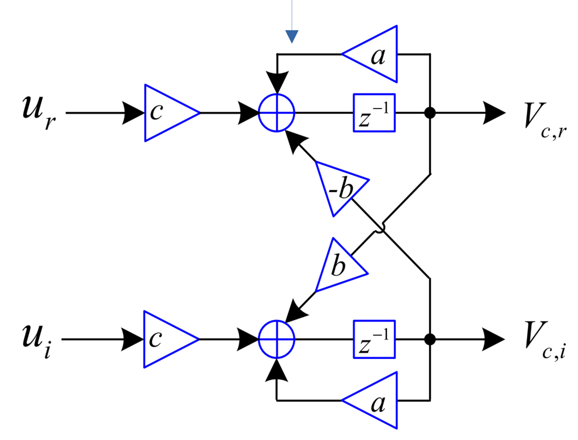
- Simulates Electrical (π mode only) & Mechanical Model of a cavity based on the works of Feng Qiu,1,2,* Shinichiro Michizono, et al, [1].
- Mechanical Model Input: Cavity Voltage Squared Output: Detuning caused by Lorenz Force ($\Delta\omega_{LFD}$)
- Mechanical Model Implementation: 4th order IIR Filter
- External microphonics: User defined table
- Electrical model parameters: Cavity Half-Bandwidth ($\Delta\omega_{1/2}$)
  Initial Detuning ($\Delta\omega_0$)
  Sampling Period (T_s)



Overview of the Cavity Simulator [1]

$$\begin{bmatrix} V_{c,r}(n) \\ V_{c,i}(n) \end{bmatrix} = \begin{bmatrix} 1 - T_s\omega_{1/2} & -T_s\Delta\omega \\ T_s\Delta\omega & 1 - T_s\omega_{1/2} \end{bmatrix} \begin{bmatrix} V_{c,r}(n-1) \\ V_{c,i}(n-1) \end{bmatrix} + \begin{bmatrix} T_s\omega_{1/2} & 0 \\ 0 & T_s\omega_{1/2} \end{bmatrix} \begin{bmatrix} u_r(n-1) \\ u_i(n-1) \end{bmatrix}.$$

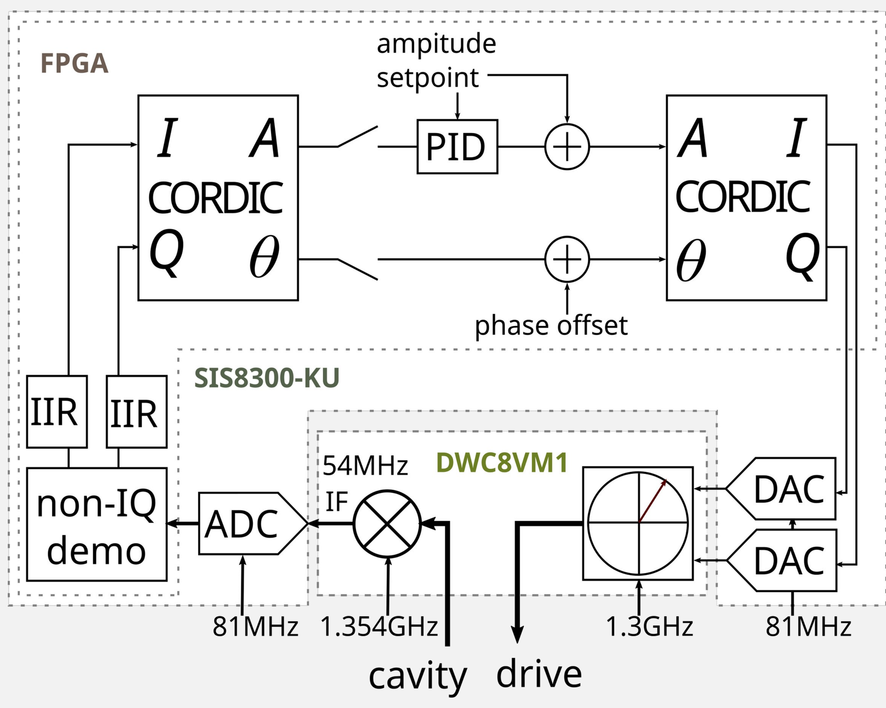
Differential equation in discreet time form [1]



Digital implementation of electrical model [1]

SEL Controller

The SEL controller is fully implemented in FPGA. The implementation uses the same hardware components as the standard GDR system. The SEL loop is an oscillator with a positive feedback that is able to track the cavity resonant frequency. In this implementation the driving frequency is changed with the use of vector modulator that modulates the reference signal. The reference signal should be in the range of the cavity center frequency.



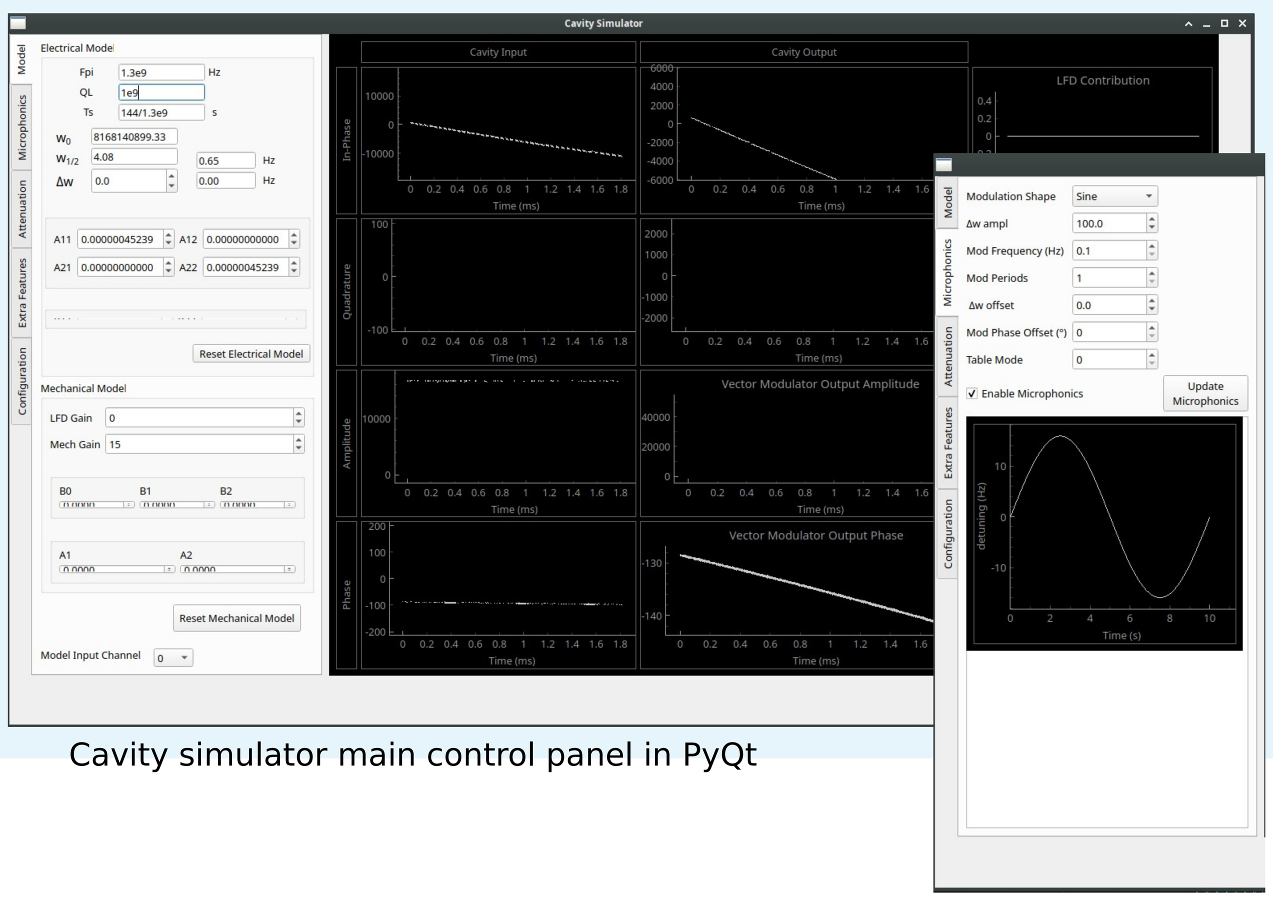
Block diagram of digital LLRF SEL controller

Hardware Test Results

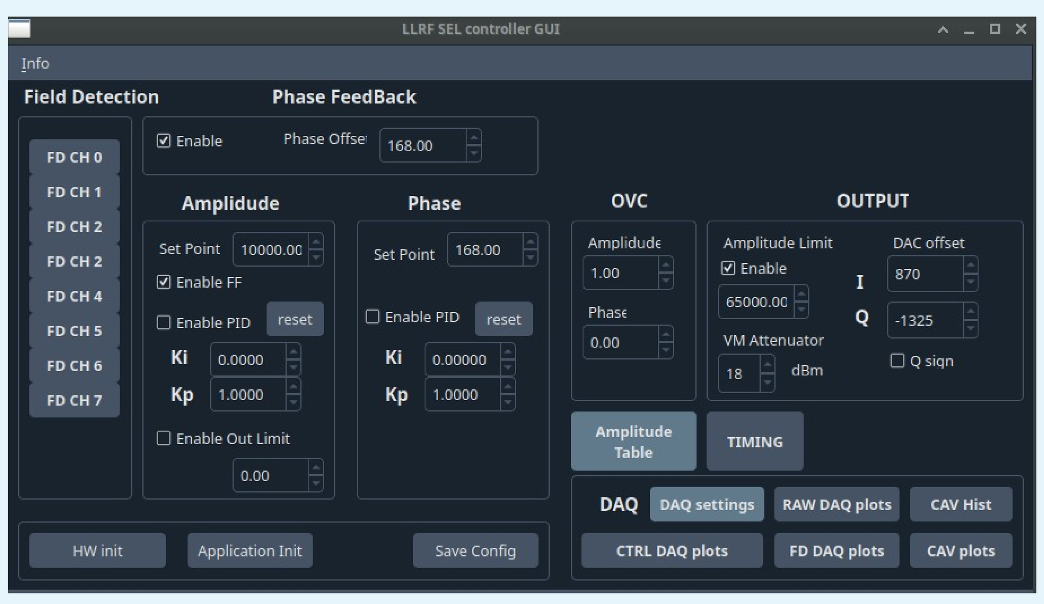
SEL with the cavity simulator has been testes on hardware with various scenarios emulating vertical test stand. This is high QL, high microphonics, long pulse and CW operations.

On the pictures PyQt panels presenting one case:

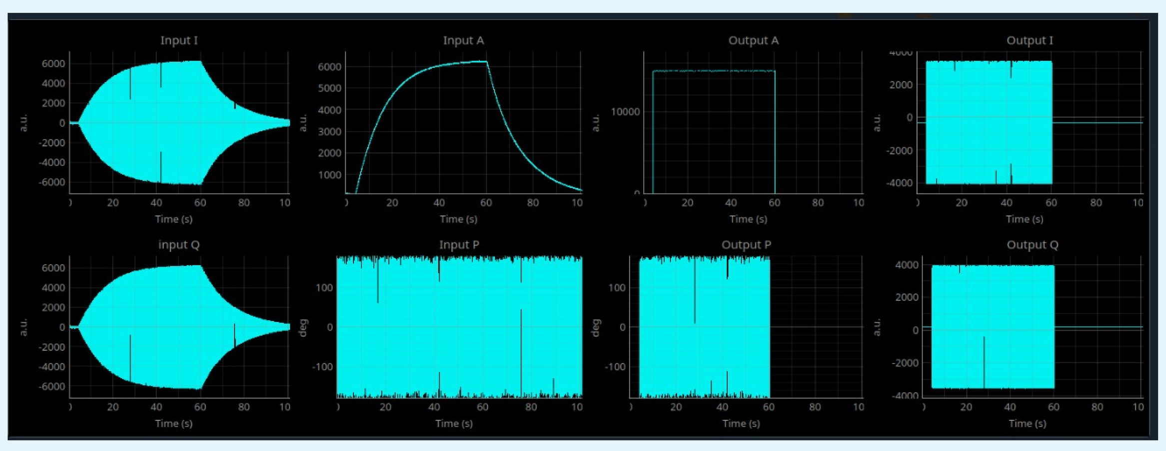
- long pulse (~1.5s) operations
- cavity QL = 1e9
- microphonics making 16Hz detuning at 0.1 Hz cavity Bandwidth



Cavity simulator main control panel in PyQt



SEL controller main panel in PyQt (PySide6)

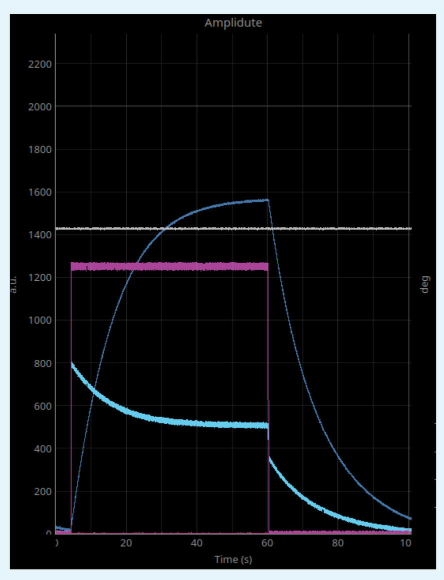


DAQ plots of the SEL controller in PyQt

Summary

The setup of the cavity simulator with the SEL controller helped significantly in the software and firmware development process.

The SEL controller has been finally successfully tested at the vertical test stand. The controller was able to stayed lock for with cavity with high QL up to 5e10 and with high microphonics generated by increase of the cryobath temperature from 1.5K to 2K in a few minutes.



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[1] Real-time cavity simulator-based low-level radio-frequency test bench and applications for accelerators. Feng Qiu,1,2,* Shinichiro Michizono, et al, PHYSICAL REVIEW ACCELERATORS AND BEAMS, 2018