NEXT GENERATION FRIB LLRF CONTROLLER*

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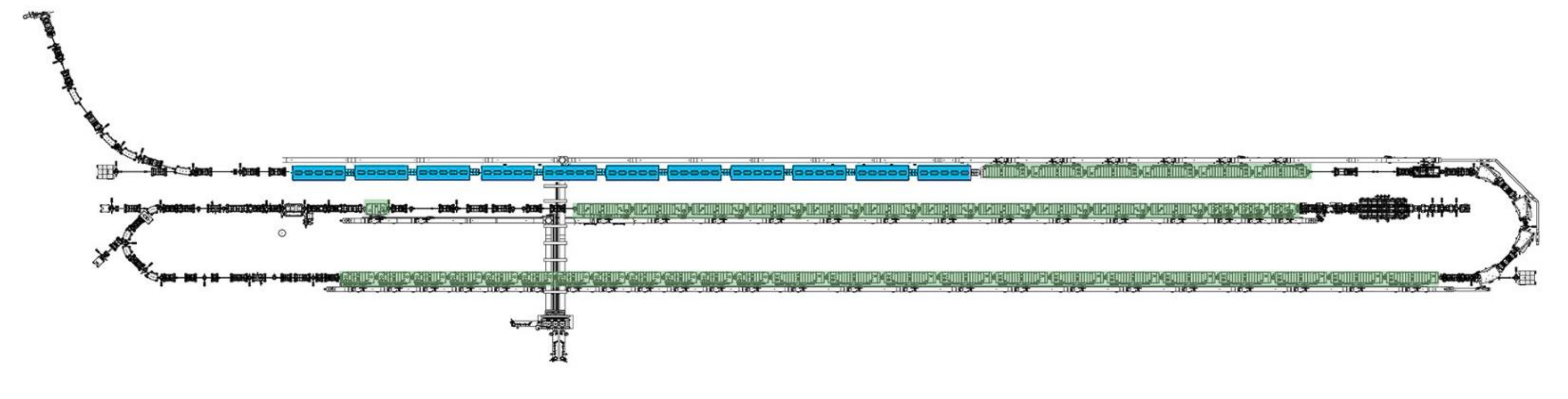
Introduction

The tremendous discovery potential of FRIB can be further extended with an energy upgrade of the FRIB linear accelerator to 400 MeV/u and to higher energies for lighter ions. Footprint of the current (green and black) and upgraded (blue) FRIB linac.



The low level radio frequency (LLRF) controller is designed to accommodate Facility for Rare Isotope Beams (FRIB) superconducting (SC) and Ultrafast Electron Microscope (UEM) room temperature (RT) cavity types (See Table 1).

Table 1: Cavity Types

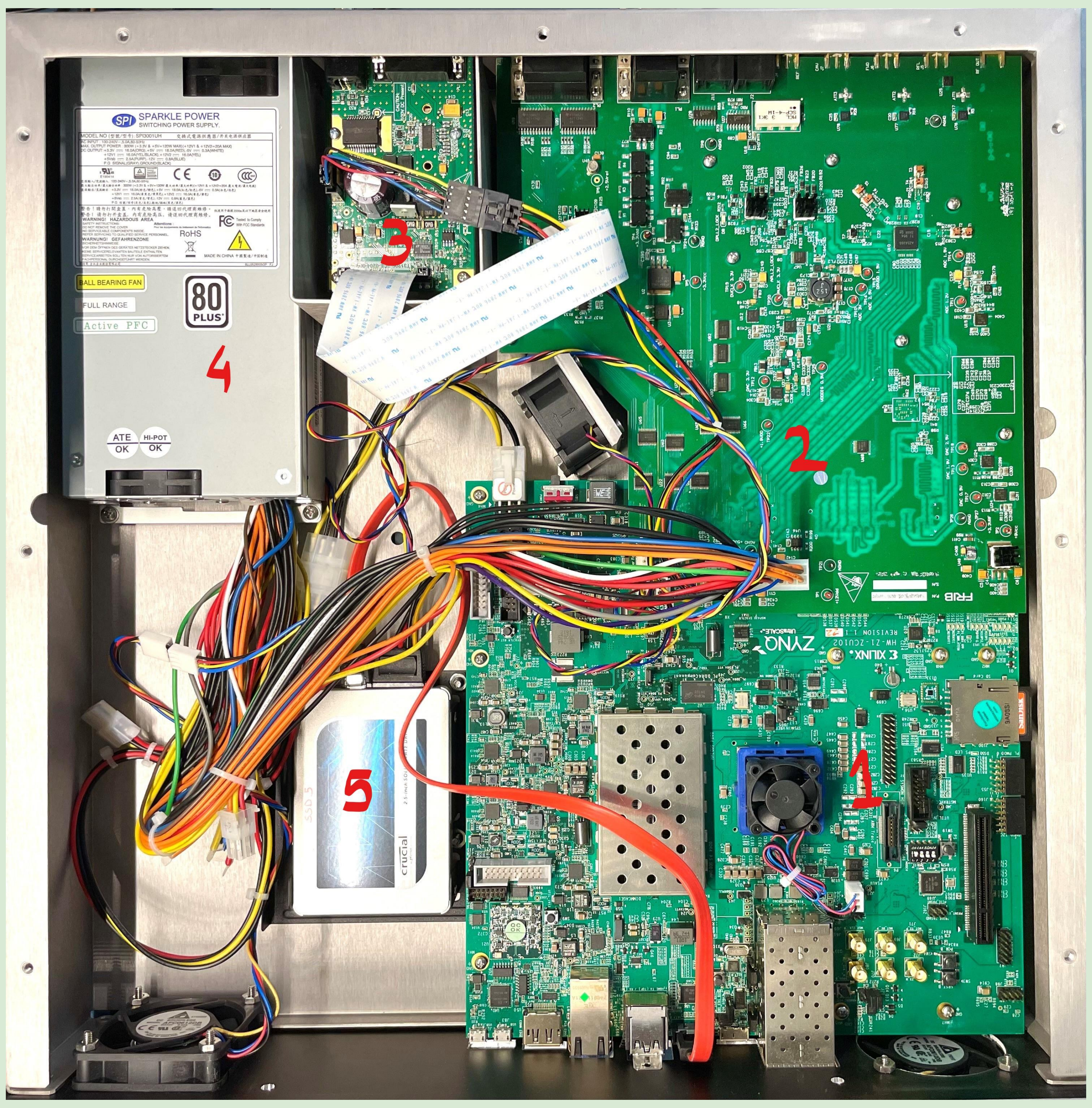
System	Frequency (MHz)	Type	Tuner
FRIB	40.25 - 322	SC/RT	Stepper/ Pneumatic
FRIB400	644	SC	Piezo/Stepper
UEM	1013.6	RT	N/A

The current LLRF controllers in operation at FRIB are based on Xilinx Spartan 6 field programmable gate array (FPGA) and support frequencies up to 322 MHz. With requirements for higher frequency operation there was a need to upgrade the LLRF controller. A comparison of current and new controllers is shown in Table 2.

Table 2: Controller comparison

Component	Current	New
Analog-to-Digital Converter (ADC)	TI ADS6442, 14-bit, 65 MSPS, 500 MHz bandwidth	TI ADS54J66, 14-bit, 500 MSPS, 900 MHz bandwidth
Digital-to-Analog Converter (DAC)	TI DAC5675A,14-bit, 400 MSPS	TI DAC37J82, 16-bit, 1.6 GSPS
FPGA	Xilinx Spartan-6	Xilinx Zynq Ultrascale Multi Processor System on Chip (MPSoC)
Phase Locked Loop (PLL) / Voltage Controlled Oscillator (VCO	TI LMK03000, Precision Clock Conditioner with Integrated VCO	TI LMK04828, Ultra Low-Noise JESD204B Compliant Clock Jitter Cleaner
RF Printed Circuit Board	FR4, 6 layer	RO4350B, 8 layer

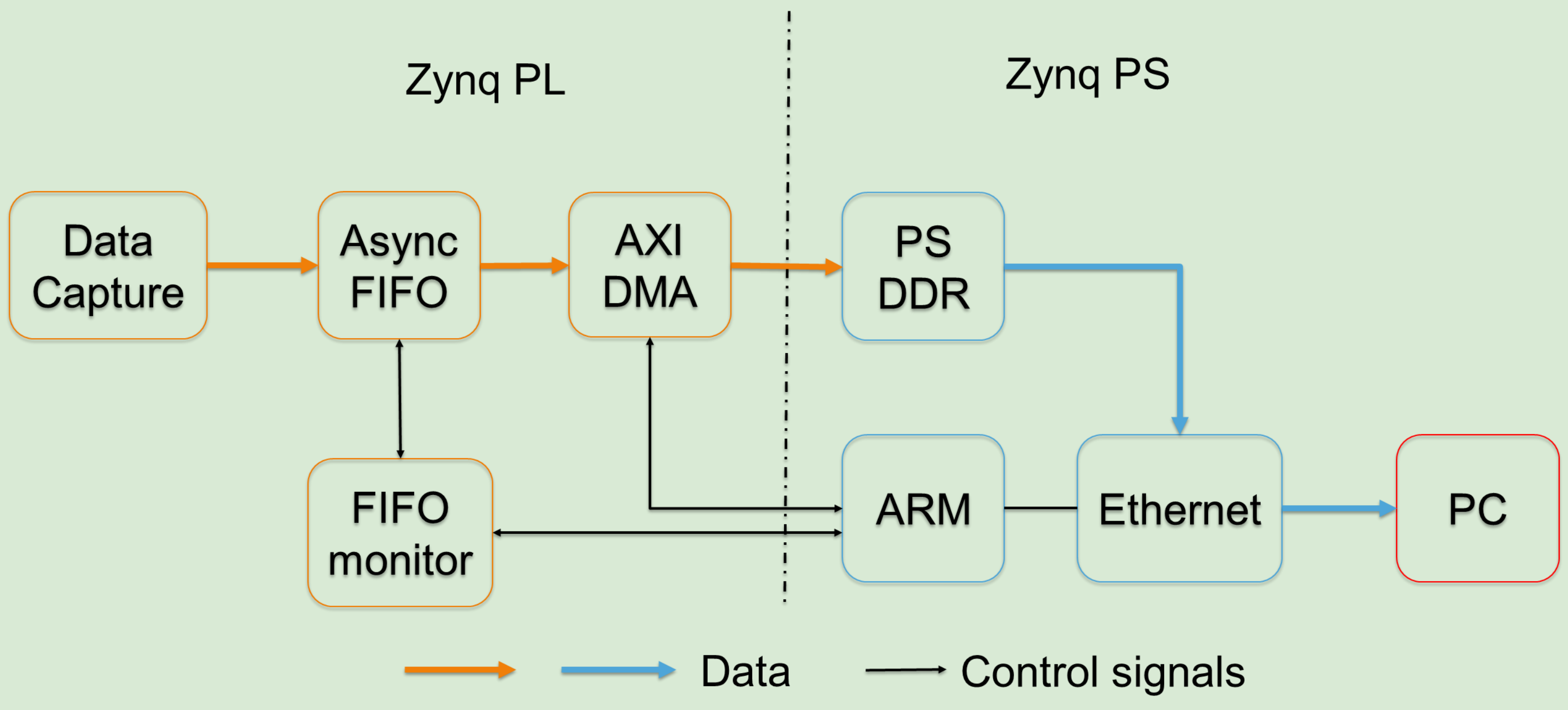
New LLRF Controller Chassis



Components -
1. Xilinx ZCU102 FPGA Board
2. RF Board
3. Stepper/Piezo Tuner board
4. 1U Switching Power Supply
5. Solid State Drive (SSD)

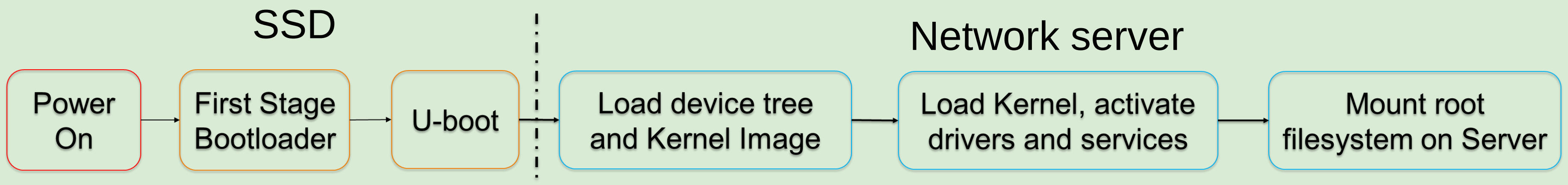
Features –
- 2U chassis
- Efficient thermal design with multiple cooling fans
- Single power supply for all components
- Rack mountable
- Modular

Fast Data Acquisition


Zynq PL
Zynq PS
Data Capture
Async FIFO
AXI DMA
PS DDR
FIFO monitor
ARM
Ethernet
PC
Data
Control signals

- Fast data capture at native resolution of ~ 5 MHz.
- AXI DMA, configured in simple mode, moves data from Programmable Logic (PL) to Processing System (PS) Double Data Rate (DDR) memory that is shared between PL and user-space application.
- Helpful in performing detailed analysis, such as cavity decay, fast transient, etc.

Proposed Network Boot


SSD
Network server
Power On
First Stage Bootloader
U-boot
Load device tree and Kernel Image
Load Kernel, activate drivers and services
Mount root filesystem on Server

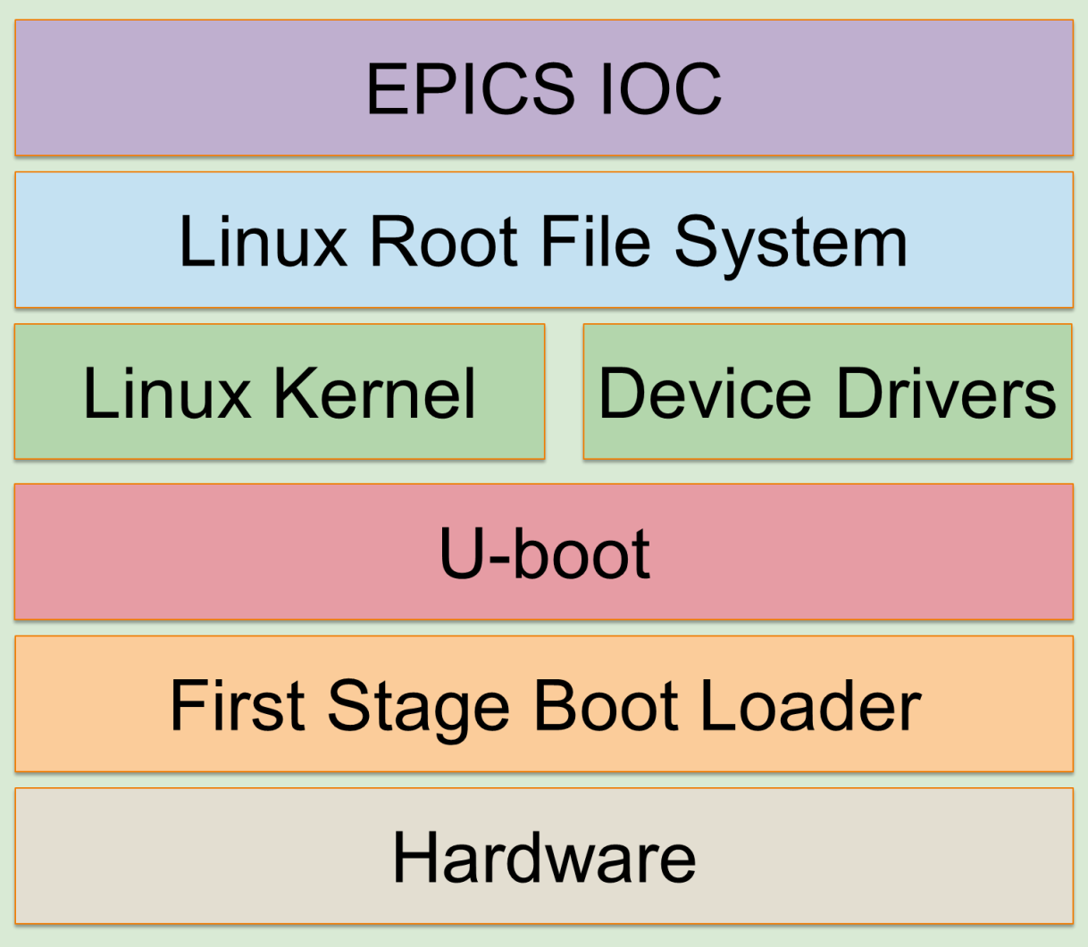
- Start booting from local storage (flash, SSD) and hand over to network server for remaining booting process.
- Keep minimum files required for boot, e.g. – FSBL, PMUFW and U-boot.
- Network server stores Linux Kernel Image, device tree binary, boot script and bitstream.
- U-boot obtains boot script that contains custom u-boot configuration from server and fetches kernel along with device tree to start kernel.
- Kernel obtains root path from server and mounts root file system over network file system that starts user-space applications.

EPICS IOC


Standalone IOC
LLRF
UDP
IOC
TCP
CS-Studio
IOC on chip
LLRF
IOC
TCP
CS-Studio

- Added latency due to network traffic.
- UDP connection is unreliable and lossy.
- Asyn port driver that uses EPICS timers as its main communication mechanism.
- Implemented in C++.

- Minimum latency since IOC server has access to FPGA registers via Linux userspace.
- Asyn driver adapted from softGlue driver available inside synApps.
- Implemented in C and needs to be ported to C++.


EPICS IOC
Linux Root File System
Linux Kernel
Device Drivers
U-boot
First Stage Boot Loader
Hardware

System	Version
Petalinux	2019.1
Linux Kernel	4.19
Linux OS	Debian 11 Bullseye
EPICS Base	3.16

Advantages -
- Running IOC server on the LLRF controller has many benefits including targeted maintenance, reduction in network traffic and latency, and distribution of resources.
- Targeted maintenance reduces risk of affecting other devices and IOCs.
- Distributed computing splits hardware computing resources.
- Gives hardware-level access to data and allows for interrupts to the IOC from the FPGA.

Challenges –
- Increase in total number of IOC servers under management.
- Maintenance of spares, keeping up-to-update with latest packages/versions.

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