Very Low Noise Receiver Technology for Digital Beam Position and Phase Measurement

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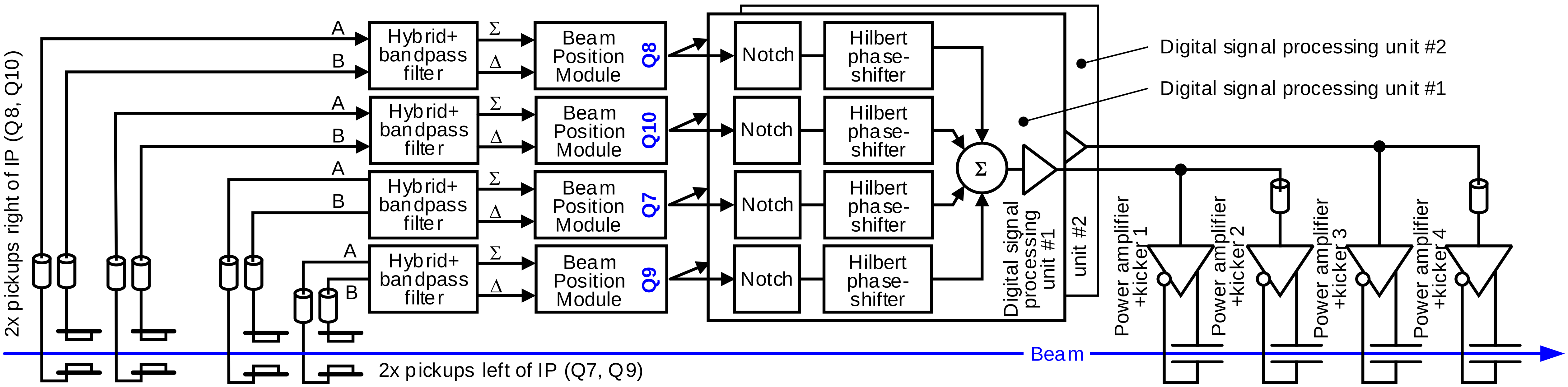
LHC transverse feedback system (ADT)

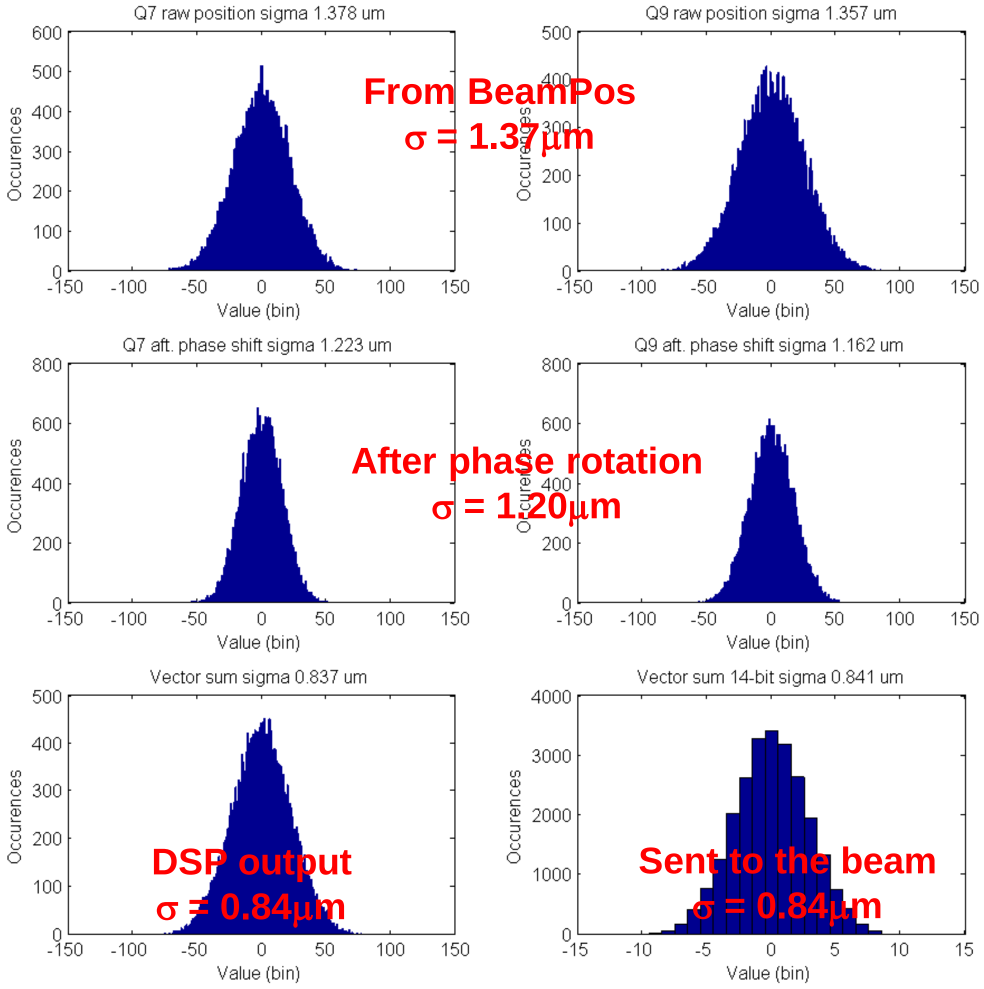


Current performance and motivation for upgrade

Noise floor of the LHC TFB beam position measurement system used in the LHC Runs I/II* was determined as:

1.03-1.40 μm_{RMS} at full scale ±2 mm (i.e. about -63 dBc)

Depending on pickup, settings and operating conditions.



*** LHC Run I (2009-2013), LHC Run II (2013-2018)**

Current performance and motivation for upgrade

The TFB performance during the LHC Runs I and II was greatly sufficient for the LHC operation. Nevertheless:

- **Recent studies showed that the TFB noise floor in the LHC must be reduced by at least factor of two in order to operate the machine with large beam-beam tune shift as foreseen in the High Luminosity LHC [2] and suppress the risk of loss of Landau damping by noise [3].**
- **Improvement by factor of 4 is required to recover an emittance growth rate in the order of 2% per hour as in the present LHC.**
- **Also, the future feedback system foreseen to suppress the LHC Crab Cavity noise in HL-LHC [4] relies on improved noise performance of the upgraded TFB.**

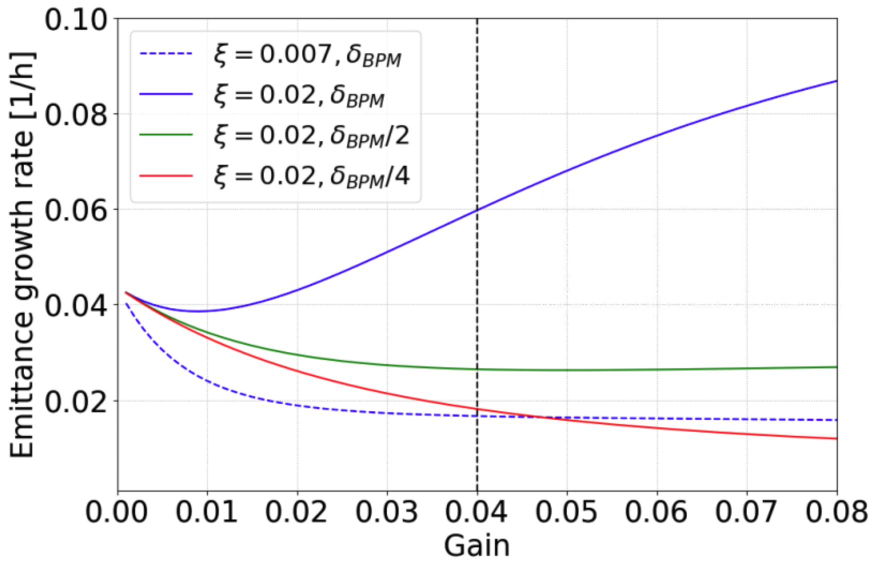
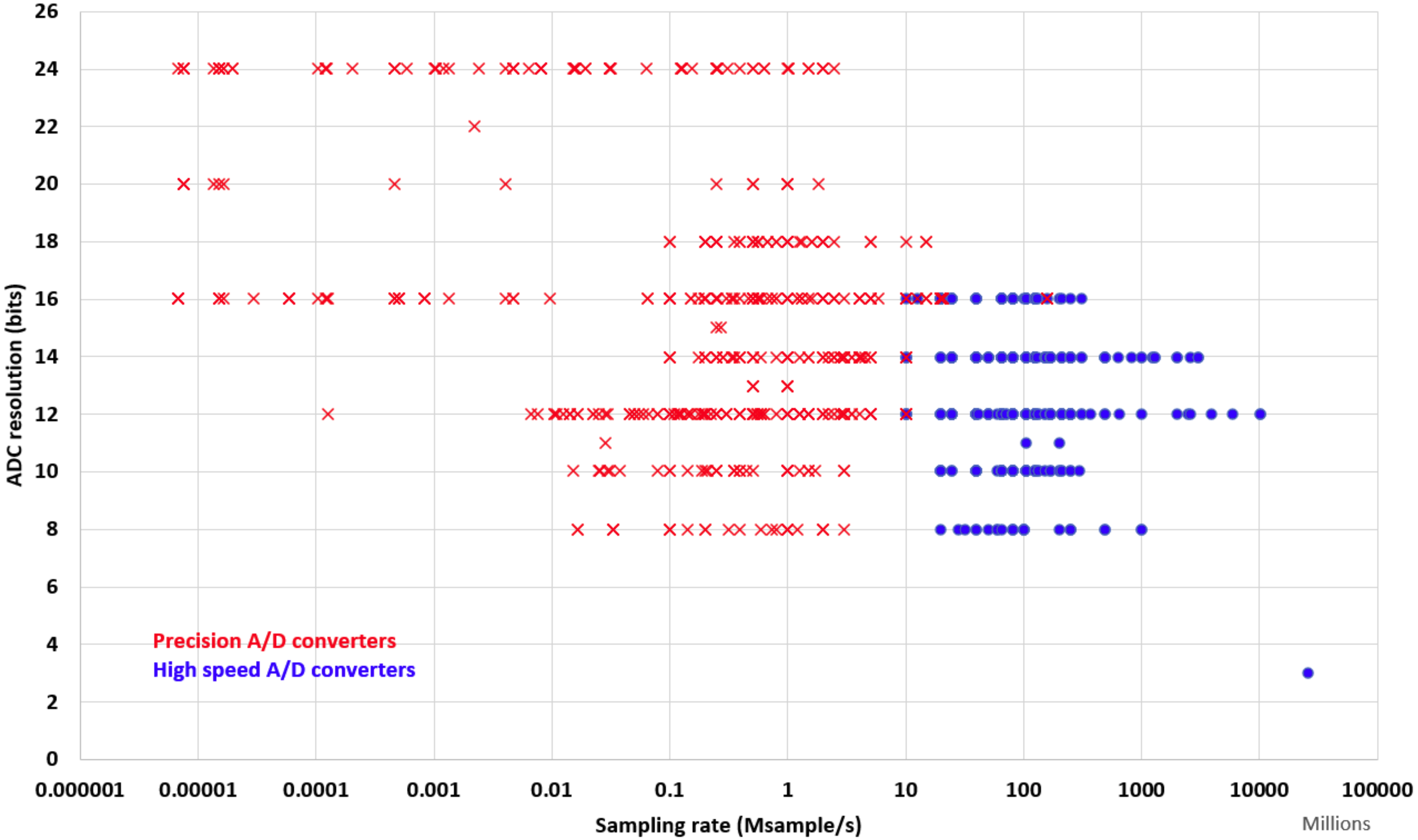


FIG. 10. Extrapolation of the emittance growth rate based on Eq. (1) and the parameters obtained empirically to a configuration featuring a reduced beam-beam tune shift with respect to the experiment. The potential impact of a reduction of the feedback noise by a factor 2 and 4 is also shown. A vertical dashed line was added to indicated the current operational feedback gain.

[2] Buffat, X. et al: "Modeling of the emittance growth due to decoherence in collision at the Large Hadron Collider, in Phys. Rev. Accel. Beams 23, 021002 (2020)

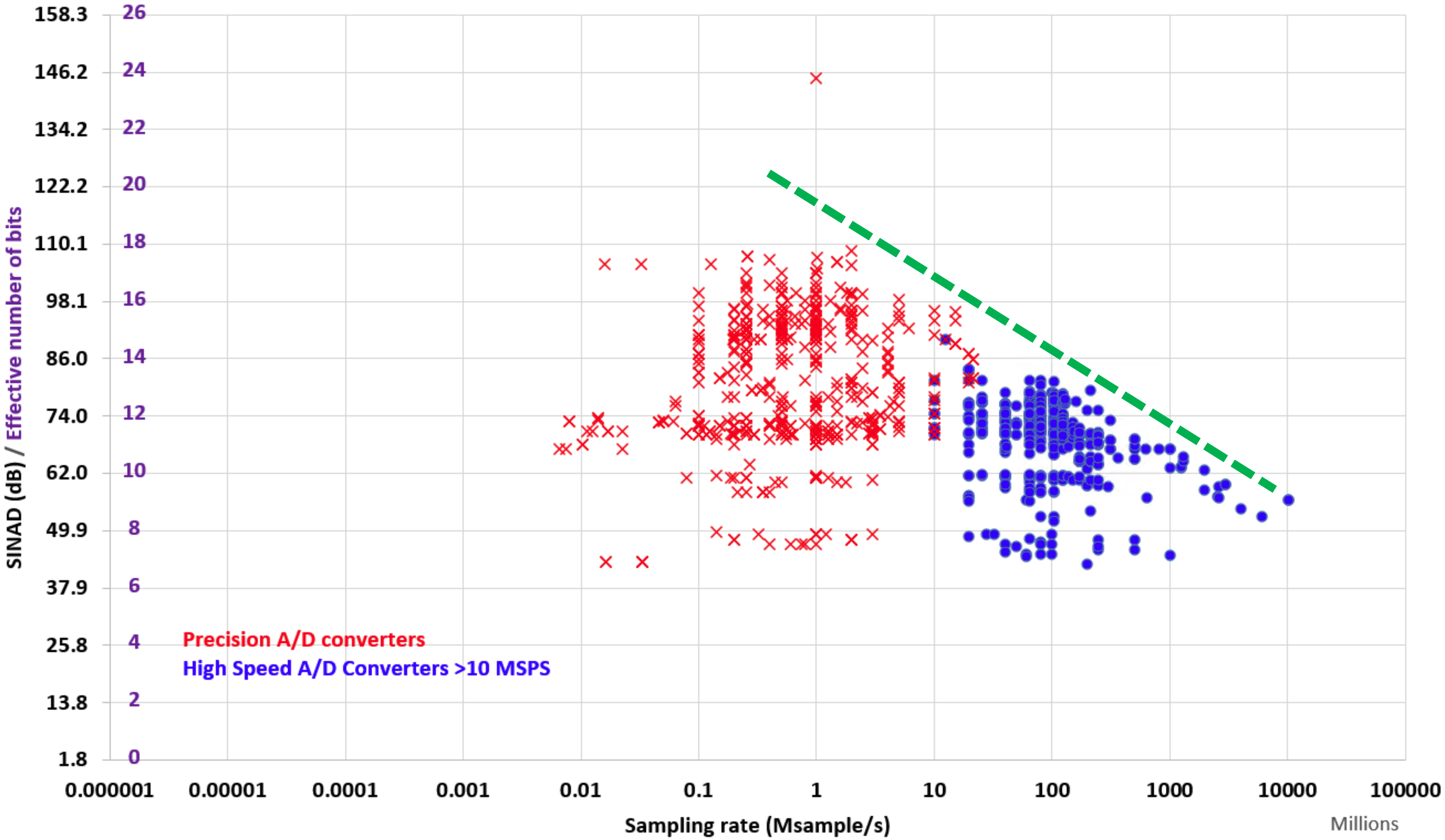
Few words on ADC performance…

1178 AD converter types from the Analog Device's portfolio. Datasheet parameters.



Few words on ADC performance…

1178 AD converter types from the Analog Device's portfolio. Real datasheet performance.



On ADC performance…

Very good reading with comprehensive ADC data:

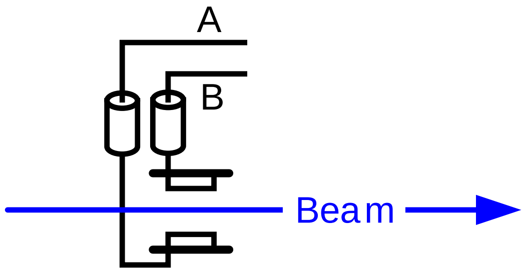
Boris Murmann, Department of Electrical Engineering, Stanford University:

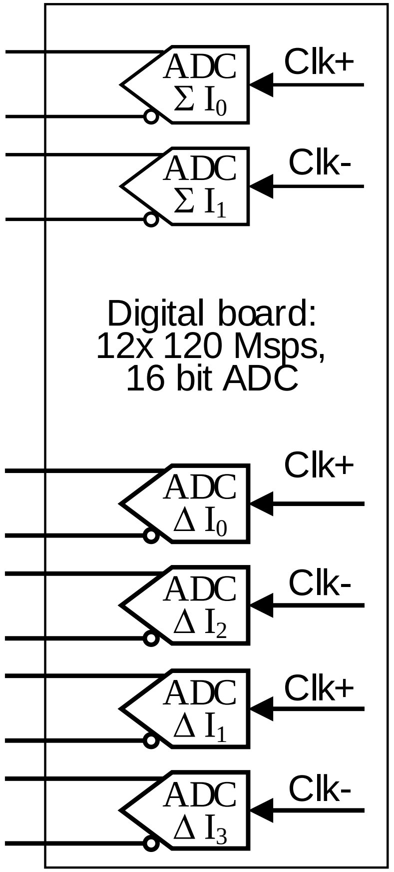
Energy Limits in A/D Converters

See [6] [7]

New system

Our FPGA (XC7A200T-1FFG1156C) can interface maximum six, dual channel, 16-bit DDR ADCs





Towards a new, very low noise hardware

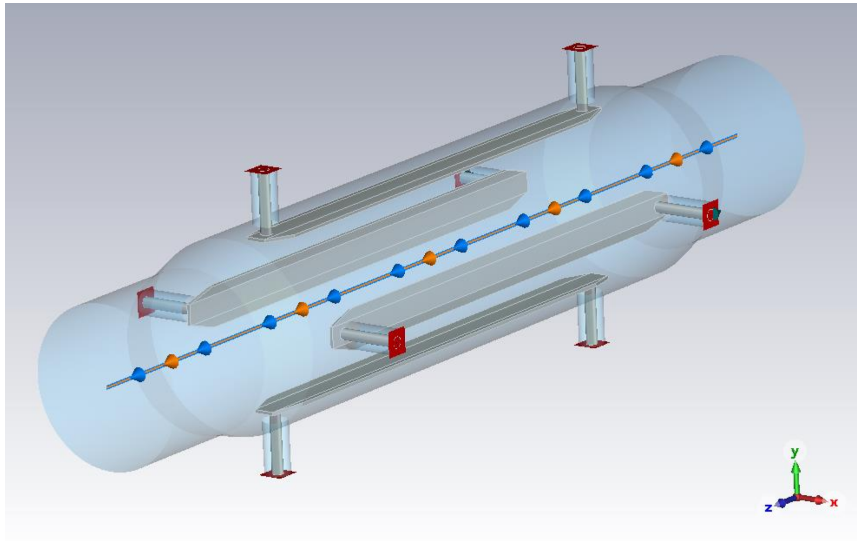
Options considered and evaluated

1) **Direct sampling of the raw A and B signals by low resolution, high speed digitizers.**
2) **Direct sampling of a band-pass filtered A and B signals by high resolution, medium speed digitizers.**
3) **Direct sampling of a band-pass filtered Σ and Δ signals by high resolution, medium speed digitizers.**
4) **Continue using the super-heterodyne principle and high resolution, medium speed digitizers, like the old beam position measurement system, but "super-optimize everything possible".**

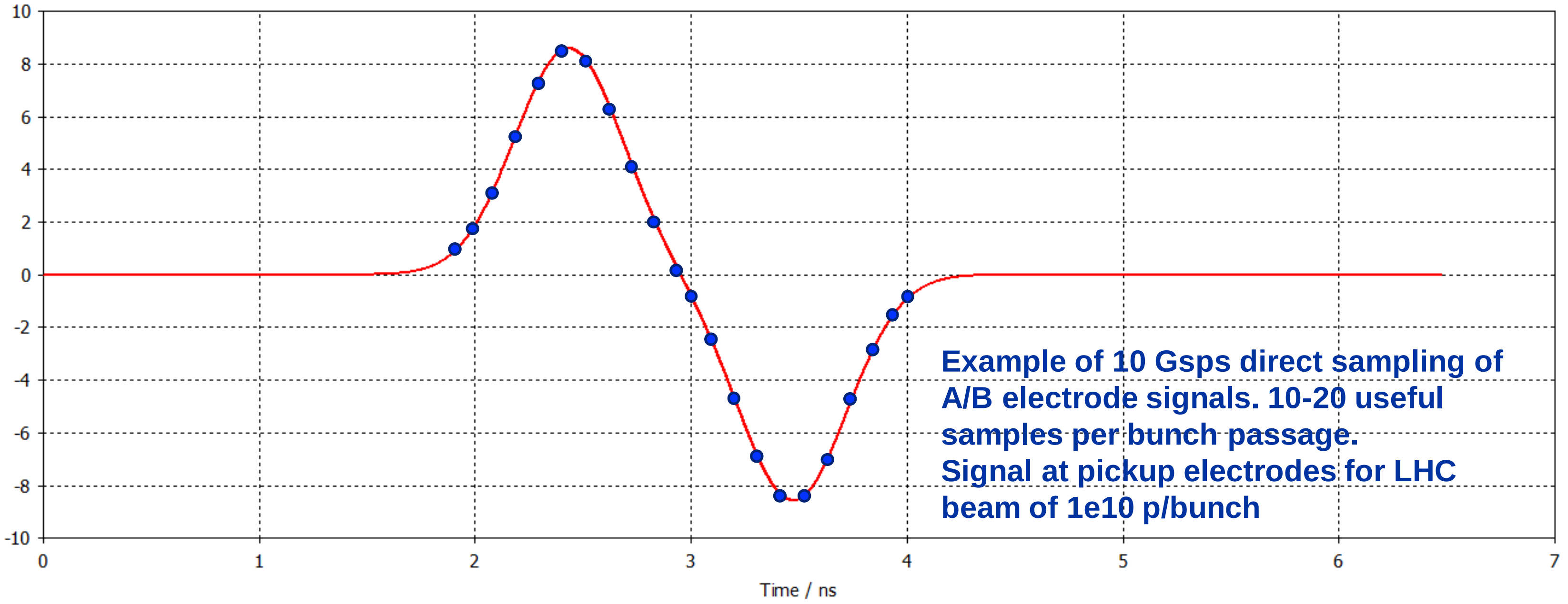
Towards a new, very low noise hardware

1) Direct sampling of the raw A and B signals by high speed digitizers.

The pickup electrode signals are typically a 1 ns long pulses with not more than a 2 dB difference in amplitude for a full scale bunch position movement. Effective number of bits (ENOB) of currently available multi-Gsps digitizers is too low for our application…



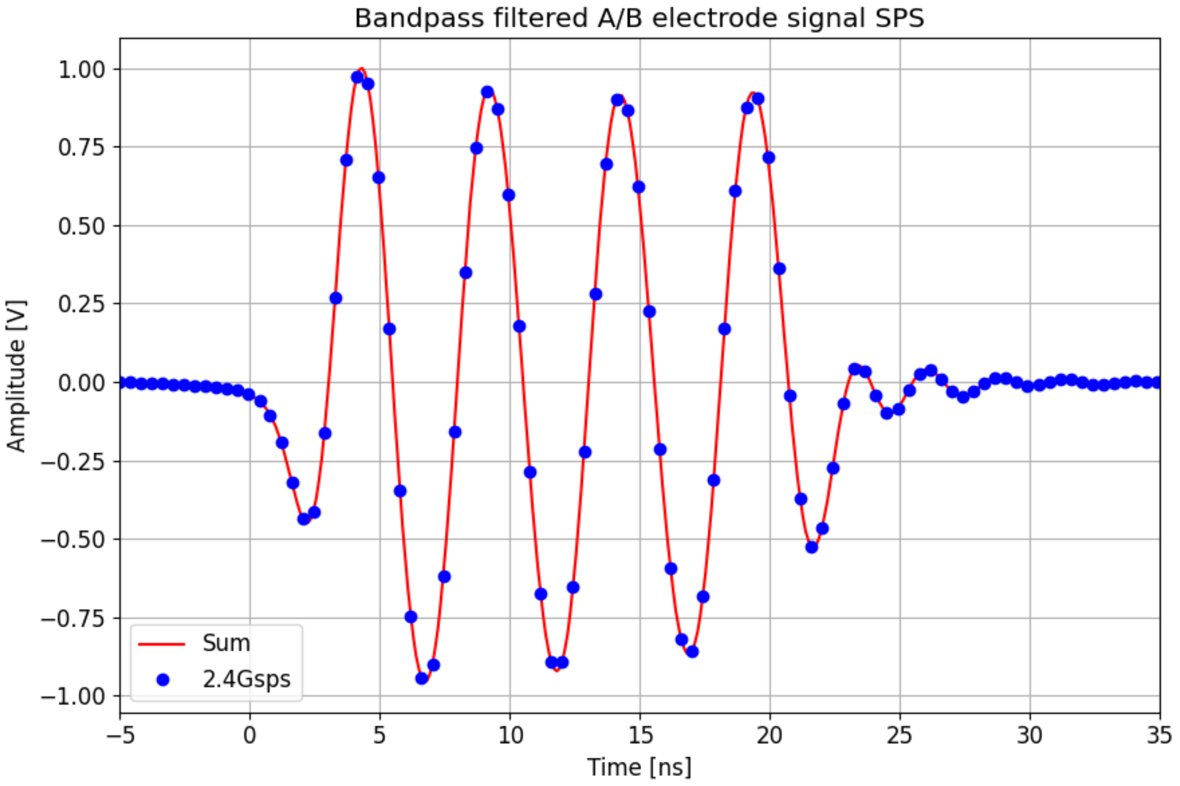
Pickup simulation and analysis
Manfred Wendt, CERN SY/BI

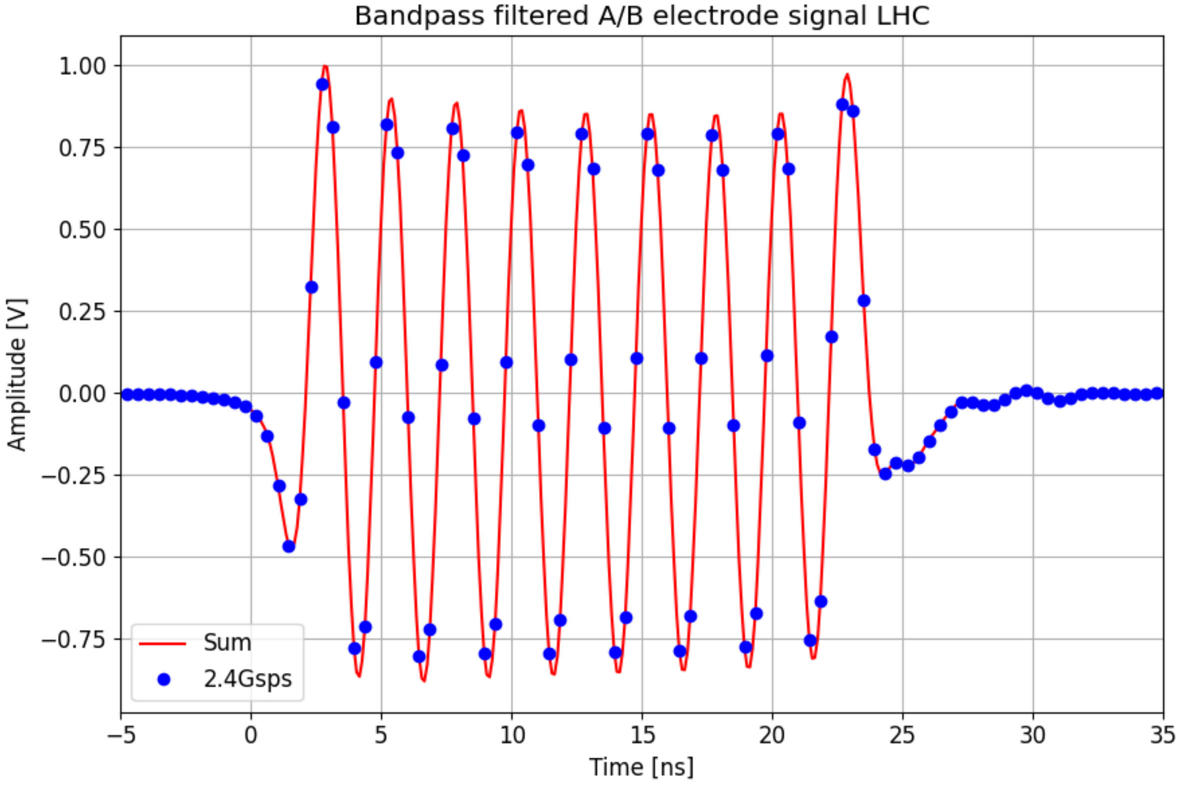


Towards a new, very low noise hardware

2a) Direct sampling of a band-pass filtered A and B signals by high speed digitizers.

2.5 Gsps provides ~30 useful samples. With ENOB ~10 bits we gain only 2-3 bits. Not enough.

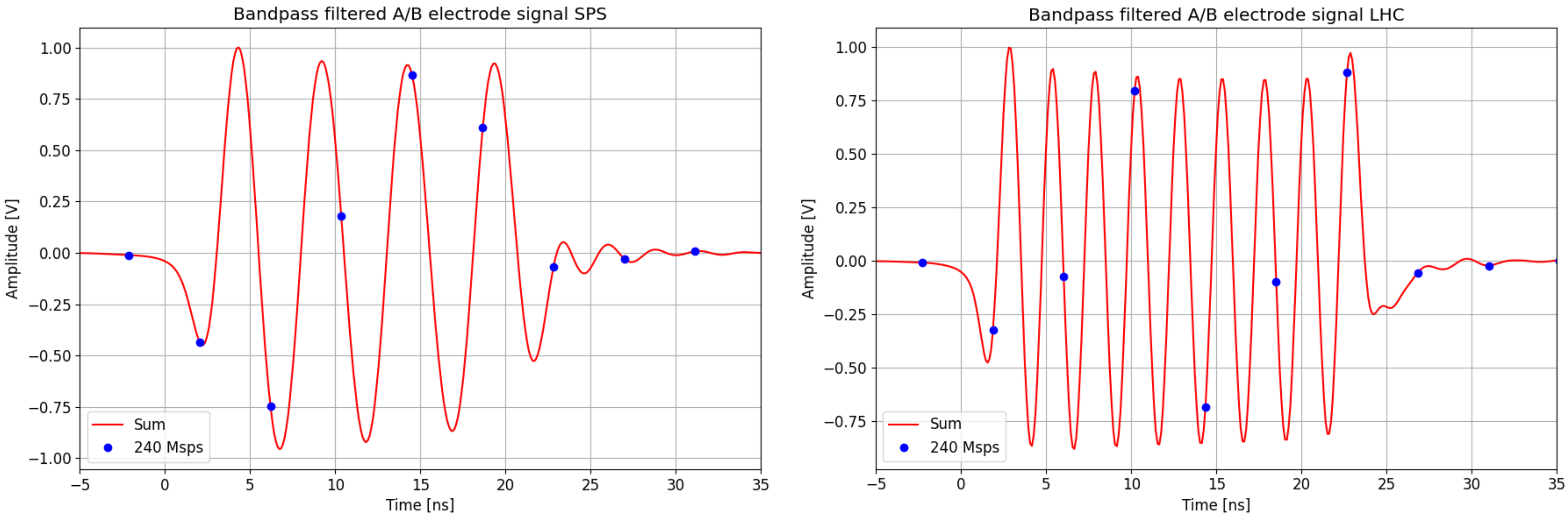




Towards a new, very low noise hardware

2b) Direct sampling of a band-pass filtered A and B signals by high resolution, medium speed digitizers.

240 Msps provides ~3 useful samples. With ENOB ~14 still not enough resolution for A-B calculation



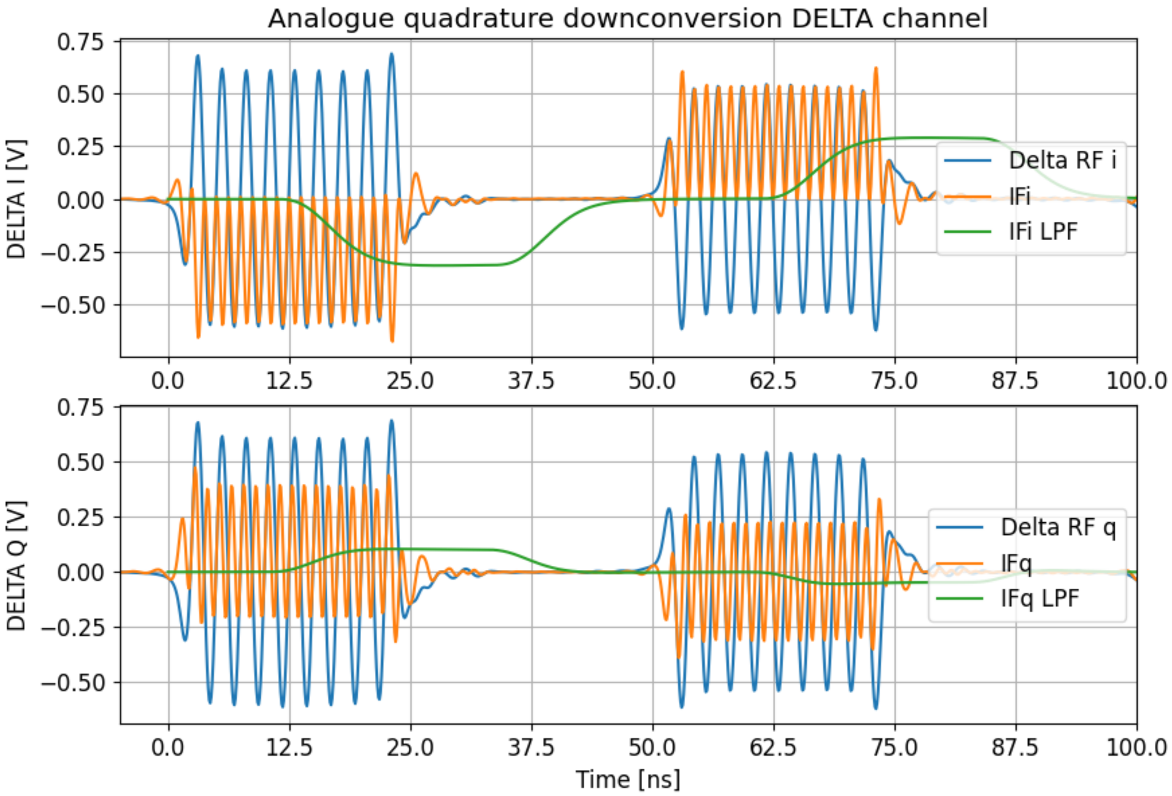
Towards a new, very low noise hardware

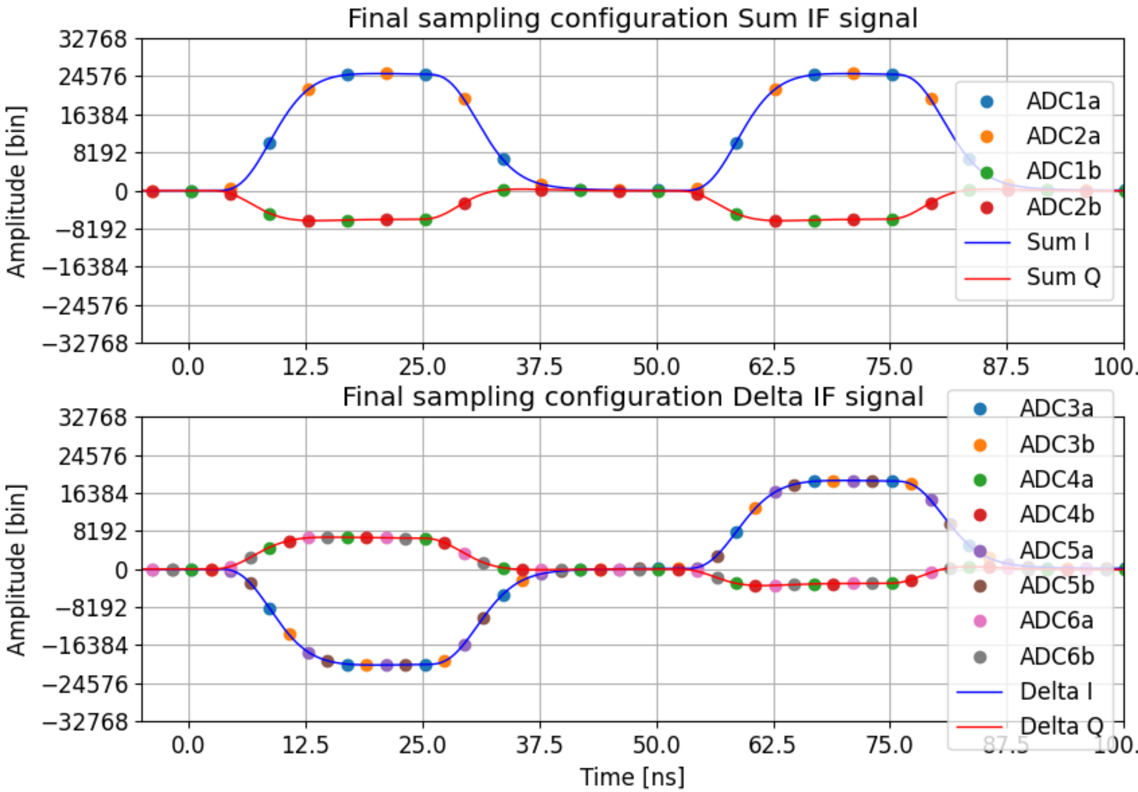
3) **Direct sampling of a band-pass filtered Σ and Δ signals by high resolution, medium speed digitizers.**

Use analogue hybrid to calculate the Δ signal. Direct sampling by 16-bit (ENOB 13-14 bits), 240 Msps converters would provide about the same performance as we have now.

Towards a new, very low noise hardware

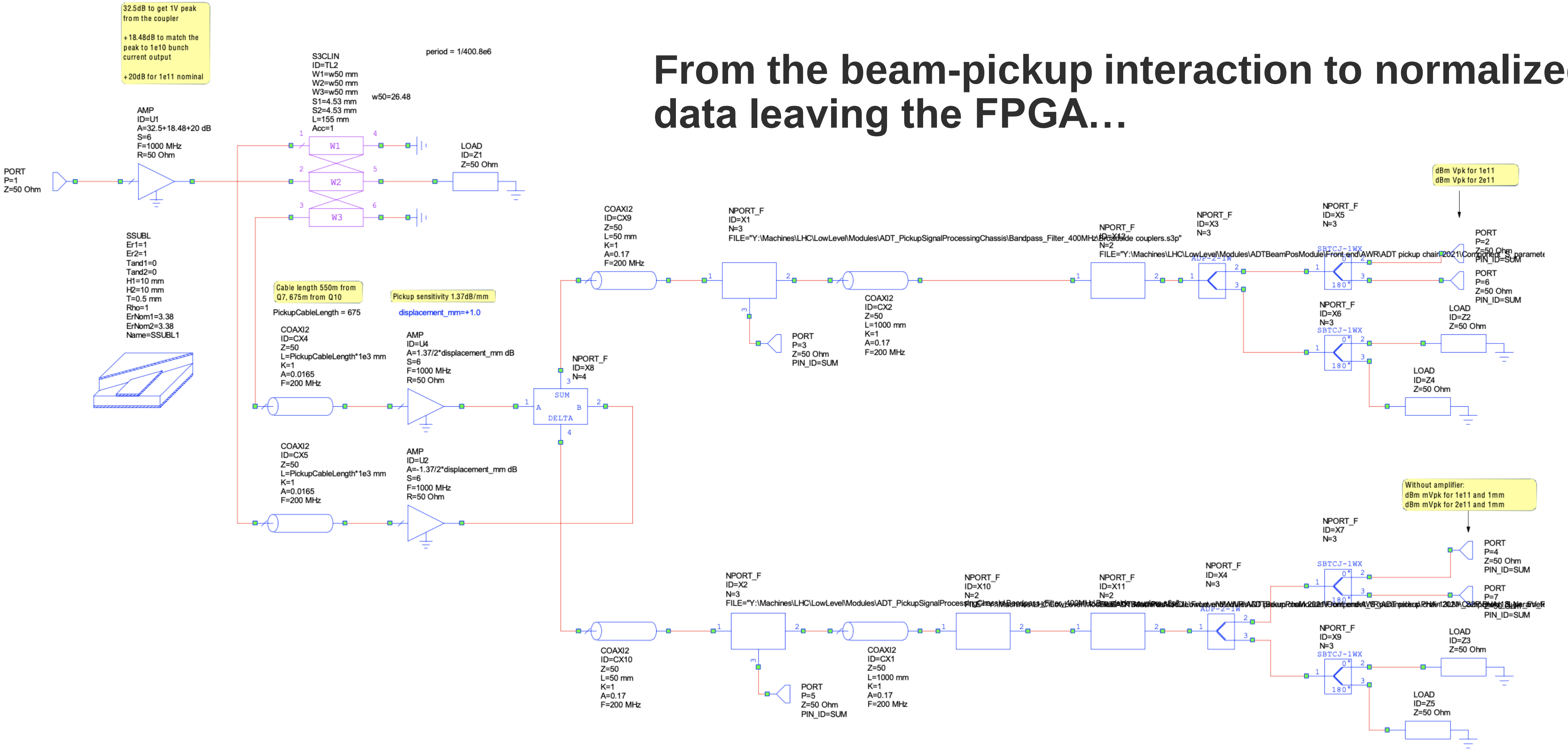
4) **Continue using the super-heterodyne principle and high resolution, medium speed digitizers, like the old beam position measurement system, but "super-optimize everything possible".**





Complete, multi physics model of the new system

From the beam-pickup interaction to normalized position data leaving the FPGA…



Features of the new system

Ideally connect the pickup directly to the ADC input…

- **Use the maximum of available signal power from the pickups**
- **Eliminate all unnecessary components in between**
- **Thorough analysis and optimization of the signal levels for each beam type**

New concept of fully differential, quadrature RF receivers

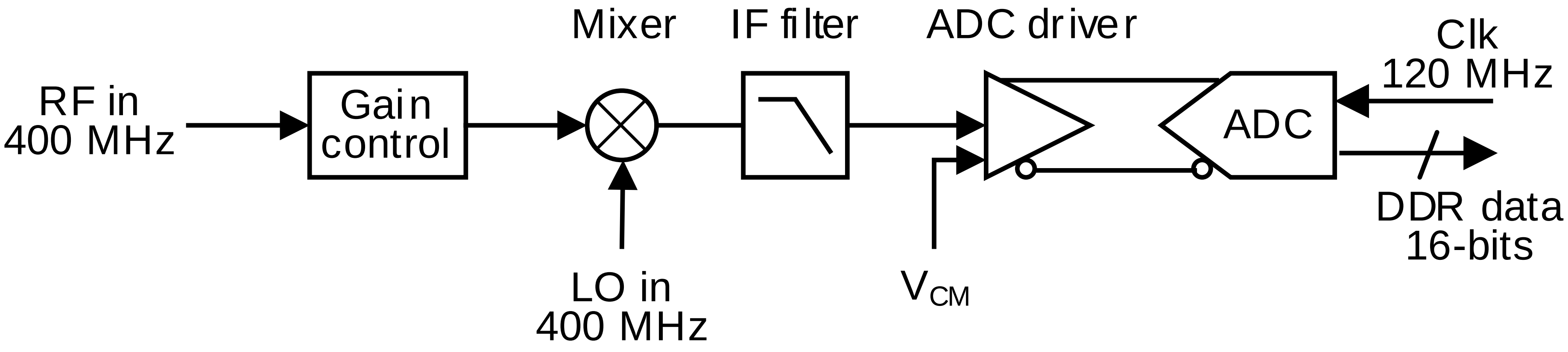
New ADCs. FPGA can interface up to six, dual channel ADCs (pin constraints)

- **Was 40 Msps/16-bits (1 sample per bunch passing)**
- **Now 120 Msps/16-bits + interleaved sampling to obtain 240 Msps for Σ and 480 Msps for Δ (6/12 samples)**

New signal processing

- **Use available information from multiple turns to further improve S/N of the position information**

General digitizing RF receiver architecture



Non-exhaustive list of things to consider:

Input RF level
Input matching
Gain switching time
Gain control IP3 and noise figure
Mixer LO and RF levels
Mixer IP3

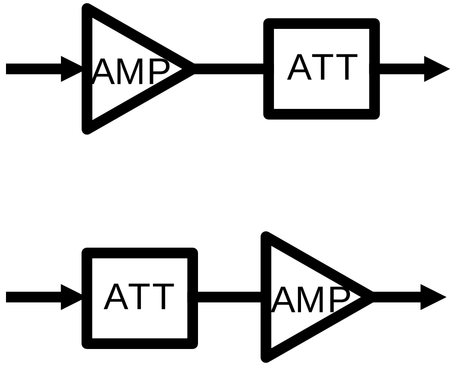
Mixer RF leakage
Mixer LO leakage
Mixer termination
Mixer wideband matching
IF amplifier frequency response
IF amplifier impulse response

IF amplifier IP3
Back-biasing through IF amplifier
ADC input impedance
ADC input level (differential)
ADC common mode voltage
ADC driver settling time

Input gain control: Noise figure of a cascaded system

Noise figure of a cascaded system $F_{total} = F_n + G_n \cdot \{F_{n-1} + G_{n-1} \cdot [\ \ldots\ F_3 + G_3 \cdot (F_2 + G_2 \cdot F_1)]\}$

Attenuator gain (dB)	Attenuator NF (dB)	Amplifier gain (dB)	Amplifier NF (dB)	Total gain (dB)	Total NF ATTN+AMP (dB)	Total NF AMP+ATTN (dB)
0	0	+22	1.1	+22	1.1	1.1
-2	2	+22	1.1	+20	3.1	1.112
-4	4	+22	1.1	+18	5.1	1.132
-6	6	+22	1.1	+16	7.1	1.163
-10	10	+22	1.1	+12	11.1	1.287
-15	15	+22	1.1	+7	16.1	1.707
-20	20	+22	1.1	+2	21.1	2.817

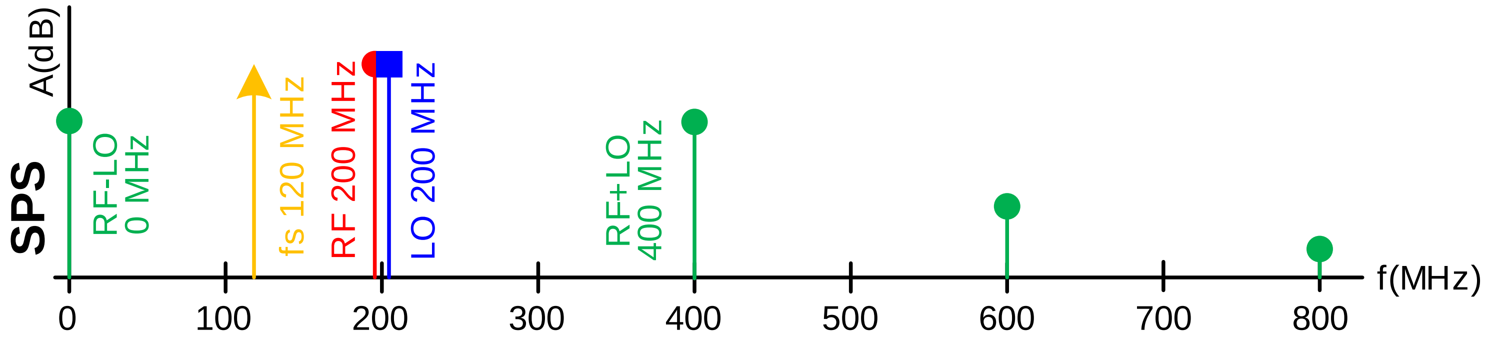


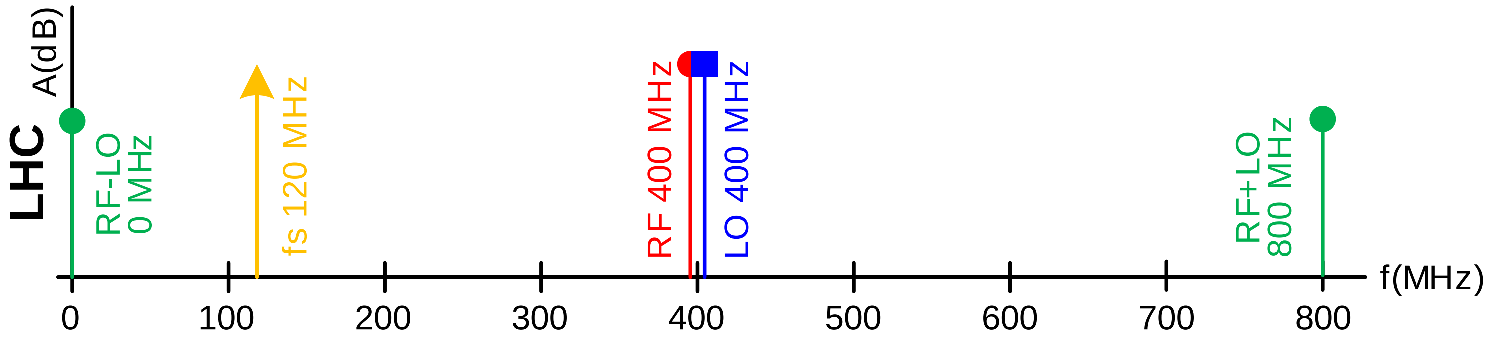
But we need very high P1dB/IP3 amplifier to work in this configuration (we used MiniCircuits TSS-13LN+, G = 22dB, NF = 1.1dB, P1dB = +24dBm)

IF filter+amplifier considerations

Whole signal chain much have impulse response shorter than the bunch spacing (<25 ns)

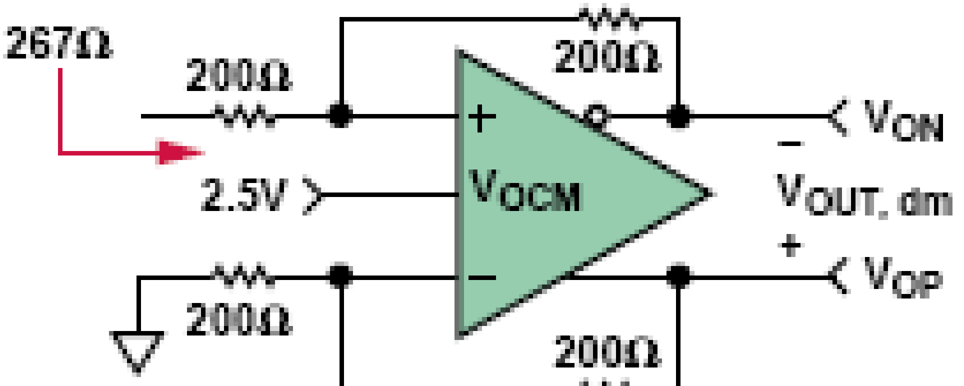
Good suppression of all mixing and leakage products. No ringing. ADC input is switched capacitor type of load. IF filter is very difficult to impossible…

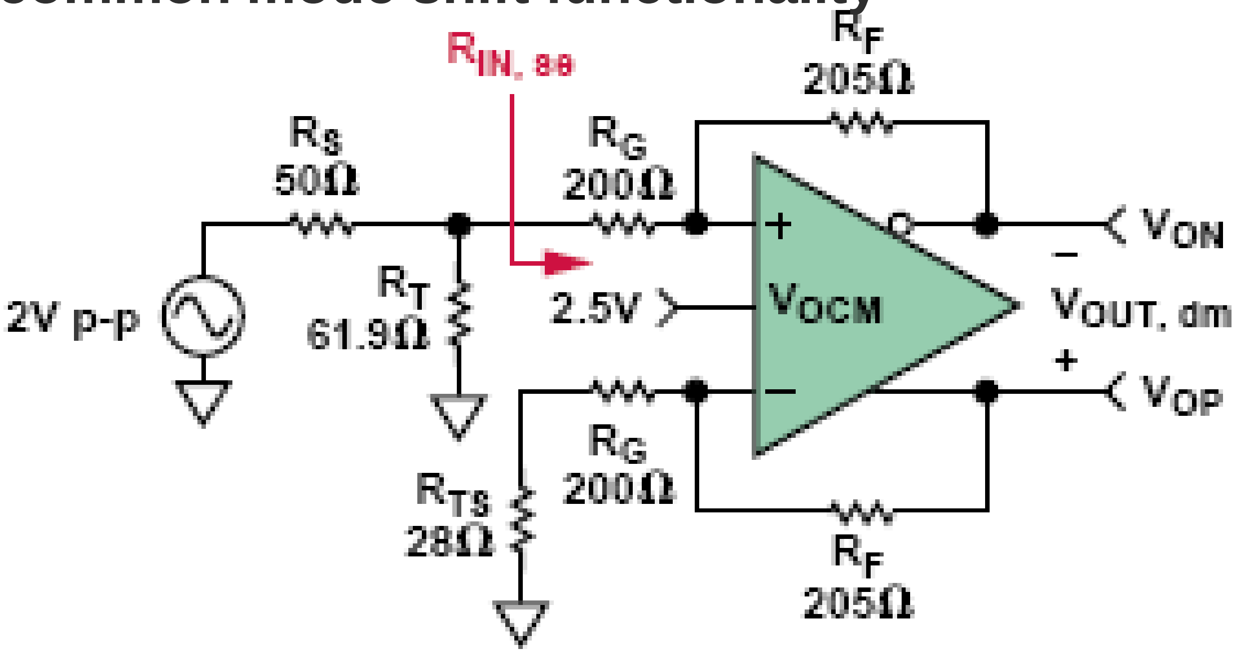




Fast ADC driver with DC-coupled path

Single ended to differential driver with common mode shift functionality





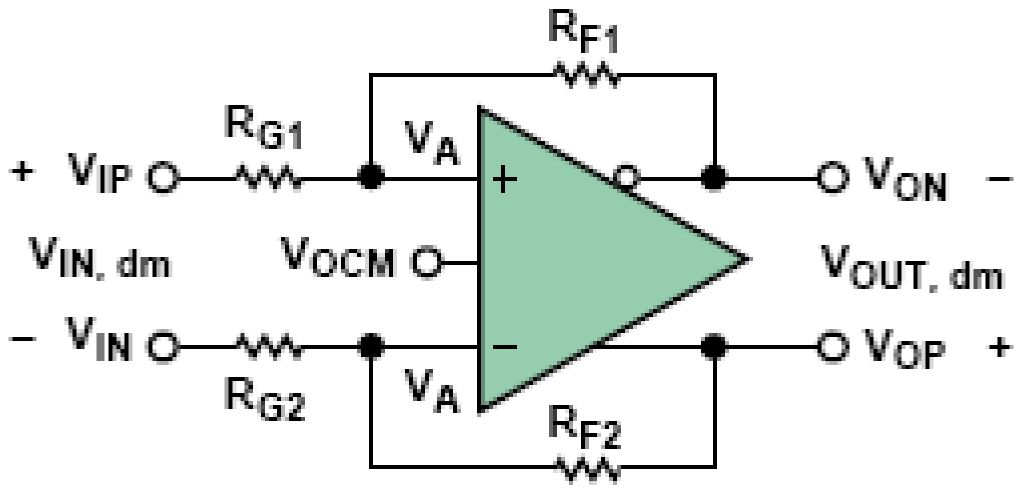
Input impedance is difficult. For proper treatment of both DM and CM we need perfectly balanced circuit.

Back biasing of the source from V_{CM} via the feedback resistors!

"Rules of the Road" for High-Speed Differential ADC Drivers
https://www.analog.com/en/analog-dialogue/articles/rules-for-high-speed-differential-adc-drivers.html

Fast ADC driver with DC-coupled path

Differential to differential driver with common mode shift functionality



Fully differential driver is much better. Input impedance defined by R_{G1}/R_{G2} and no signal power is wasted in termination resistors.

Still problem with back biasing of the source from V_{CM} via the feedback resistors!

"Rules of the Road" for High-Speed Differential ADC Drivers
https://www.analog.com/en/analog-dialogue/articles/rules-for-high-speed-differential-adc-drivers.html

Noise contribution of the IF/ADC driver amplifier

LTC6409 10GHz GBW, 1.1nV/√Hz Differential Amplifier/ADC Driver

- **Goal to keep the contribution of the ADC driver <0.5 LSB_{RMS}**

  → Gain must be very low (<6 dB)

- **We need high output level from mixers**
- **Preferably use the Ri resistors as signal termination**
- **Use 0.1% thin film resistors for good CMRR and lower current noise**

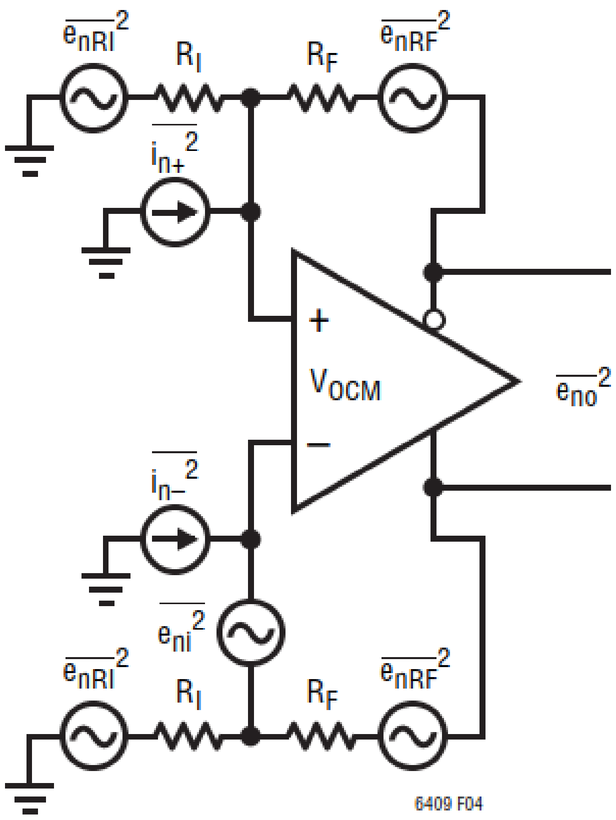


Figure 4. Simplified Noise Model

"Rules of the Road" for High-Speed Differential ADC Drivers
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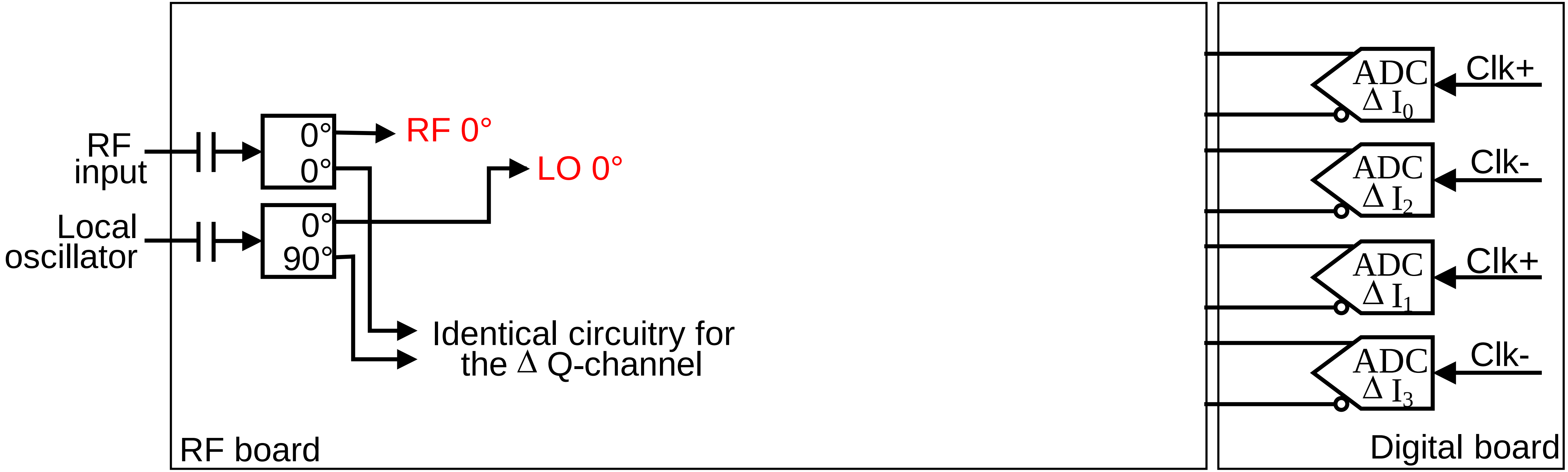
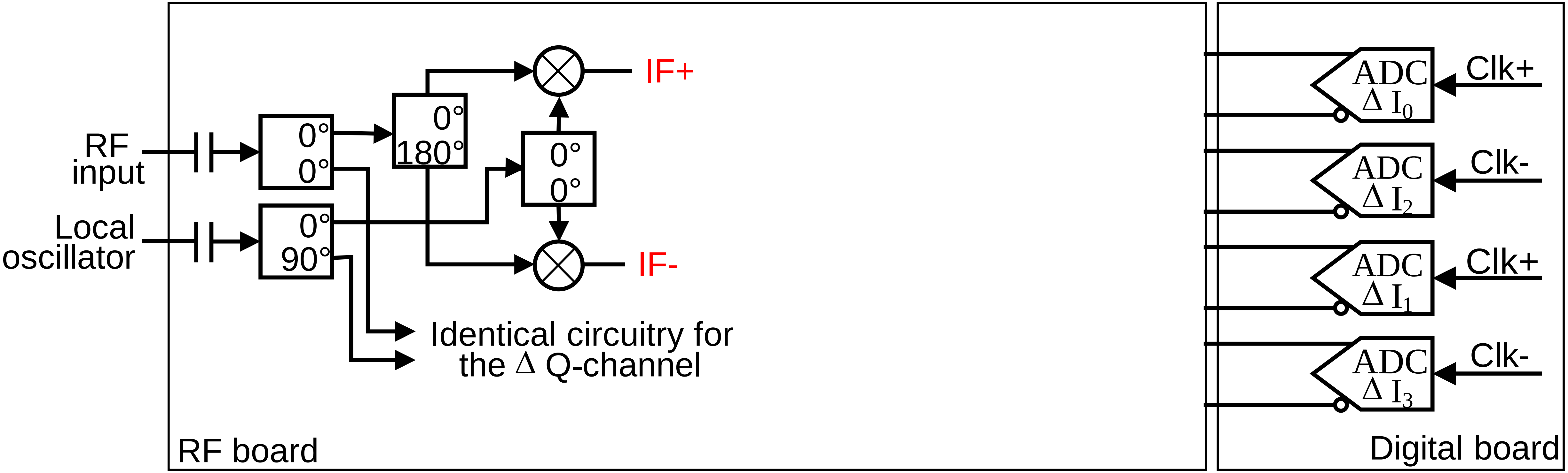
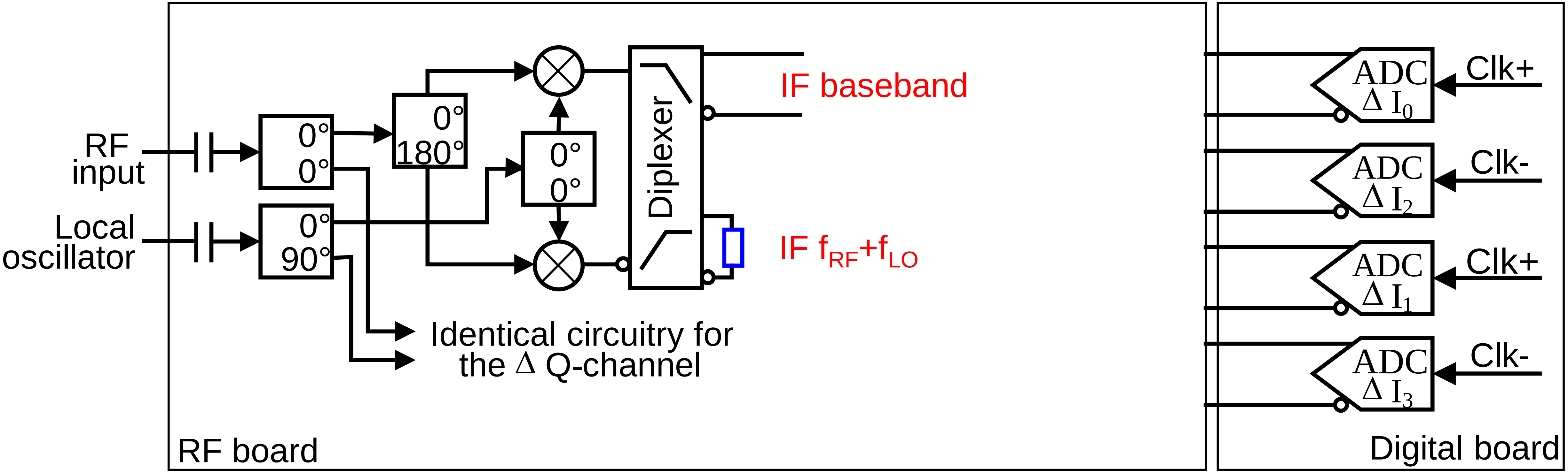
Fully differential receiver and interleaved ADC driver



Fully differential receiver and interleaved ADC driver



Fully differential receiver and interleaved ADC driver



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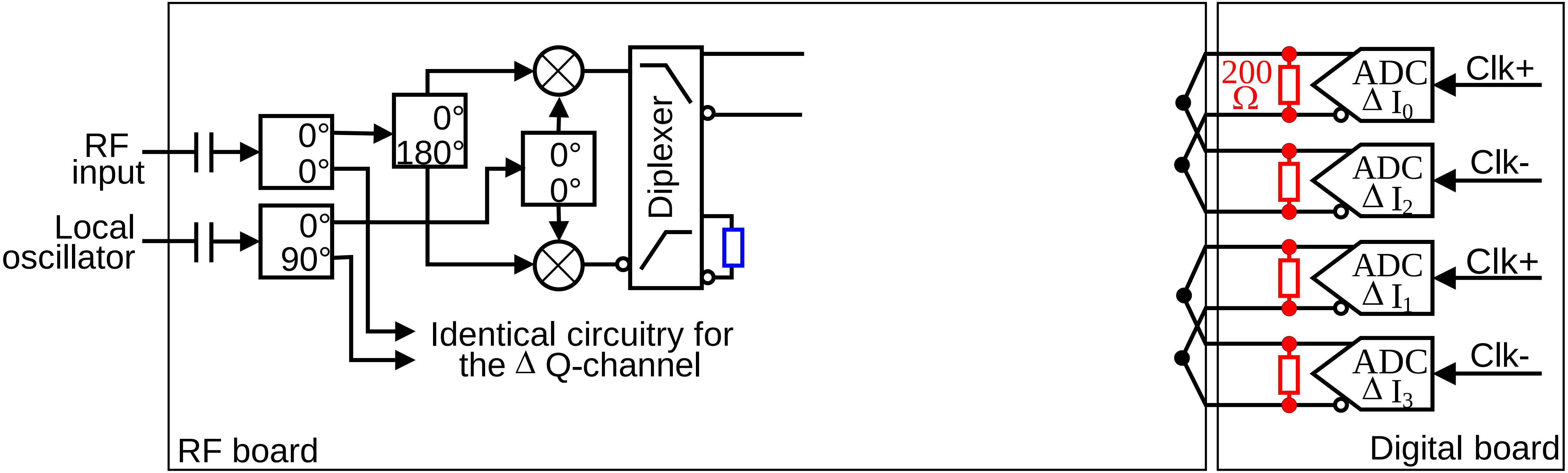

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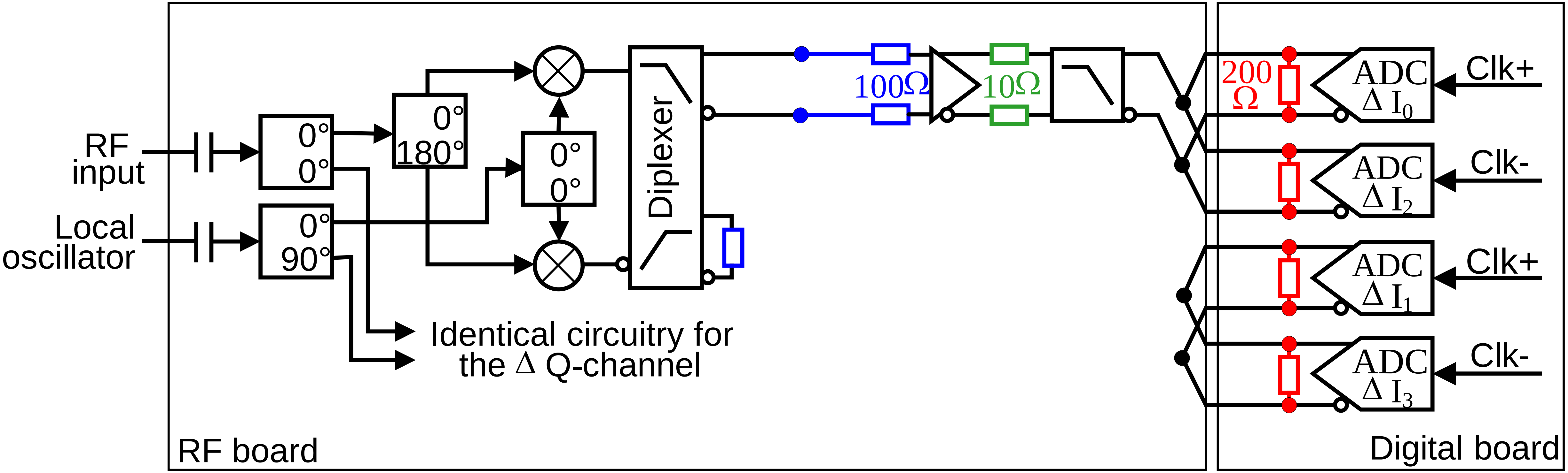

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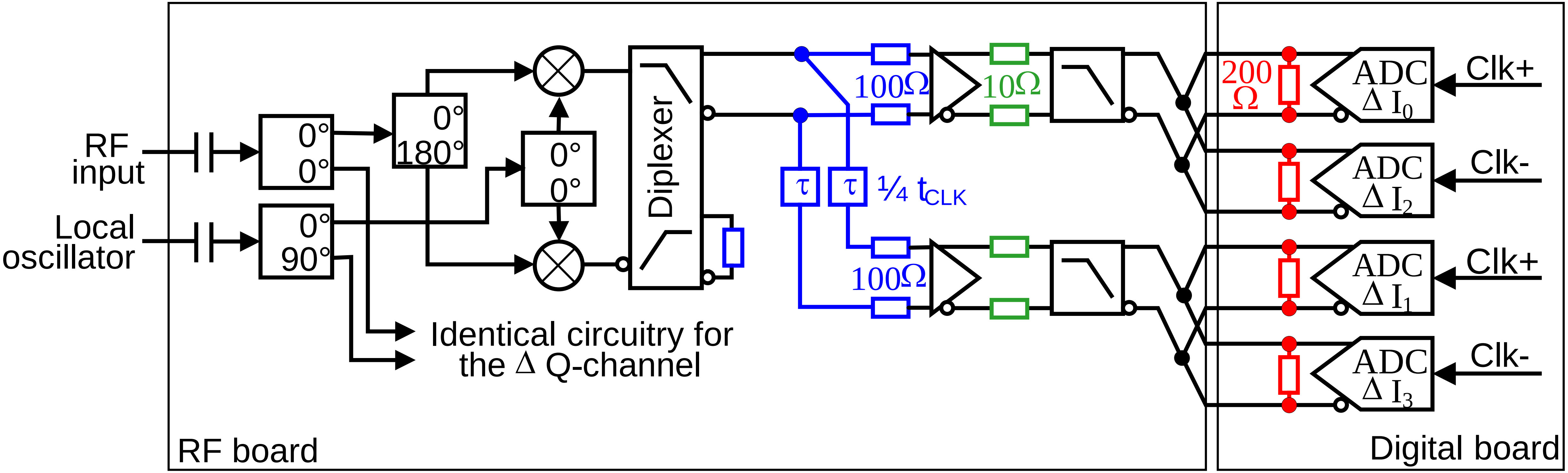
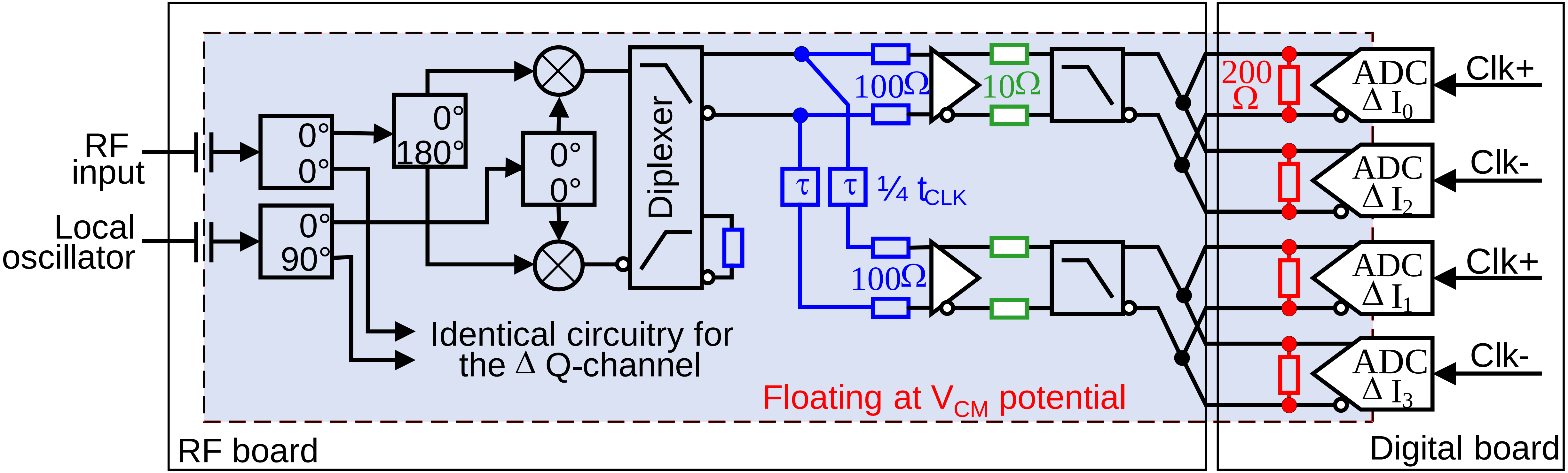
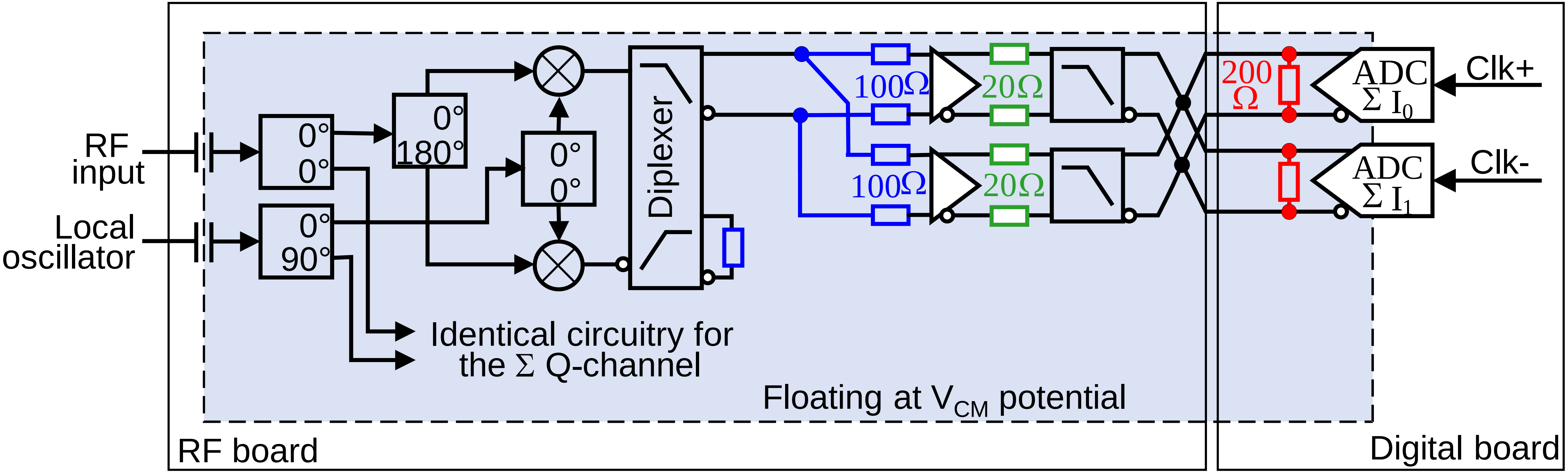


Fully differential receiver and interleaved ADC driver

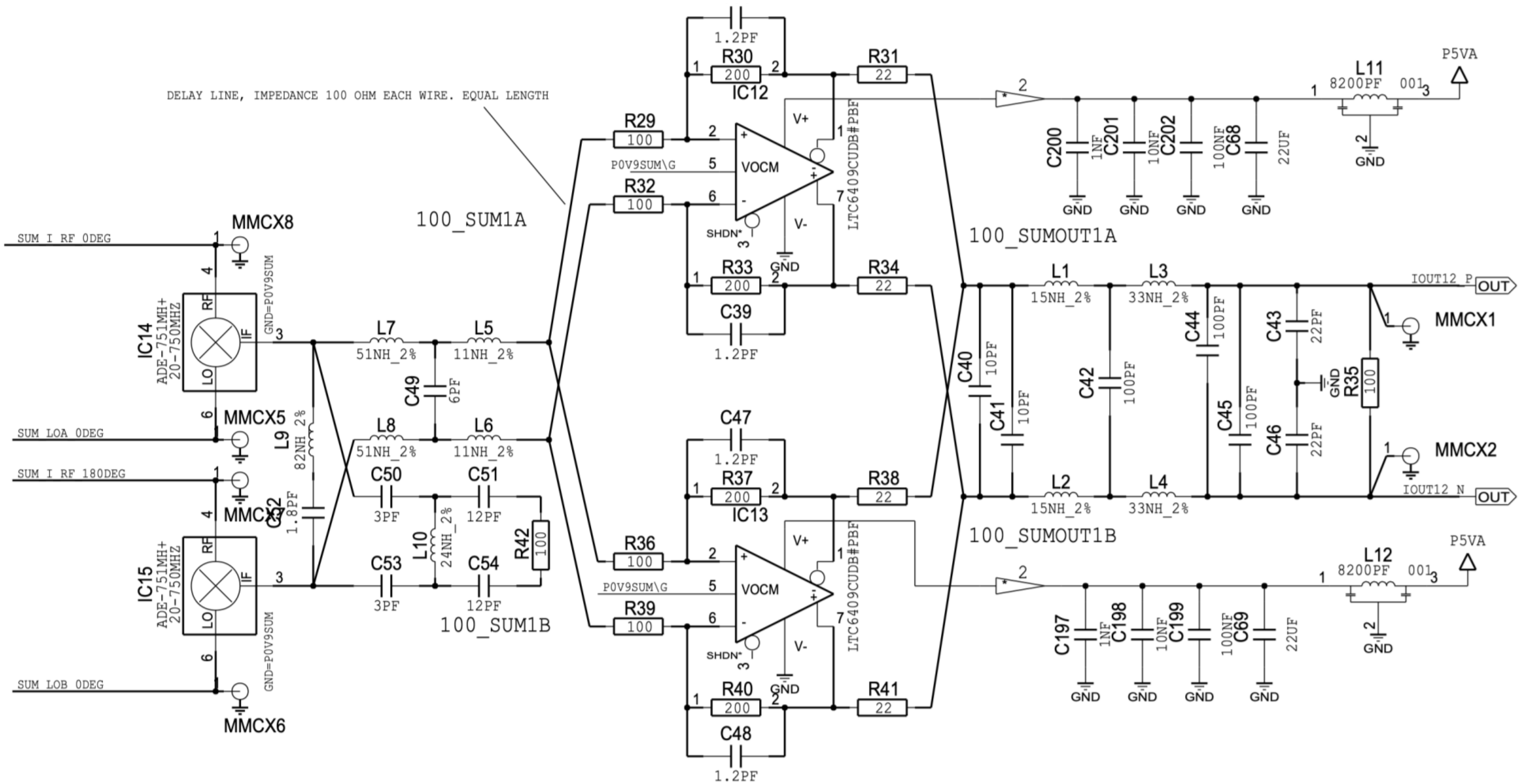


Fully differential receiver and interleaved ADC driver



Fully differential receiver and interleaved ADC driver

All this would work only if the impedances and delays are tightly controlled and everything is perfectly symmetrical. Not an easy job for the PCB designer. Thank you William!



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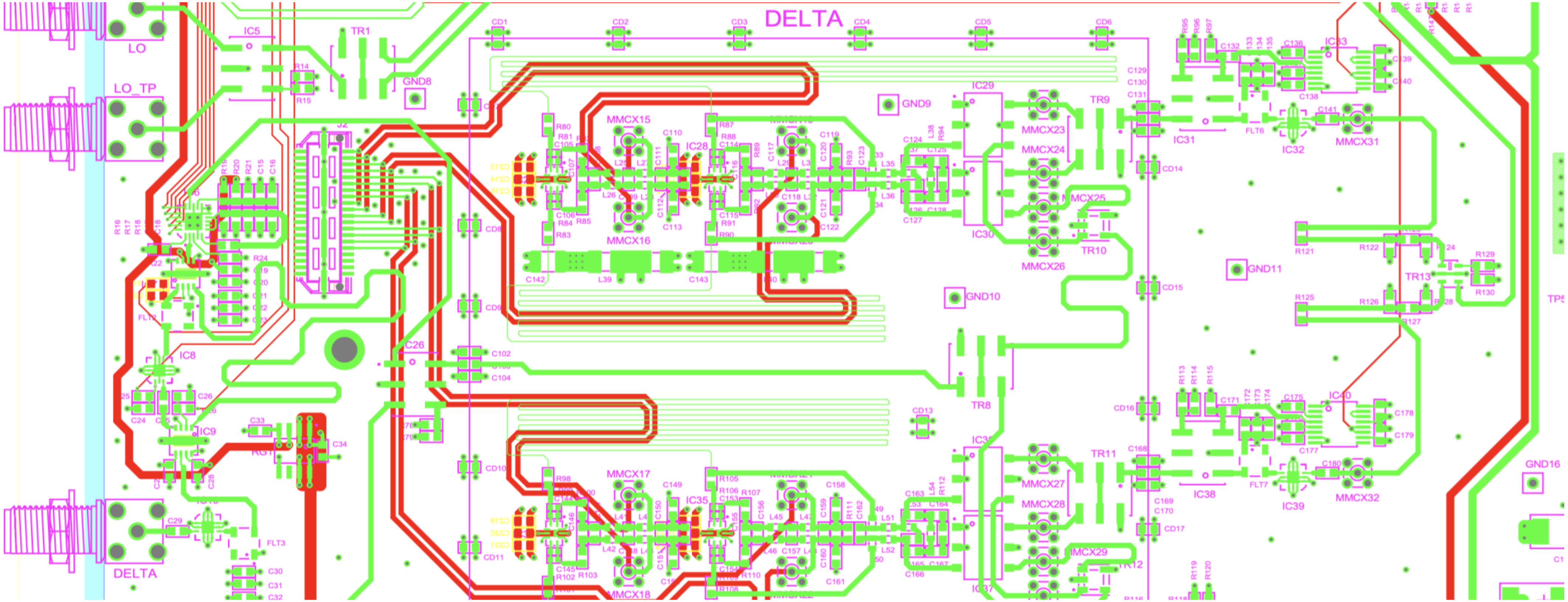
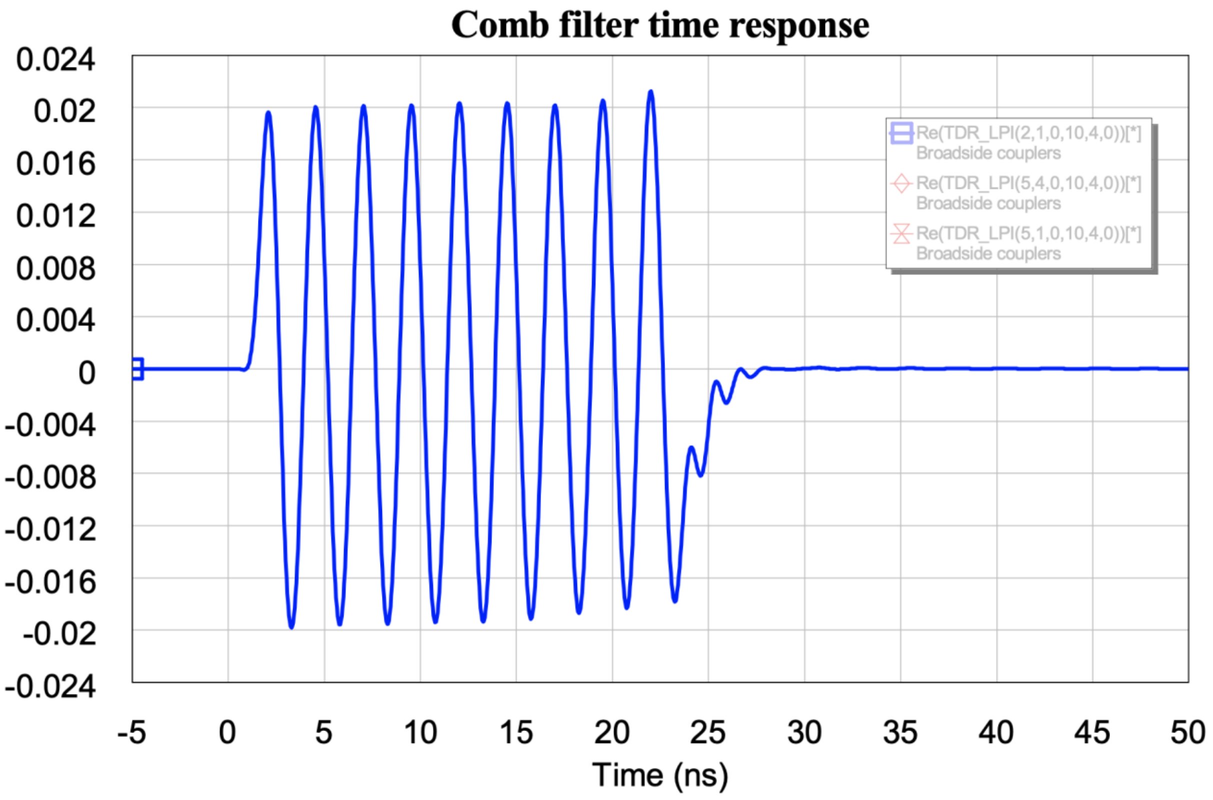
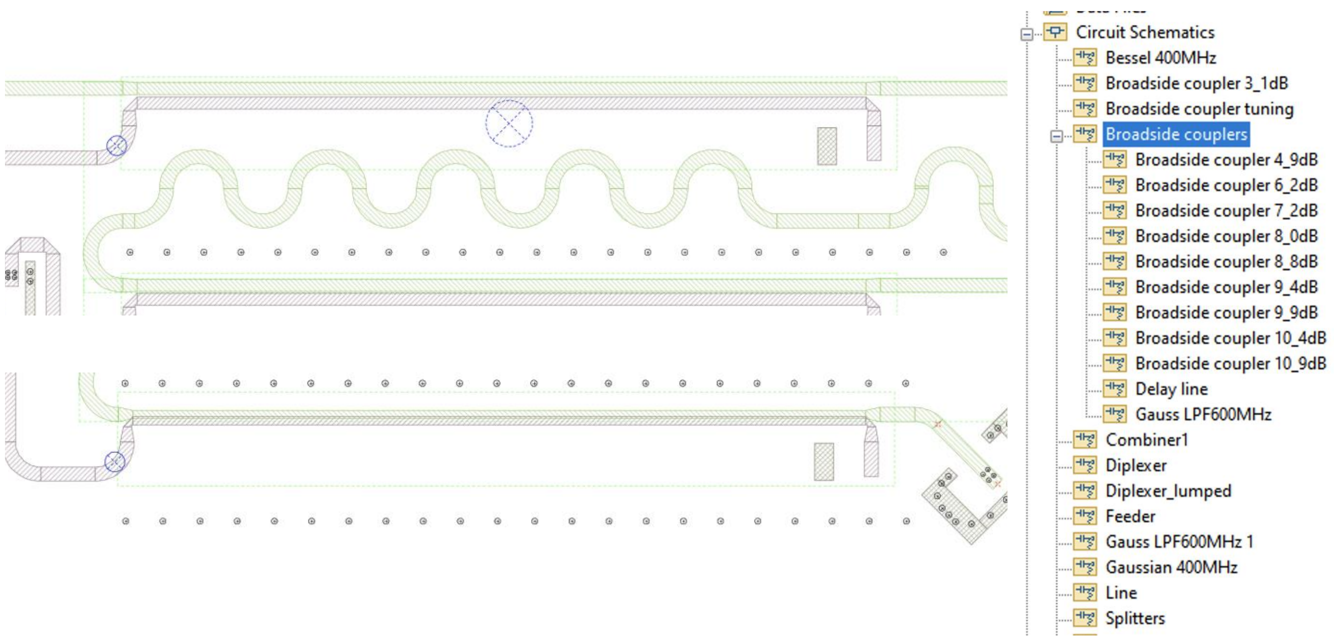


RF bandpass filter with tightly controlled impulse response

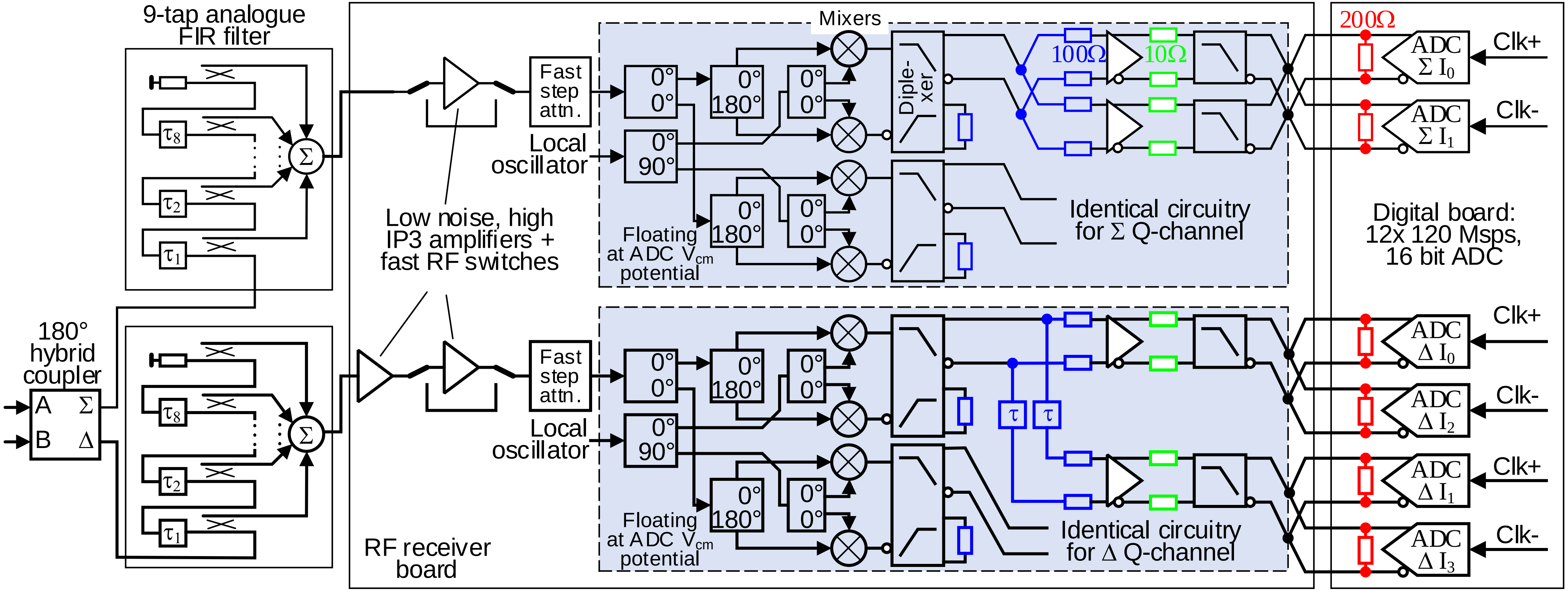
Optimized for maximum transmission at fc. We have gained >10dB of pickup signal power.



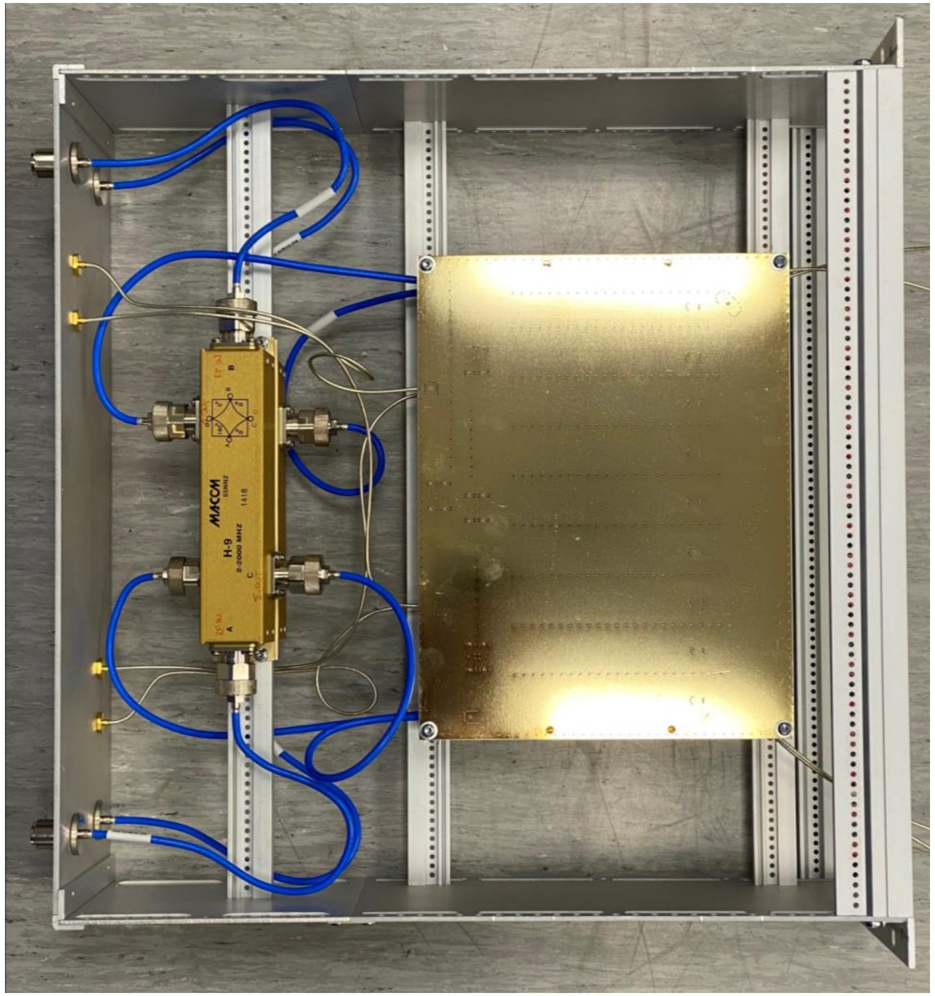


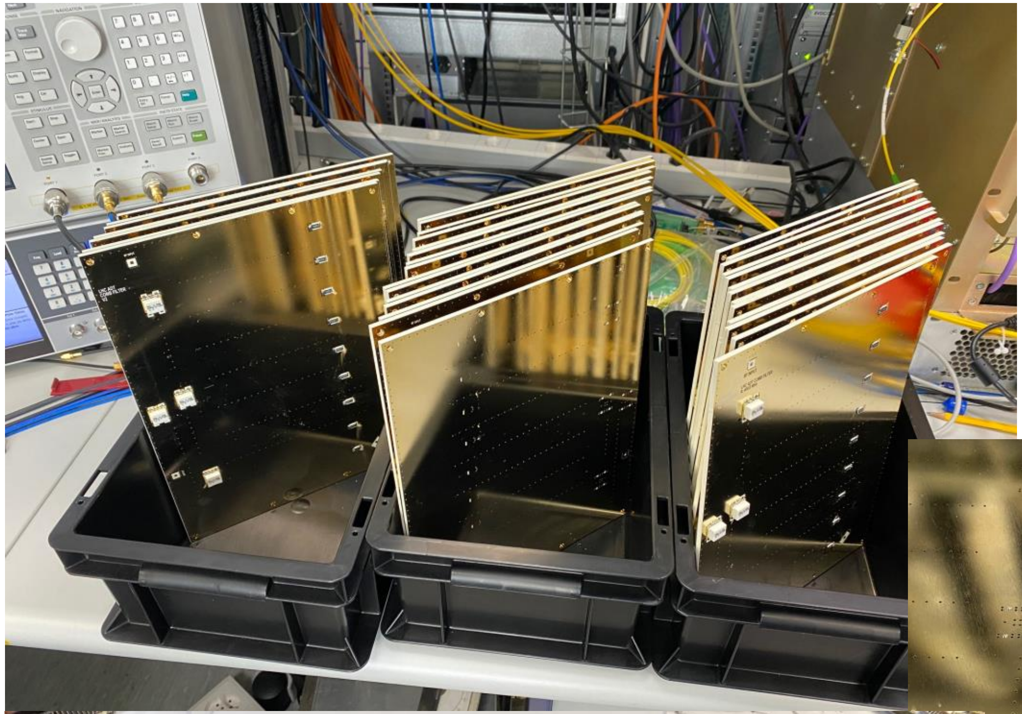
A full overview of the new Beam Position Measurement system.

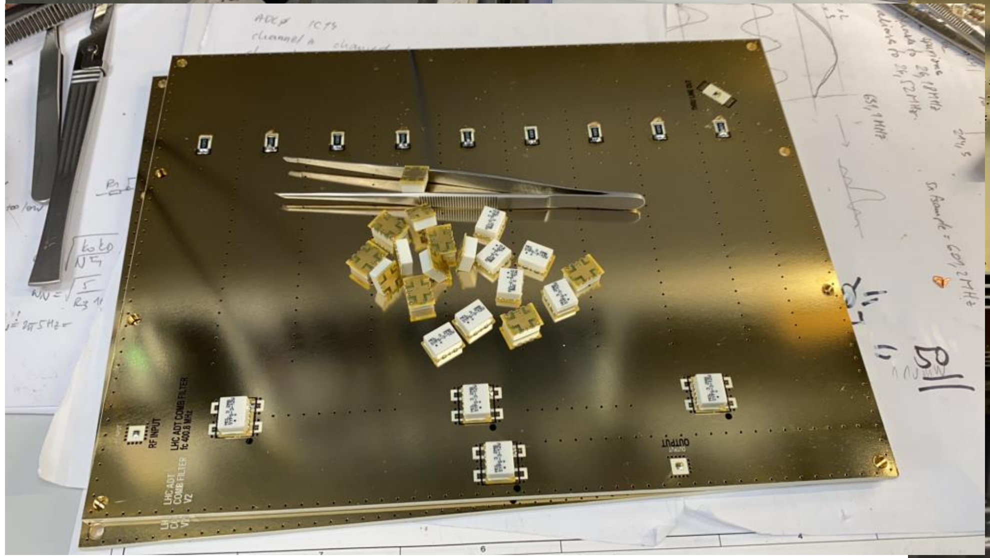
FPGA can interface maximum six, dual channel ADCs (pin constraints):

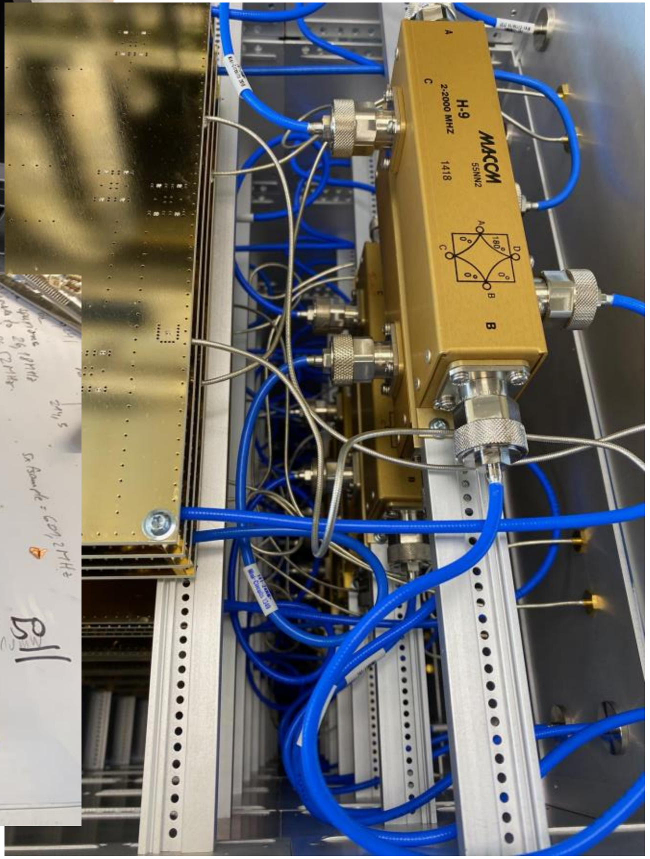


New hardware









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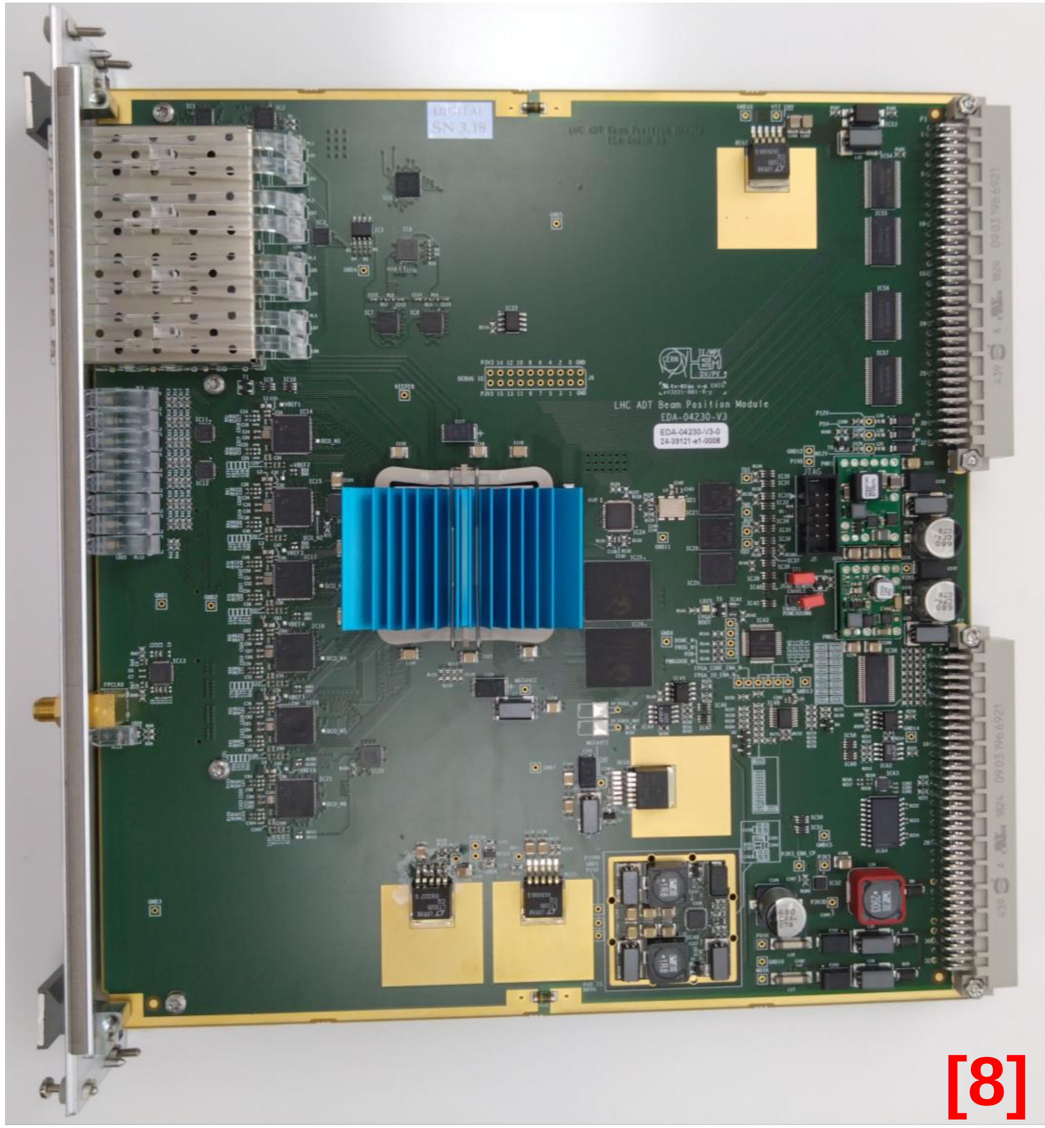

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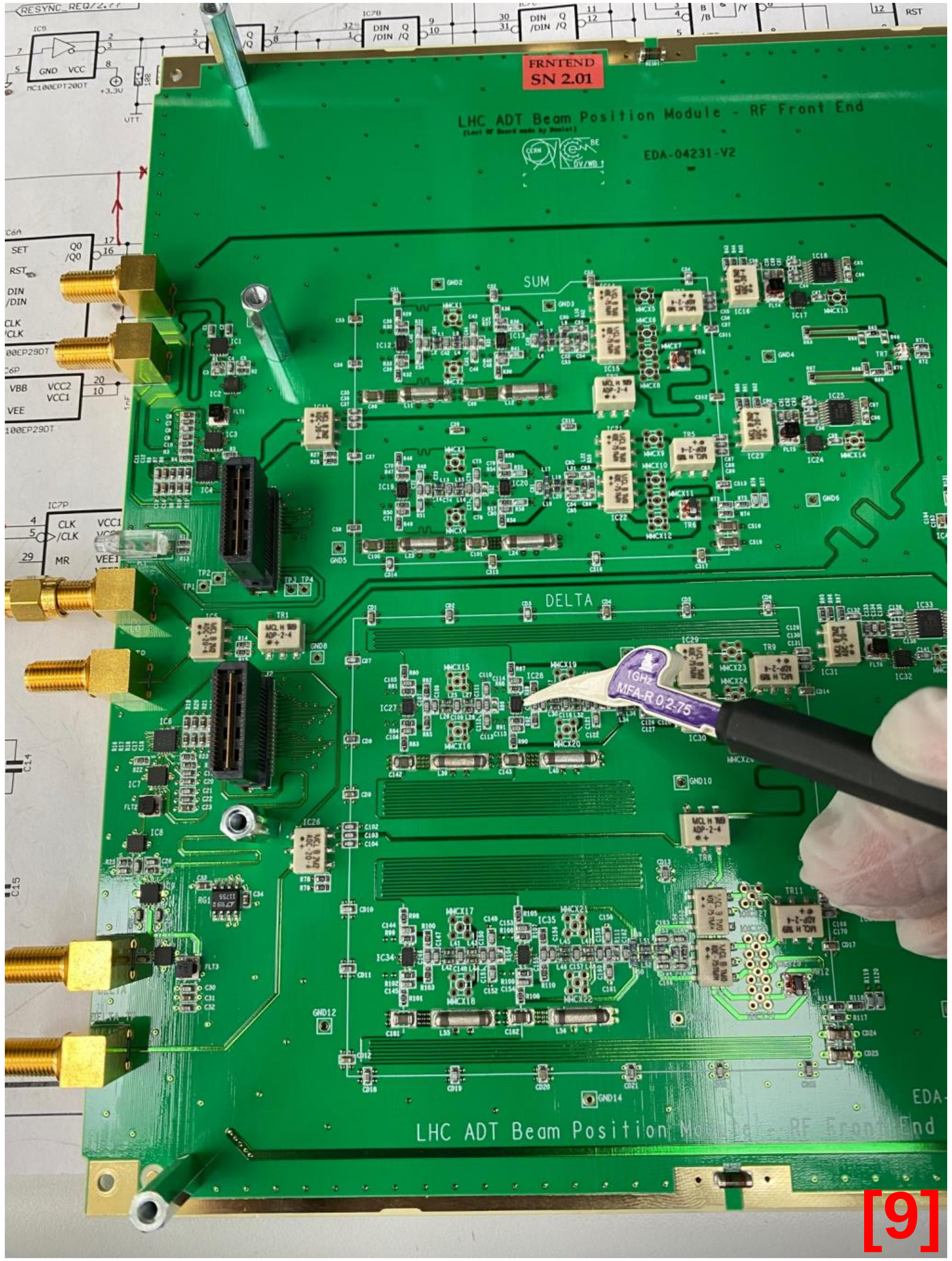
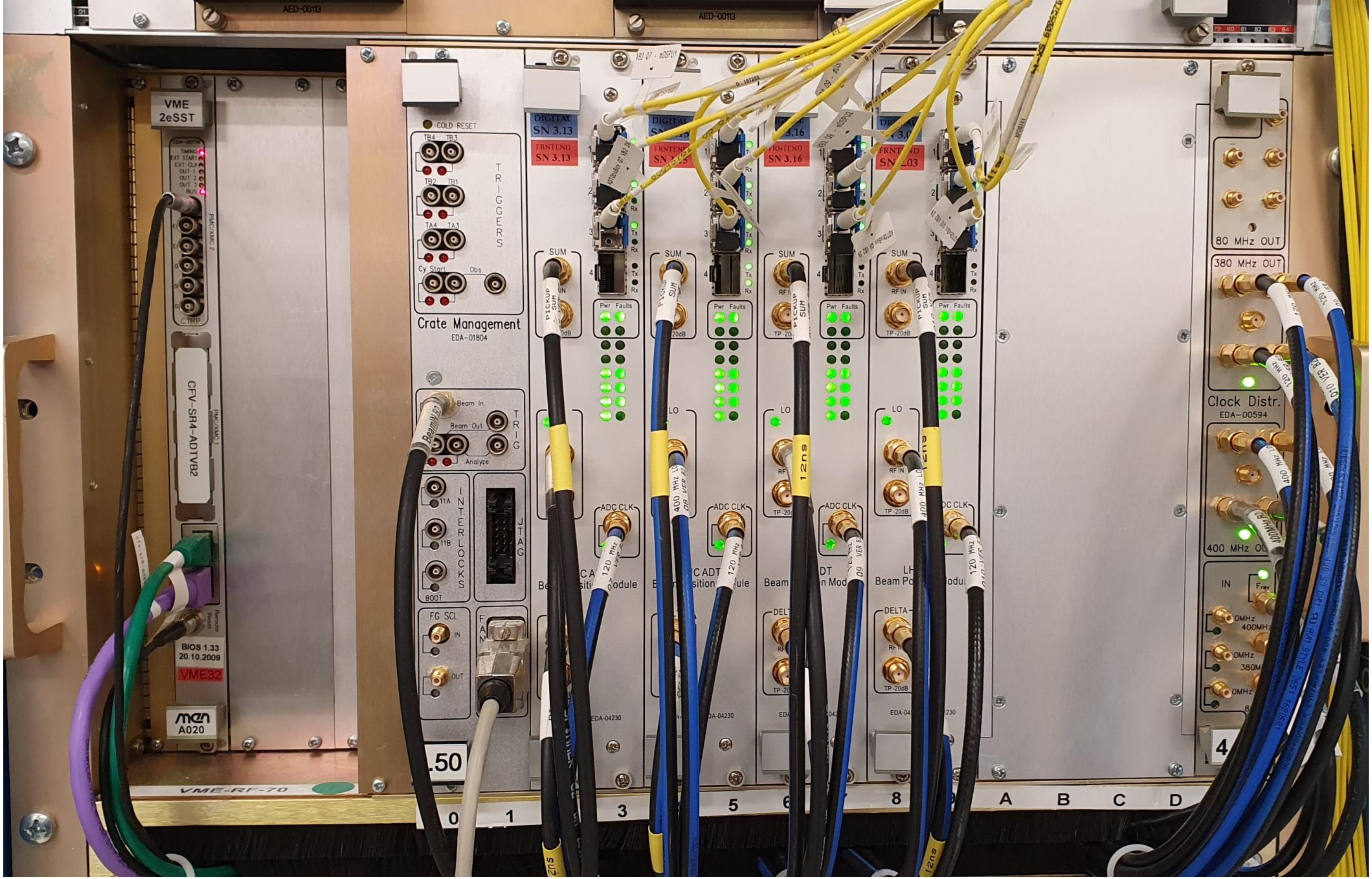


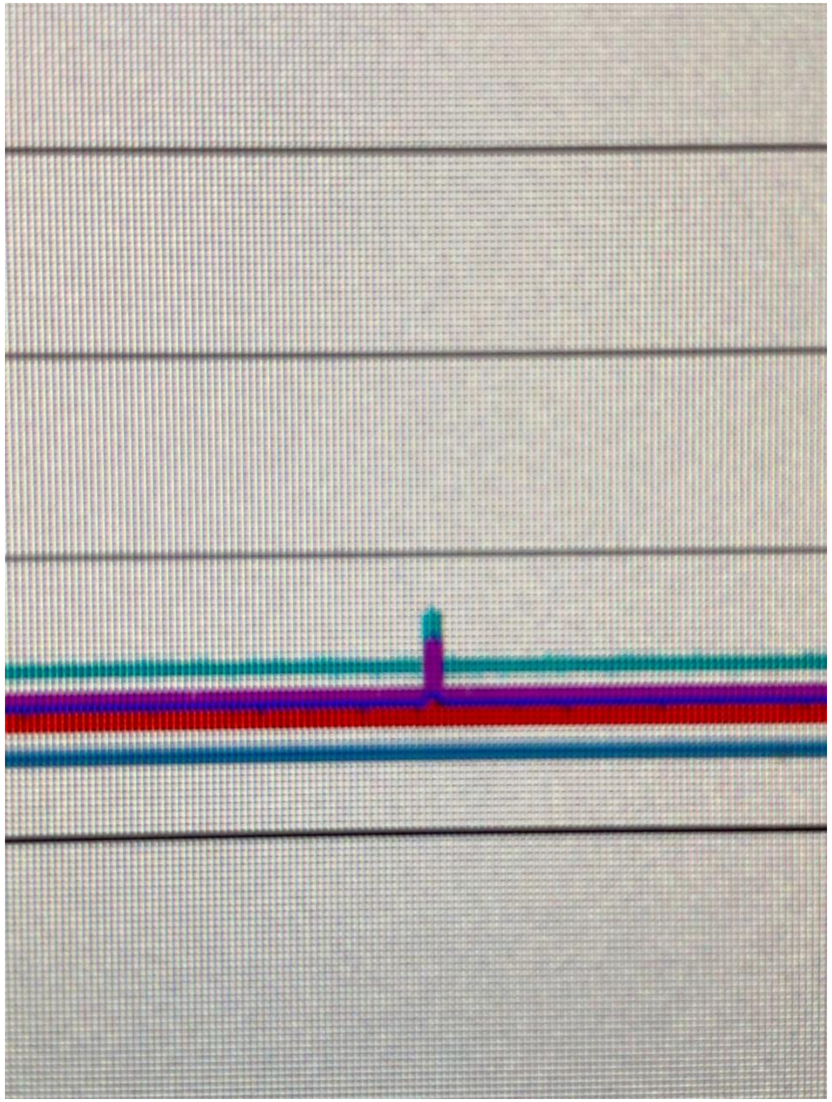
[9]

New system for one beam and one plane (4 pickups)



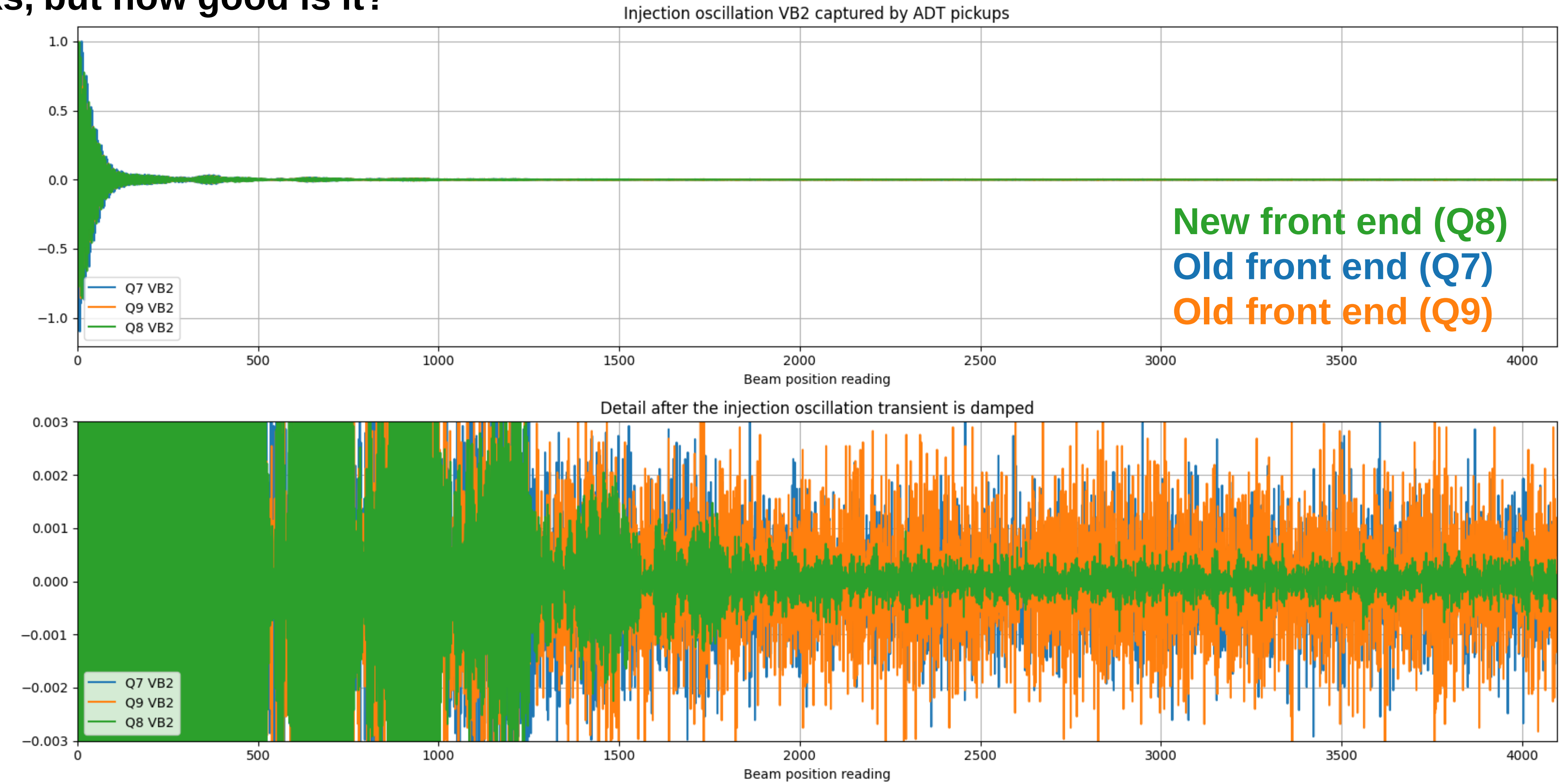
But will it work with beam?

LHC beam test.
First circulating bunch after 3 years of shutdown.
19.10.2021, 19:36:51

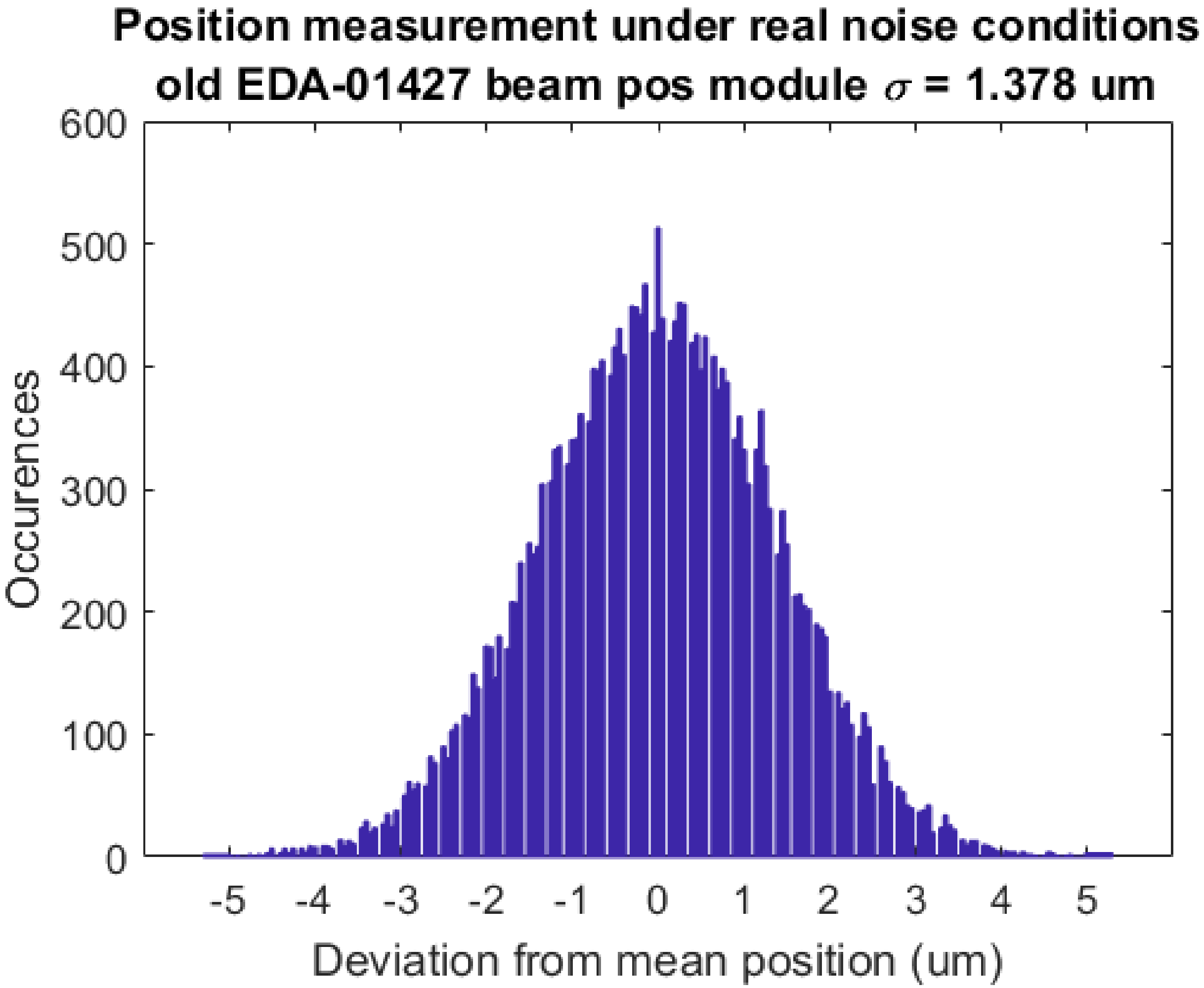


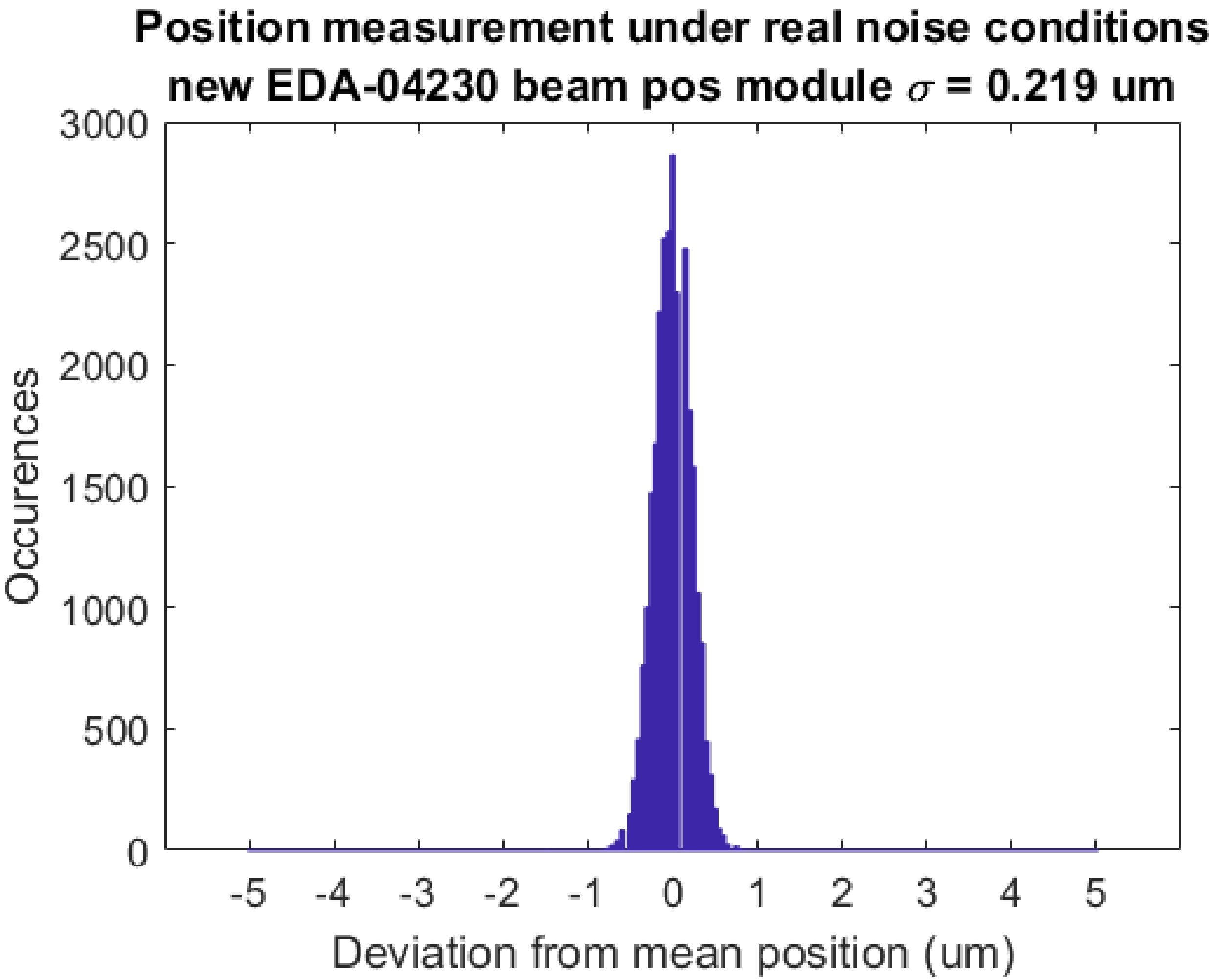
But will it work with beam?

25.10.2021 - The very first injection oscillation damping with all new ADT pickups fully set up.
It works, but how good is it?



Obtained results: New BPM noise performance





References

[1] D. Valuch and V. Stopjakova, “New Generation of Very Low Noise Beam Position Measurement System for the LHC Transverse Feedback”, in Proc. 13th Int. Particle Accelerator Conf. (IPAC'22), Bangkok, Thailand, Jun. 2022, pp. 849-852. doi:10.18429/JACoW-IPAC2022-TUPOST007

[2] Buffat, X. and Herr, W. and Pieloni, T. and Valuch, D., “Modeling of the emittance growth due to decoherence in collision at the Large Hadron Collider, in Phys. Rev. Accel. Beams 23, 021002 (2020)

[3] S.V. Furuseth and X. Buffat, “Loss of transverse Landau damping by noise and wakefield driven diffusion, in Phys. Rev. Accel. Beams 23, 114401 (2020)

[4] P. Baudrenghien and T. Mastoridis, “Transverse emittance growth due to RF noise in the high-luminosity LHC crab cavities, in Phys. Rev. ST Accel. Beams 18, 101001 (2015)

[5] P. Baudrenghien, D. Valuch: Beam phase measurement and transverse position measurement module for the LHC. Poster at LLRF07 https://edms.cern.ch/ui/#!master/navigator/document?P:1126834229:1854519948:subDocs

[6] Boris Murmann: Energy Limits in A/D Converters IEEE paper (2013) https://ieeexplore.ieee.org/document/6577781

[7] Boris Murmann: Energy Limits in A/D Converters: https://indico.cern.ch/event/191624/attachments/273635/382982/murmann20120525cern.pdf

[8] LHC Beam Position Module, digital board https://edms.cern.ch/item/EDA-04230-V3-1/0

[9] LHC Beam Position Module RF front end https://edms.cern.ch/item/EDA-04231-V3-0/0

Conclusions

- **Noise floor of the transverse feedback system in LHC must be lowered by factor of two to four to be compatible with the beam operation in High-Luminosity LHC.**
- **TFB in LHC is fully digital, the noise is dominated by the beam position measurement noise.**
- **A new generation of very low noise receivers and redesigned signal path was researched and implemented during LHC long shutdown 2 (2018-2021).**
- **A reduction of factor ~6.5 was achieved with the new generation hardware.**

Thank you for your attention

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