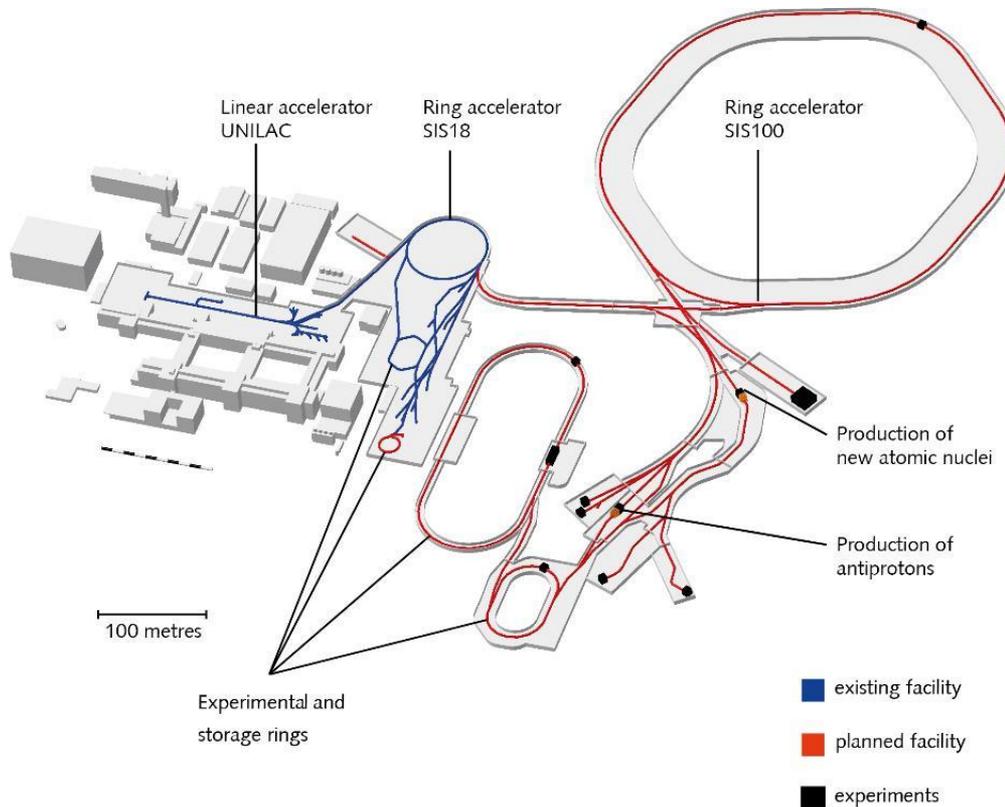
A detailed wireframe 3D model of a heavy-ion synchrotron and storage ring. The model shows a large, roughly oval-shaped main ring with several smaller, more complex sections branching off, including a large loop on the left and a series of smaller loops and structures on the right. The entire structure is rendered in a black wireframe style, showing the intricate geometry of the particle accelerator components.

Heavy-Ion Synchrotron and Storage Ring LLRF Systems at GSI and FAIR: Status and Machine Development Experiment Results

D. Lens, K. Groß, H. Klingbeil, U. Laier, B. Zipfel (GSI-RRF)

LLRF Workshop 2022, Brugg-Windisch

10.10.2022



GS/FAIR

Heavy-ion synchrotrons:

- SIS18 (upgrade)
- SIS100

Storage rings:

- ESR (upgrade)
- CRYRING (upgrade)
- Collector Ring CR
- High-energy storage ring HESR

FAIR Construction Site



July 2022

SIS100 tunnel



Photo: M. Konradt/GSI/FAIR

Ring RF Systems for FAIR (without HESR)



Ring	RF System	Frequency Range [MHz]	Voltage per Cavity [kV]	Duty Cycle	Length	Qty
SIS18 Upgrade	Ferrite cavities, h=4	0.85 ... 5.5	16	100%	3 m	2
	Accel. h=2 (MA)	0.43 ... 2.8	13.3	100%	1.2 m	3
	Bunch Compression	0.8 ... 1.2	40	0.05%	≈ 1 m	1
SIS100	Accel. h=10 (Ferrite)	1.1 ... 3.2	20	100%	3.0 m	14
	Bunch Compression	0.310 ... 0.560	40	0.05%	1.2 m	9
	Barrier Bucket	Broadband	2 x 15	20%	1.1 m	2
	Long. Feedback	Broadband	12 ... 15	100%	1.1 m	2
CR	Debuncher (RIB, anti-protons, incl. bucket generation)	1.10 ... 1.25 (1.50) (pbar)	Pulsed: 40 (21) CW: 2 (1.35) (pbar)	0.06%	1.125m	5
CRYRING	Existing Swedish system	0.135 ... 2.4	0.15 ... 0.35	100%	≈ 3 m	1
ESR	Ferrite cavity, h=2 Barrier Bucket	0.85 ... 5.5	5	100%	1.68	1
		broadband	0.6 (2 pulses)	50%	1.13	2 in 1

courtesy H. Klingbeil

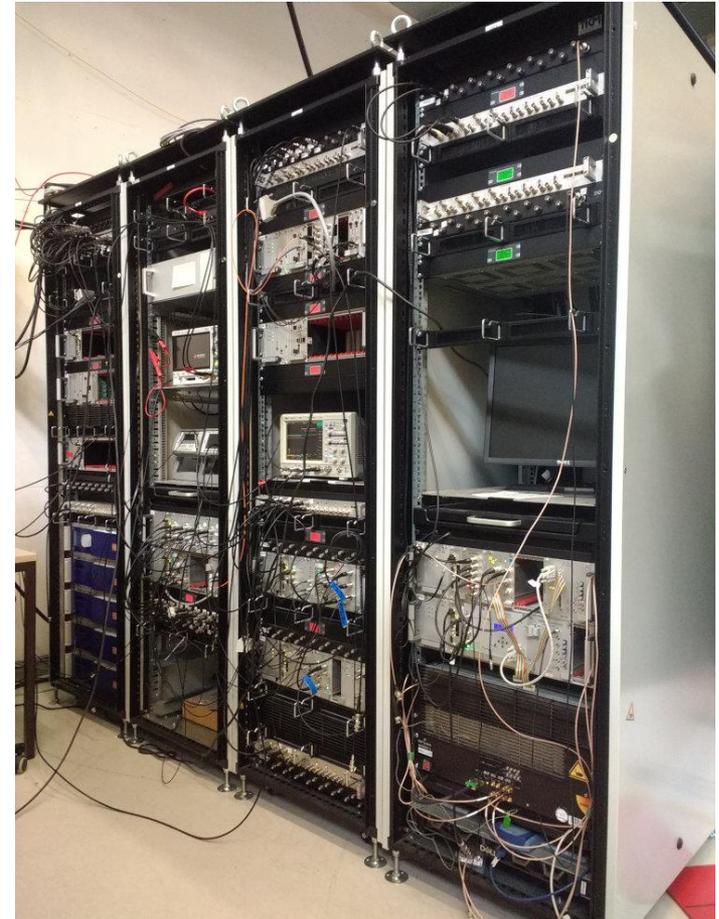
FAIR RF Systems (Selection)



SIS100 Acceleration
(RI Research
Instruments GmbH)



SIS100 Bunch
Compression
(Aurion Anlagentechnik
GmbH)

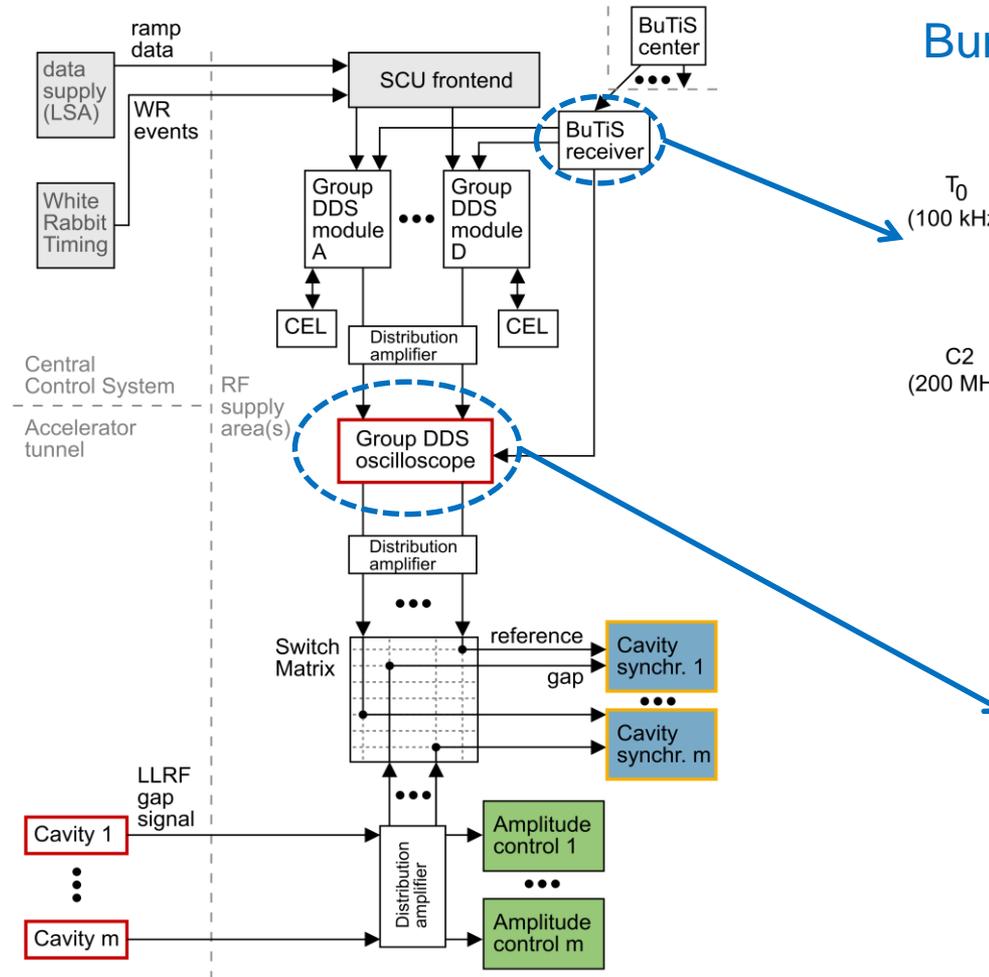
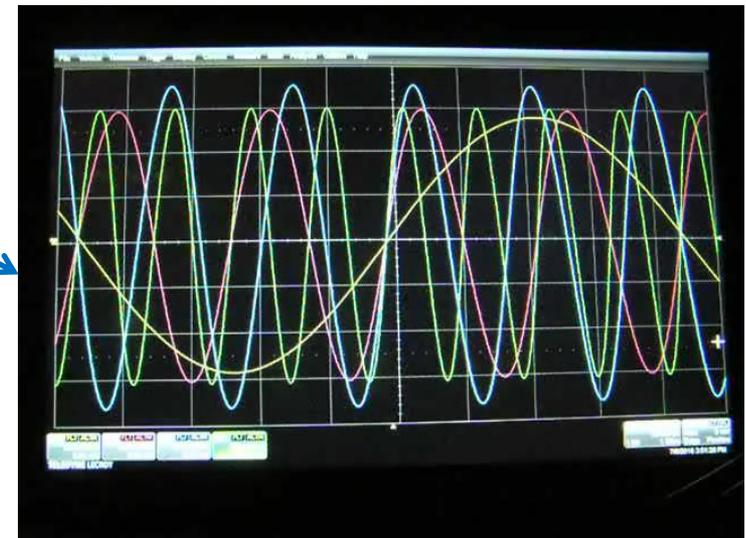
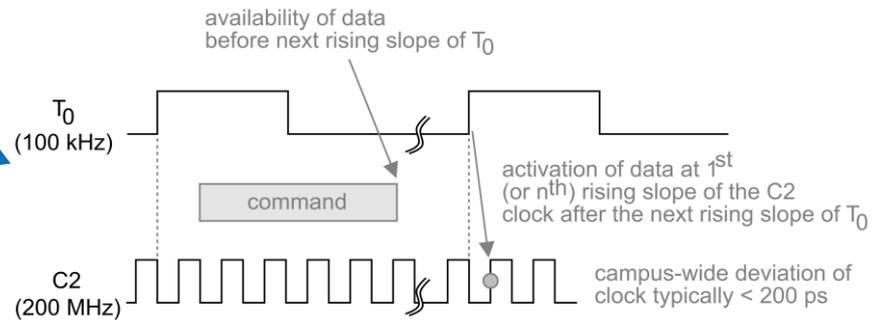


LLRF racks for one cavity system
(cavity control, control system
interface)

- Fast ramping rate, up to 10 MHz/s
- Large frequency span: revolution frequency at SIS18:
215 kHz ... 1.36 MHz
- LLRF accuracy under dynamic conditions:
Amplitude $\pm 6\%$, phase $\pm 3^\circ$
- Light to heavy ions from $^1\text{H}^+$ to $^{238}\text{U}^{73+}$
- Large dynamic range of RF amplitude, up to 60 dB
- Several RF supply areas (SIS100: 5)
- Synchronization of different types of RF systems:
CW, pulsed, broadband
- Multi-harmonic operation
- Beam feedback loops: Beam phase control, bunch-by-bunch longitudinal feedback

LLRF Topology: Reference Signals

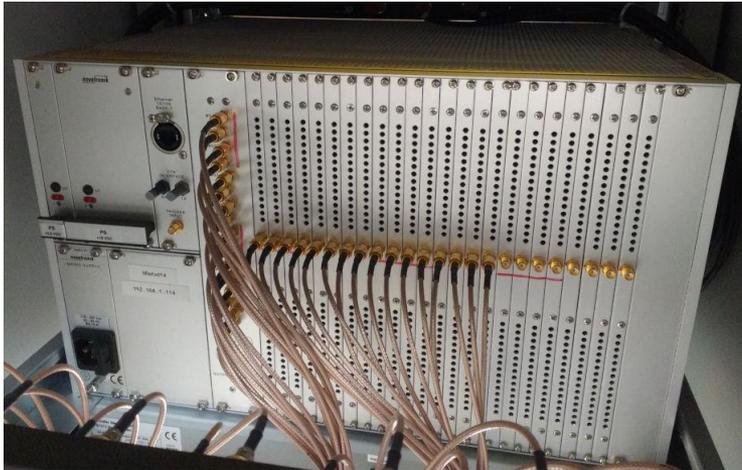
Bunch Phase Timing System (BuTiS)



Equal signal transmission properties from gap & reference to cavity synchronization

Group DDS (h=1,4,5,8) signals using Calibration Electronics (CEL)

LLRF Module Examples (I)



Switch Matrix (Novotronik Signalverarbeitung und Systemtechnik GmbH)



BuTiS Receiver Station (GSI, WORK Microwave GmbH, PPM Vialite)

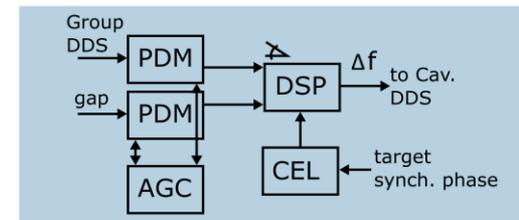
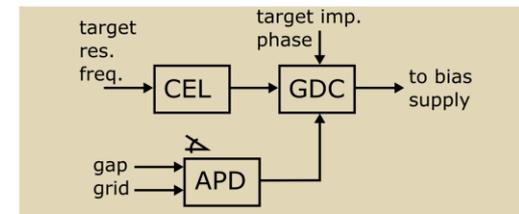
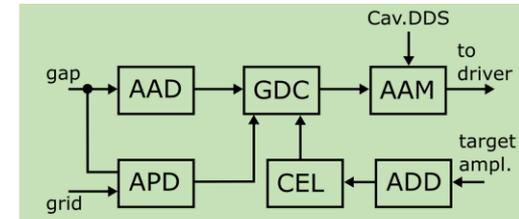
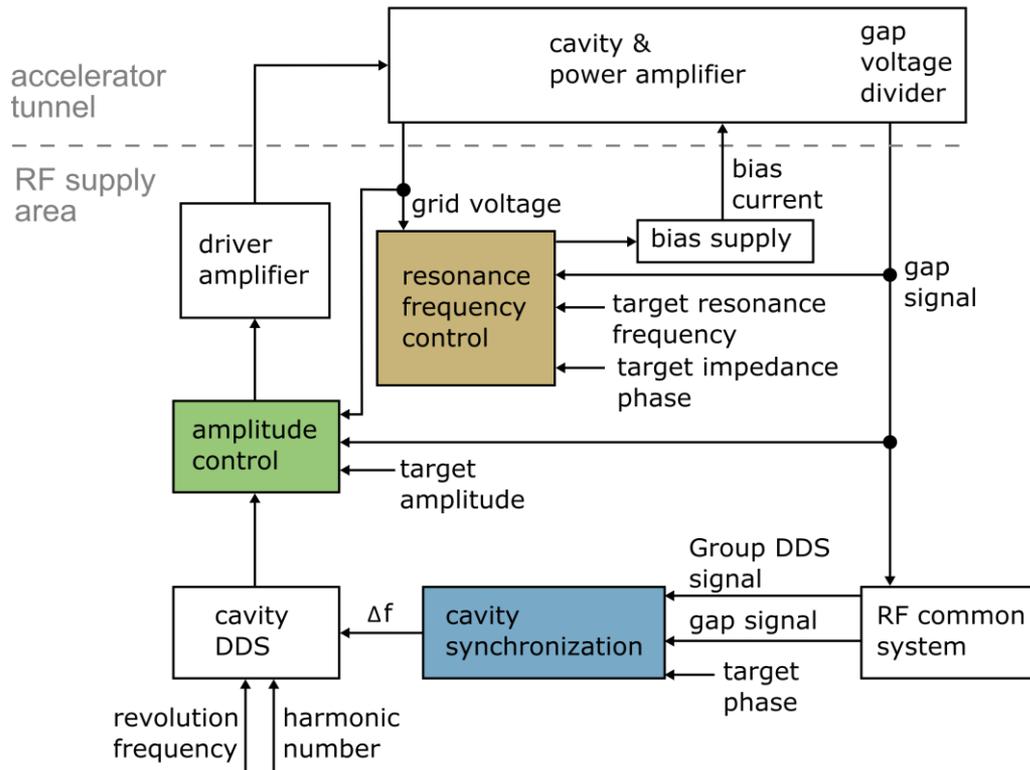


DDS (GSI) with FPGA Interface Board FIB3 (KTS – Kommunikationstechnik und Systeme GmbH)



RF Distribution Amplifier (GSI)

LLRF Topology: Cavity System



- Multiple use of modules and interfaces, e.g.:
 - Generic controller (GDC): Amplitude control, resonance frequency control, ...
 - Calibration electronics (CEL): Calibration of phase & amplitude, feedforward, ...
 - DSP: Cavity synchronization, beam phase control, longitudinal feedback

LLRF Module Examples (II)



Amplitude control crate (GSI)



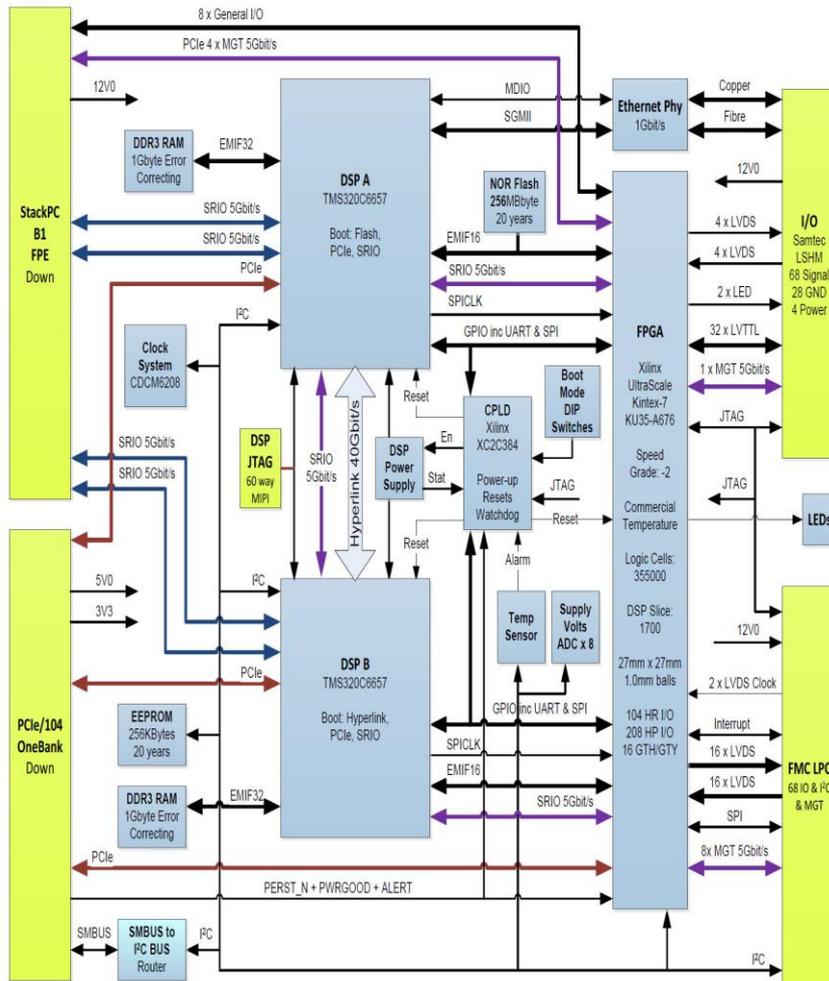
CEL, calibration electronics (GSI)



DSP System (Sundance Multiprocessor Technology Ltd.)

DSP System Architecture

Figure 1 Block diagram of SMT6657

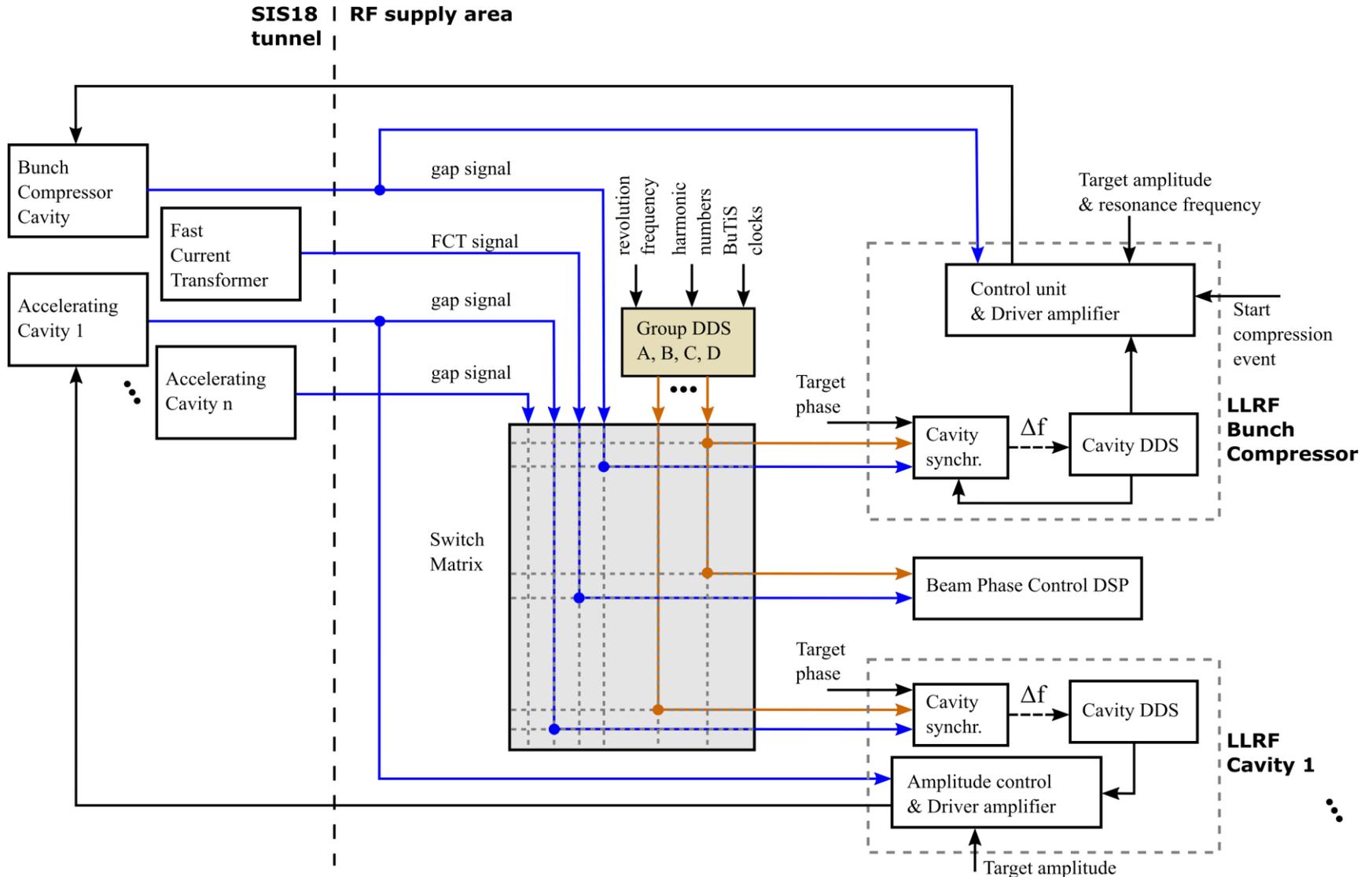


System architecture of SMT-6657 (Sundance Multiprocessor Technology Ltd.)

- 2 DSPs (TI, 1.25 GHz)
- Xilinx Kintex7 UltraScale FPGA
- PCIe interface to host PC
- DSP A: master (booting, monitoring, acquisition, ...)
- DSP B: real-time operation and closed-loop control @ 310 kHz
- ADC/DAC: FMC mezzanine card SMT-FMC311
- I/O boards (trigger, optical, etc.)

From: Design Description SMT6657, Sundance Ltd., 2018

Cavity Synchronization



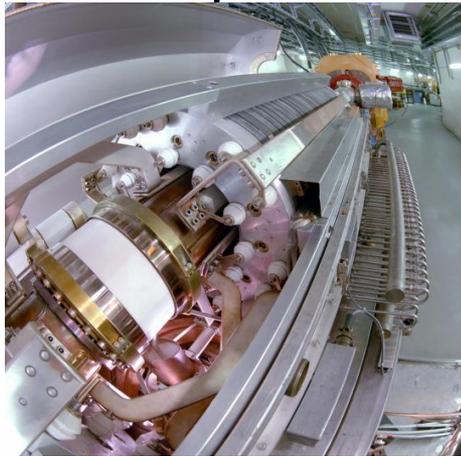
SIS18 Machine Development Experiments (MDE)

Magnetic rigidity
up to 18 Tm

Injection
energy:
11.4 MeV/u

Extraction energy:
 $^1\text{H}^+$ up to 4000 MeV/u
 $^{238}\text{U}^{73+}$ up to 1000 MeV/u

Photo: A. Zschau



Ferrite
cavities
(2x)



MA cavities (3x)

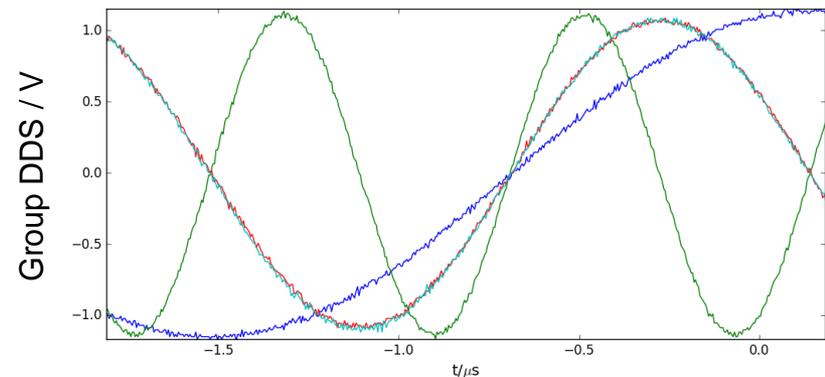
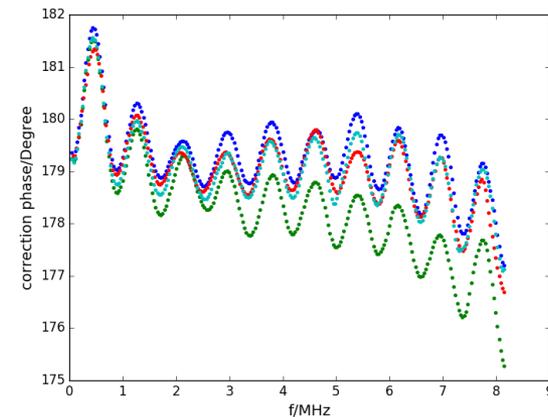
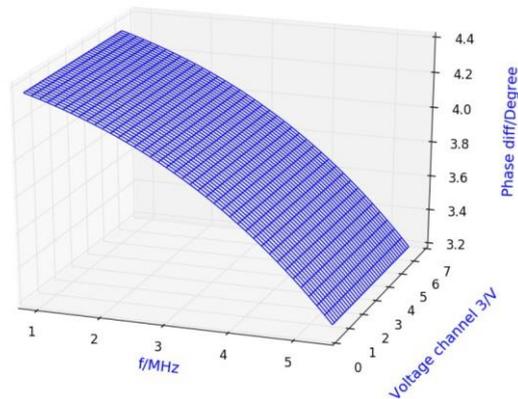
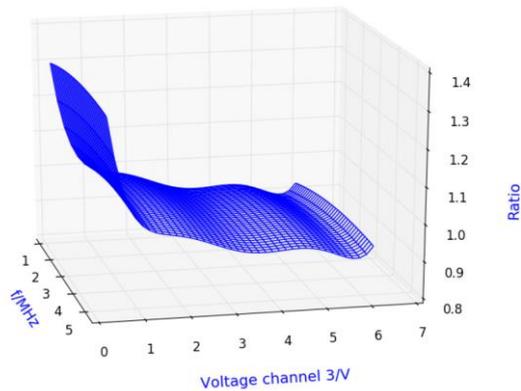


Bunch compressor

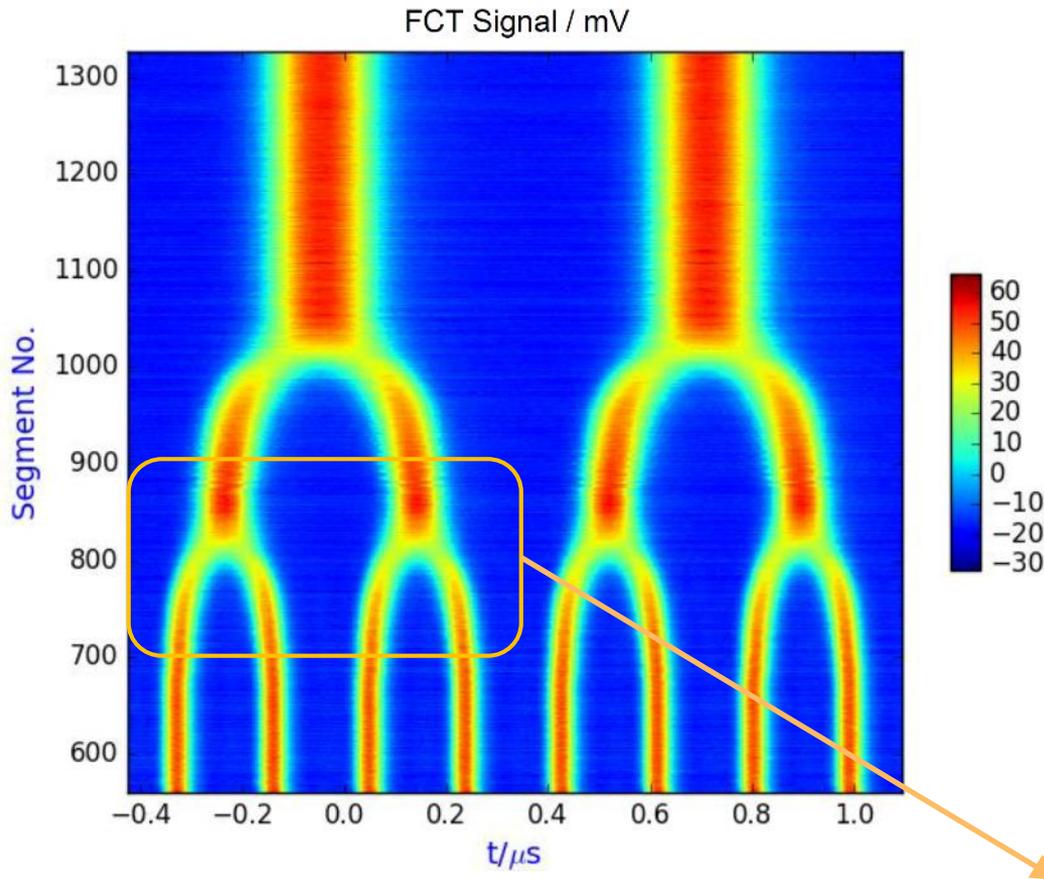
Photo: G. Otto

SIS18 Cavity and Group DDS Calibration

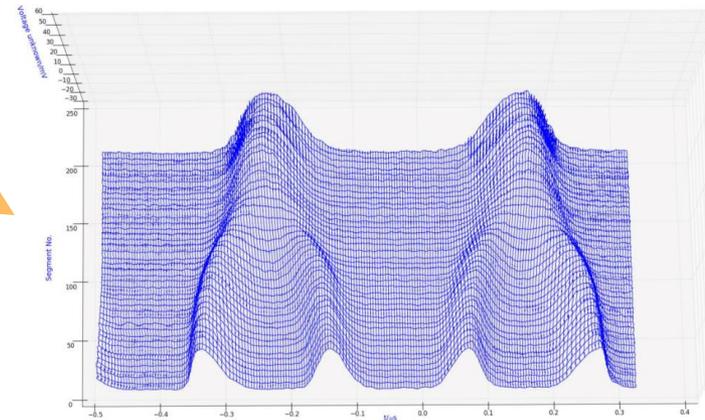
- Delay measurements and adjustments
- Cavity calibration: Amplitude & Phase
- Group DDS calibration with respect to BuTiS (courtesy A. Andreev)



SIS18 MDE: Bunch Merging



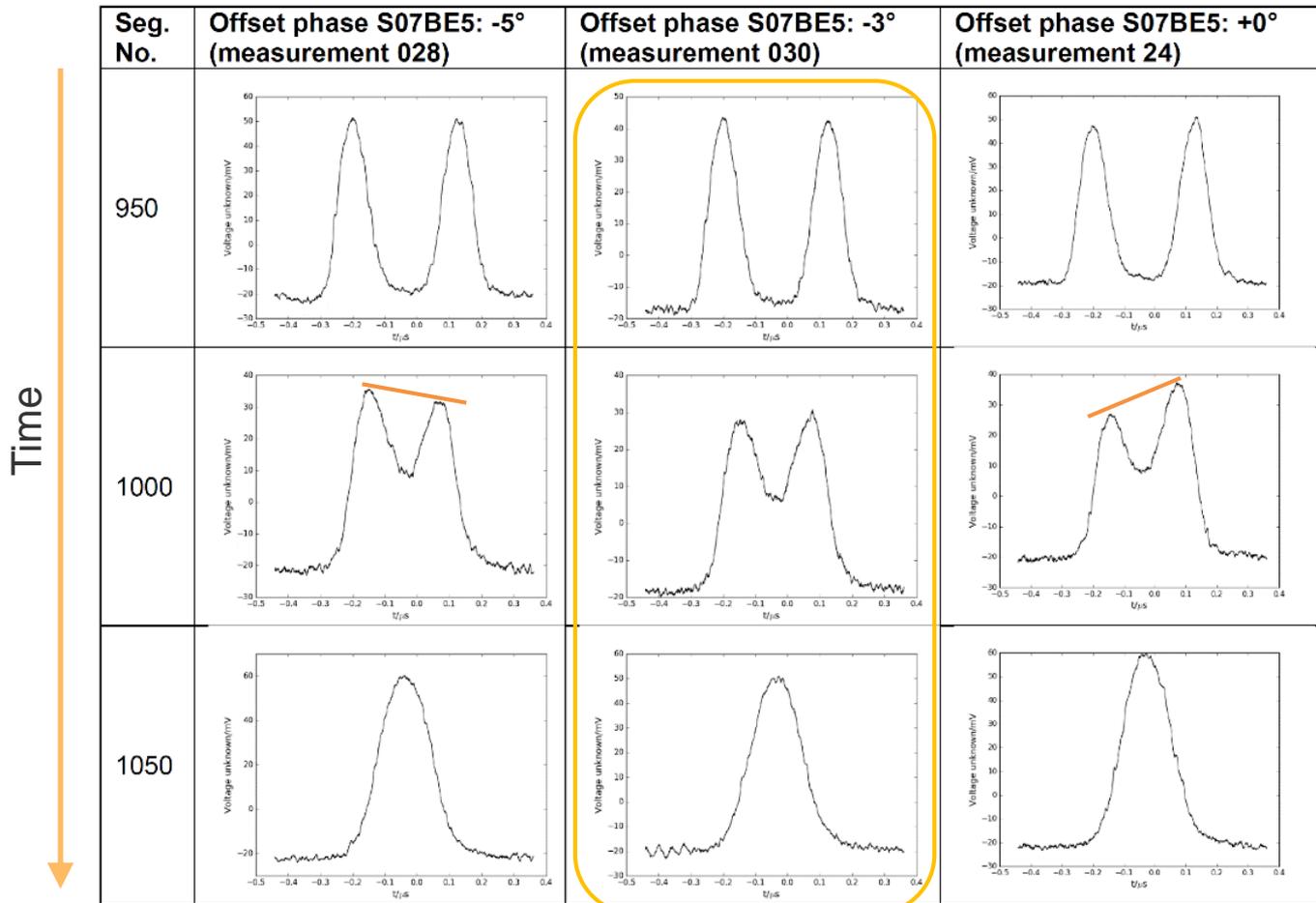
- Bunch merging at flattop
 - Ion species: $^{40}\text{Ar}^{18+}$
 - $h=8 \rightarrow 4 \rightarrow 2$
 - Beam current ≈ 1.3 mA
- Fully controlled by CCS, but:
- Phase accuracy of $\pm 3^\circ$ not yet achieved for all SIS18 systems
- LLRF upgrade still in progress



FCT signal for optimized merging
(manual phase offsets $> \pm 3^\circ$ for some systems)

Optimization of Merging Process

FCT Signal

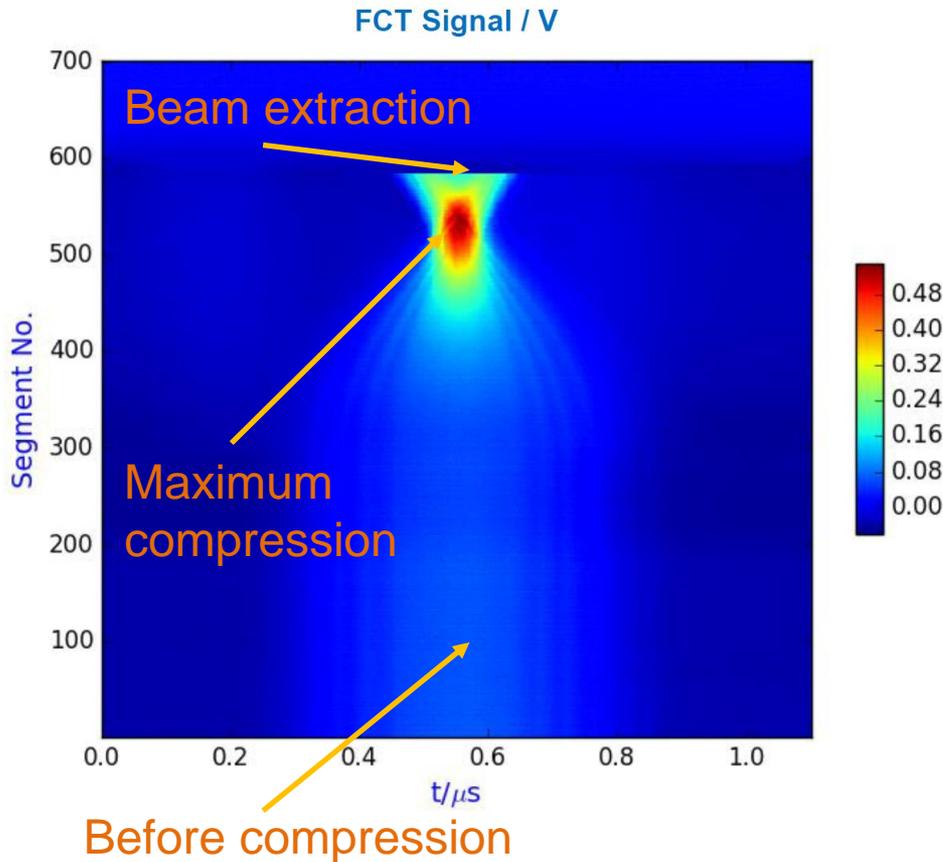


- Optimization of merging by adjusting the phase of one cavity
- Sensitive test for phase errors of a few degrees

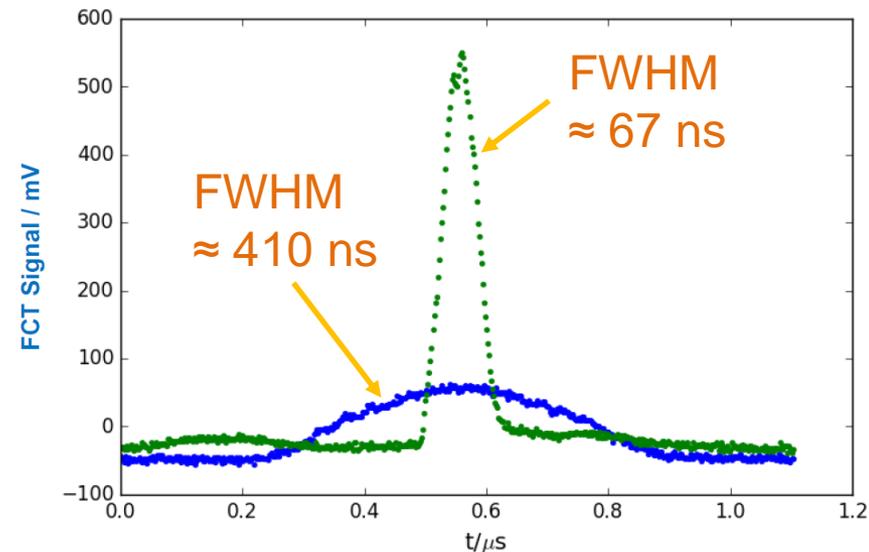
Best result

Default CCS value

SIS18 MDE: Bunch Compression



- Bunched beam at flattop, voltage with MA cavity: 760 V
- Pulse of bunch compressor cavity shortly before extraction, rise time < 40 μs, voltage amplitude 30 kV



$$\sqrt{\frac{\hat{U}_2}{\hat{U}_1}} = \sqrt{\frac{30760 V_p}{760 V_p}} \approx 6.36$$

- Majority of LLRF hardware delivered and tested
- Machine development experiments at existing machines (SIS18, ESR) for verification of LLRF functionality
- Number of 19“ racks for FAIR:
 - SIS100: 153
 - CR: 25
- Rack pre-assembly is ongoing (>50% completed)
- LLRF firmware development is ongoing
- Start of installation in SIS100 supply tunnel in 2023

- LLRF concept for GSI & FAIR, including upgrade of existing machines:
 - High ramping rate, large frequency span, different types of cavity systems
 - Modular LLRF setup with standardized analog and digital modules
 - Use of the same standardized modules for different purposes
- LLRF topology:
 - Reference signal distribution: BuTiS, Group DDS, Switch Matrix
 - Amplitude and (for some systems) resonance frequency control
 - Cavity synchronization
- SIS18 machine development experiments:
 - Successful multi-harmonic operation: Bunch merging and compression
 - Verification of LLRF topology for FAIR
- Status of LLRF realization for FAIR