Low Level RF for Industrial LINACs

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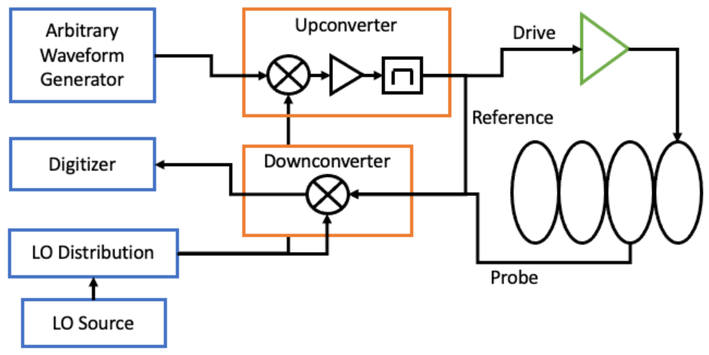
Abstract

Compact particle accelerators are increasingly needed in medical, industrial, and defense settings. Such an accelerator requires a highly efficient, lightweight, and space-efficient footprint; this leverages particularly unique requirements on RF, power, and thermal budgets. Low Level RF systems have historically fallen into two categories. Custom systems developed at national laboratories or industrial systems using custom hardware specifically designed for LLRF. Recently however advances in RF technology accompanied by demand from applications like quantum computing have led to commercially available systems that are viable for building a modular low-level RF system. RadiaSoft has been working with SLAC on developing the LLRF system for a structure consisting of multiple accelerating cavities in such an energy- and space-constrained footprint. Here we provide an overview of two different design methodologies that utilize varying amounts of COTS components when considering scalability, footprint, and modularity.

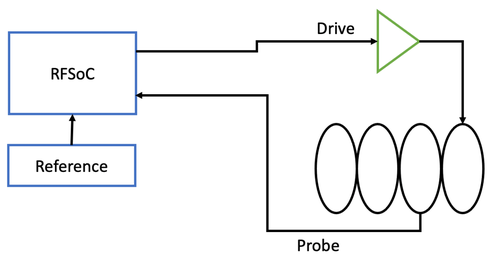
Traditional LLRF Architecture

The Low-Level Radio Frequency (LLRF) control system is primarily responsible for delivering RF to amplifiers, receiving and processing signals for the various RF diagnostics, and control of the RF cavities to include phase, amplitude, and frequency. When building a LLRF system there are a number of design considerations that lead to the choice of frequency parameters, digital vs analog, and how to modulate the RF signals. One of the most common architectures utilizes an intermediate frequency that is used for digitization and an analog system to perform up and down conversion.

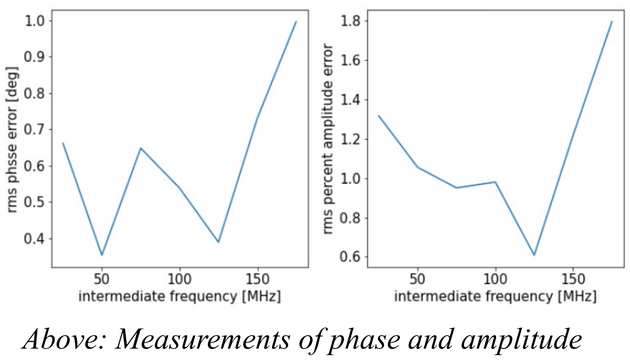


RF SoC Based System

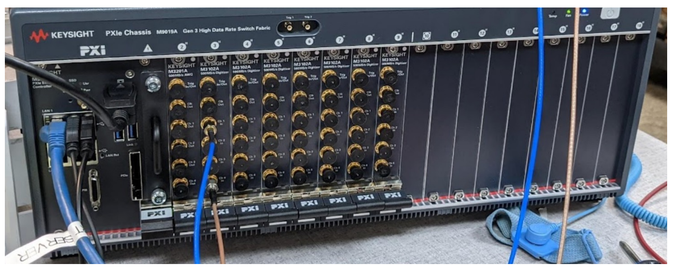
Modern signal processing algorithms and advanced semiconductor fabrication techniques have led to the advent of technologies such as the Xilinx RFSoC. This integrates multiple RF signal chains with programmable hardware and compute on the same chip, and has recently been a popular system of investigation for BPM and RF control systems in accelerators. Their high bandwidth and capabilities for sampling in different Nyquist zones make them an attractive solution for certain applications. Here the block diagram is as simple as it gets, allowing for high-density, compact designs.



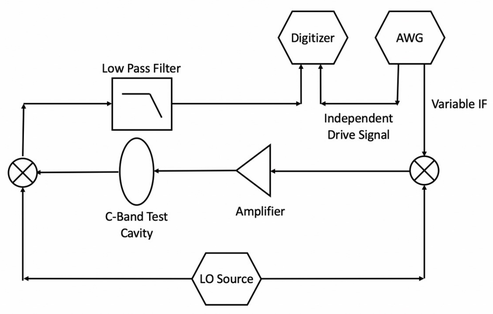
Keysight Digital LLRF System



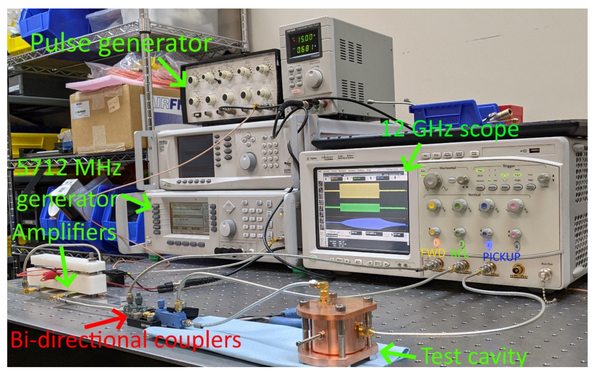
Above: Measurements of phase and amplitude stability as the intermediate frequency is varied. Below: Photo of the Keysight AWG and Digitizers



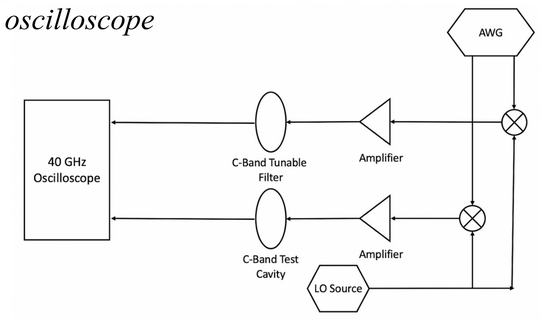
Right: Measurement setup for verifying the phase and amplitude stability of the digital system with standard RF components for the up and down conversion



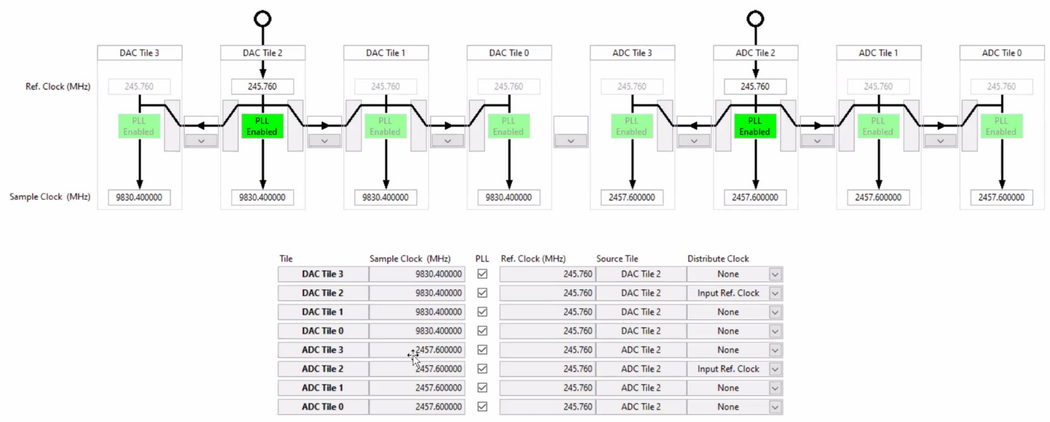
The digital system is comprised of a an M3102A PXIe Digitizer from Keysight and an M3201A PXIe Arbitrary Waveform Generator also from Keysight. Our AWG resolution is 16 bit at a 500 MS/s sample rate. The digitizer resolution is 14 bit at a 500 MS/s sample rate. The choice of intermediate frequency is largely determined by the available digital components and the constraints on RF filtering, This typically is in the 10 – 100 MHz range. Our initial choice of the intermediate frequency is 100 MHz. This is to allow for good isolation between IF signals, RF signals, and baseband signals. The arbitrary waveform generator has built in I/Q modulation for phase coherent signal generation. It can generate sinusoidal signals with envelope and phase modulation all synchronized to an internal reference clock. The DACs are 16 bit which provides a high level of precision for the RF drive signals. The digitizers are each four-channel analog to digital converters (ADCs) that sample based on the same fixed clock as the DACs. The ADCs operate at 500 MS/s and have 14 bit resolution. This was chosen to allow for precise measurement of the RF amplitude and phase at various locations in the RF network. 500 MS/s is a compromise on cost with sample frequency. Higher frequency ADCs and DACs would provide higher performance with regard to control and noise reduction. We performed tests of the 500 MS/s system to ensure the reduced sampling capacity would still provide the desired phase and amplitude stability. Top left shows the amplitude noise and phase noise as we vary the intermediate frequency. Our budget is around 0.5 degrees phase noise and 1% amplitude noise. Thus an intermediate frequency of around 100MHz should be adequate. Note that this measurement includes components used for the upconverter and downconverter system.



Below: Measurement setup for independent phase measurement using high speed oscilloscope

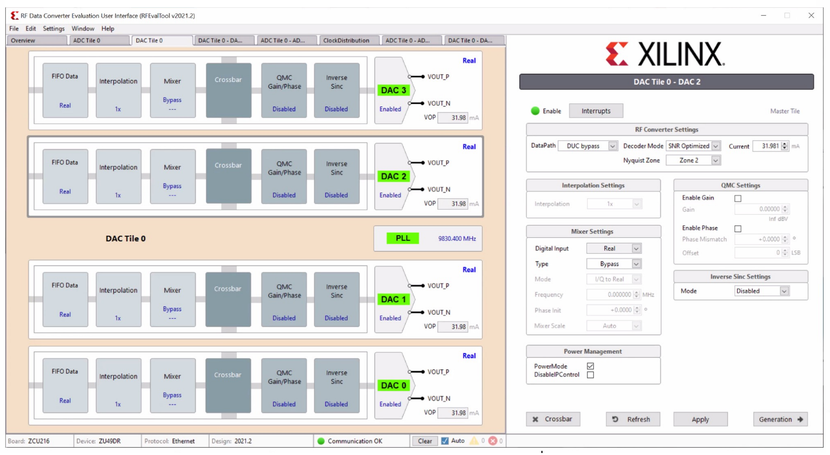


RFSoC DDC LLRF System

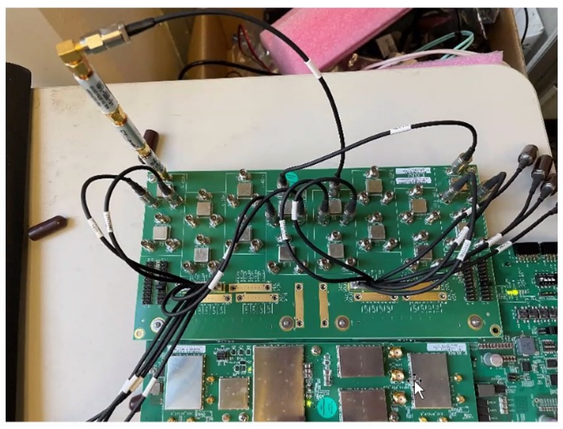


Tile	Sample Clock (MHz)	PLL	Ref. Clock (MHz)	Source Tile	Distribute Clock
DAC Tile 3	9830.400000	☑	245.760	DAC Tile 2	None
DAC Tile 2	9830.400000	☑	245.760	DAC Tile 2	Input Ref. Clock
DAC Tile 1	9830.400000	☑	245.760	DAC Tile 2	None
DAC Tile 0	9830.400000	☑	245.760	DAC Tile 2	None
ADC Tile 3	2457.600000	☑	245.760	ADC Tile 2	None
ADC Tile 2	2457.600000	☑	245.760	ADC Tile 2	Input Ref. Clock
ADC Tile 1	2457.600000	☑	245.760	ADC Tile 2	None
ADC Tile 0	2457.600000	☑	245.760	ADC Tile 2	None

Clock configuration for testing with the RFSoC



Configuration of the RFSoC in the second Nyquist zone to test the bandwidth of the system.



RFSoC in a loop back configuration to measure the amplitude and phase stability.

We have been investigating the use of an RFSoC system for a fully digital LLRF system at S and C-band frequencies. This comes with the caveat that the expected noise levels will be a bit higher than some scientific applications require. For certain industrial, security, and defense applications however the beam stability requirements are not as stringent. The opportunity of delivering a compact scalable LLRF system using this technology is promising for these applications.

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