PIP-II Resonance Control System

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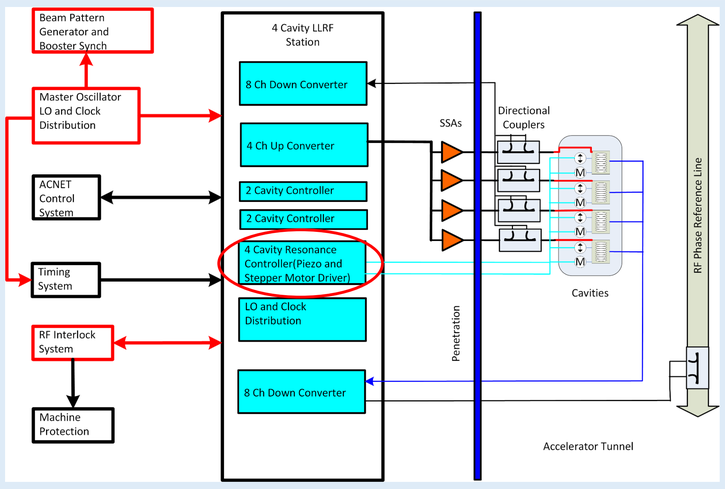
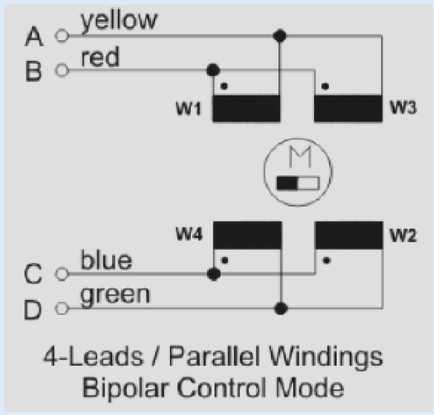
Abstract

The PIP-II Resonance Control System has the goal of providing the electronics to mechanically tune four superconducting cavities as directed by two RF control stations or via LAN manual commands (python LEEP scripts). This solution leverages the LCLS-II Resonance Control chassis design, but with an Intel based FPGA carrier and is largely compatible with LCLS-II screens. This resonance control system will have a 2 Hz/step resolution with up to 256 micro steps per full step. This system also employs piezo driver control with intended resolution better than 1 Hz and a control bandwidth of ~ 500 Hz. The piezo driver boards have ADCs for sampling key piezo signals and the DAC output. Cavity detuning information is received over a QSFP fiber interface from the RF station(s). The waveforms of these sampled signals are displayed on EPICS screens for live troubleshooting and diagnostics.

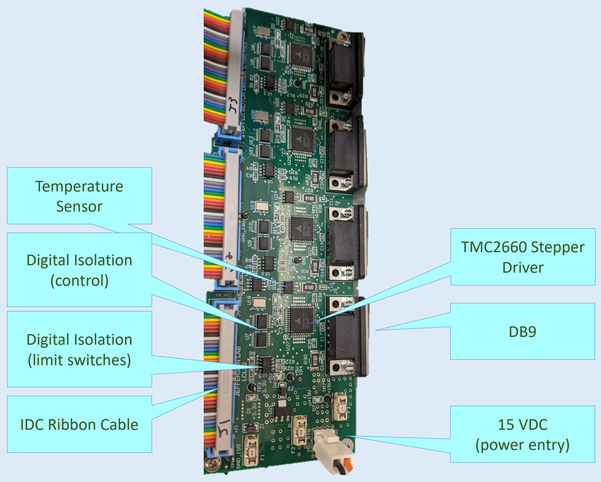


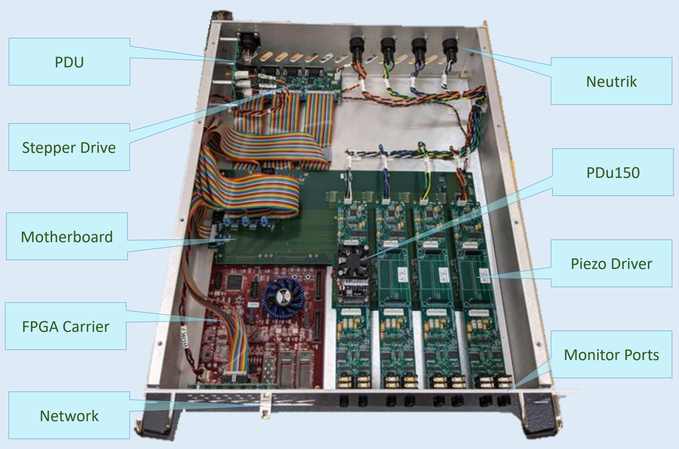
System Level Block Diagram

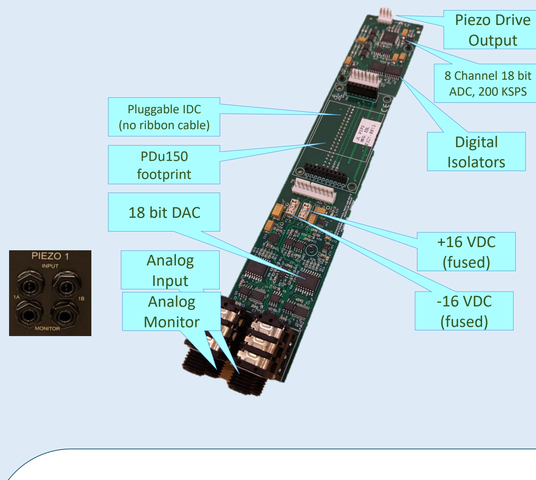
Piezo Tuner Stack



Stepper Motor







Stepper Driver Board

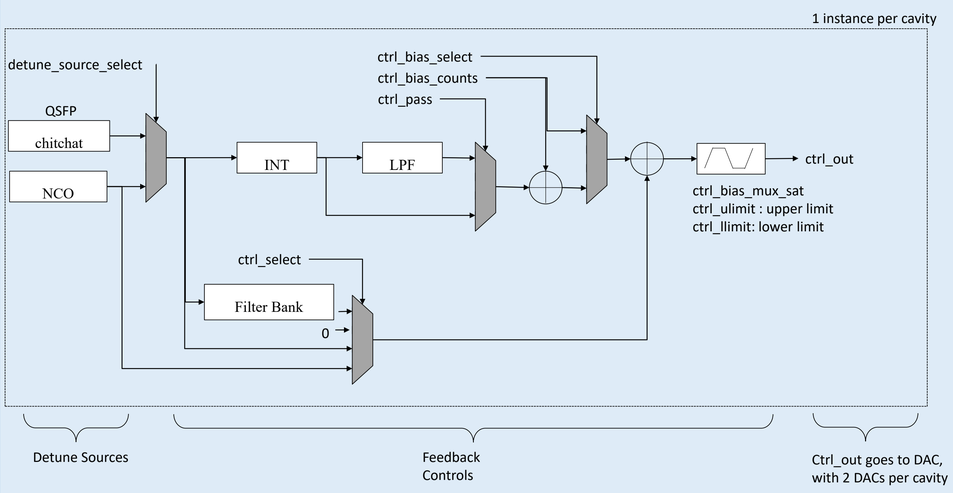
This stepper driver board will control four stepper motors. It is required that the system will have at least a 2 Hz per step resolution or better. Each stepper coil should produce no more than 2.5 Amps per phase with the drive current being controlled over the EPICS user interface. The stepper driver chip that is used is TMC2660 which uses 256 micro steps per full step. The TMC2660 uses SPI configuration with a standard DIR/STEP control. There are 200 full steps per revolution. It is also a requirement that the stepper be turned off when not in use (i.e. a zero hold current). This is accomplished with Enable/Disable MOSFETs on the TMC2660 chip. This stepper driver board also receives limit switch information which are hard physical limits. Digital isolators are used on all digital signals that interface between the stepper driver board and the FPGA carrier.

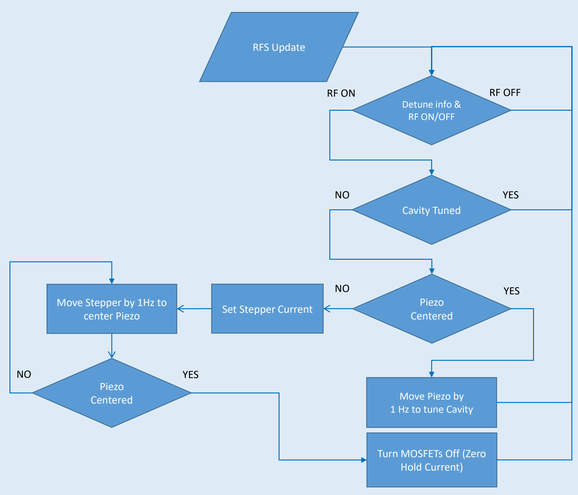
Resonance Control Chassis Layout

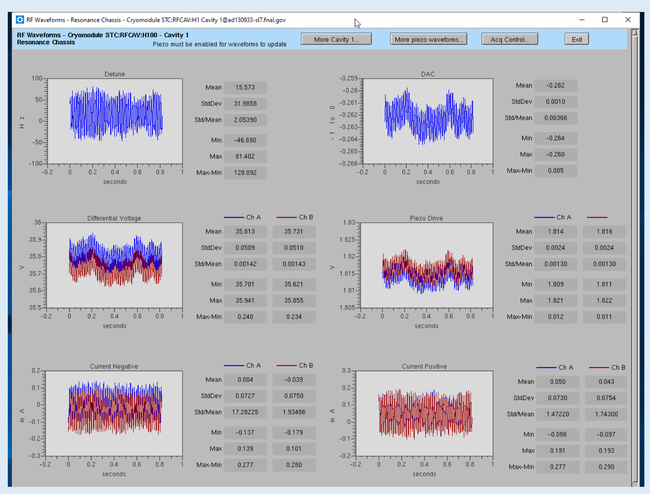
The PIP-II Resonance Control System largely leverages the LCLS-II design with several key differences. This chassis employs an Intel based Cyclone 10 GX FPGA carrier designed by Jefferson Lab LLRF. The firmware that ran on the LCLS-II RCC was largely ported onto this Intel platform with great success. The network interface between the LCLS-II RCC and the Jlab RCC is identical making the screens functionally compatible. Modifications to the Piezo boards were made to make these board-to-board pluggable, thus eliminating some of the ribbon cables and making the design cleaner and easier to maintain. This chassis can support 1 RJ-45, 1 SFP and 2 QSFP for 10 total network connection options. The RJ-45 is used for EPICS/soft IOC communication and 1 QSFP is used to receive detune information.

Piezo Driver Board

The Piezo Driver board has the goal of having a better than 1 Hz piezo tuner control and a control bandwidth of approximately 500 Hz. Detune information is received from the RFS over a dedicated fiber link (one RFS provides detune information for 2 cavities). This piezo driver board employs a PDU150 piezo driver which is a 'Commercial off-the-shelf' product. This driver allows for 100 Vpp drive. This piezo driver board is largely similar to the LCLS-II design. Several PCB routing improvements and mechanical features were added such as moving fuses to the top of the PCB and enabling this piezo driver to be directly pluggable into the FMC expansion board, thus removing ribbon cables. Digital isolators are used between all digital signals between this piezo driver boards and the FPGA carrier.







Piezo Control Configurations

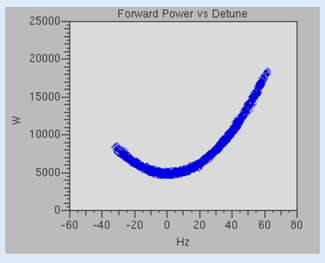
The above block diagram describes the Piezo control configurations that are currently available. This block diagram is shown for one cavity. One RFS chitchat detune link, provides detune information for two cavities. The primary piezo tuner control is achieved with a slow integrator with an optional low pass filter. This firmware also supports a customizable filter bank initially developed by FNAL. This filter bank is currently being developed but the goal will be to have the option of providing active noise cancellation. The firmware contains safety limits which are set in EPICS or manually through LEEP scripts. The control output is driven by DACs on the Piezo board (2 DACs are used per cavity, see picture in top right corner of poster of Piezo stack). The cavity bandwidth is about 35 Hz. The Piezo range is observed to be 2kHz (by adjusting the control bias to its limits). Capacitive load for a cold cavity is estimated at 4.4 uF.

Tuner Flow Diagram

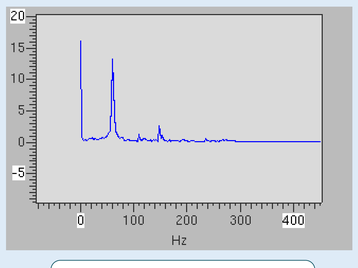
The above diagram describes when the stepper tuners should be used and when the piezo tuners should be used. All detune information is received from the RFS over a fiber link through the ChitChat protocol. If the cavity is in need of tuning and the Piezo is centered, then the piezo will be used to bring the cavity to reference. Due to low frequency helium pressure drift, the resonance point will be pushed outside of the piezo range over time. When this happens the piezo is no longer centered and the stepper motor must be used. The stepper motor will be used to center the piezo. Once centered, the steppers will turn off (have zero hold current) and the Piezo drivers will tune the cavity. Currently, it is a design decision to only move the steppers when not running beam so this step will be manually performed by operators.

Tuner Waveform Viewer

The EPICS screens developed by SLAC for the LCLS-II RCC are also compatible for this Intel based FPGA carrier JLab RCC (since the same base firmware is used). These screens have useful debug features such as the waveform viewer shown above. This waveform viewer shows the real time data and are useful for debugging and troubleshooting. This data are sampled by ADCs on the Piezo Driver board and are stored in circular buffers on the FPGA carrier. When EPICS is ready, it will offload this data to the waveform viewer. The above plots show the detune information being received by the RCC from the RFS. The waveform viewer also shows DAC output (shown in normalized counts), differential voltage, Piezo drive voltage and some current monitoring information. These waveforms are for one cavity. Stepper information is controlled on a separate screen.



FWD PWR vs Detune



FFT of Detune Data

Summary

The RCC has been tested at STC and MESON 650 Test stand at FNAL. All essential communication channels have been verified and the chassis interfaces well with EPICS. Stepper controls work as desired however more development for active noise cancelling for the piezo controls appears to be needed. This is the current focus going forward.

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References

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[2] R. Bachimanchi et al., "LLRF Resonance Control System for LCLS-II Cavities" in Proceeding of LLRF2017, Barcelona, Spain, 2017.
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[4] Larry Doolittle, private communication.
[5] Sergio Paiagua, private communication.