Electron-Ion Collider Common Platform System Architecture

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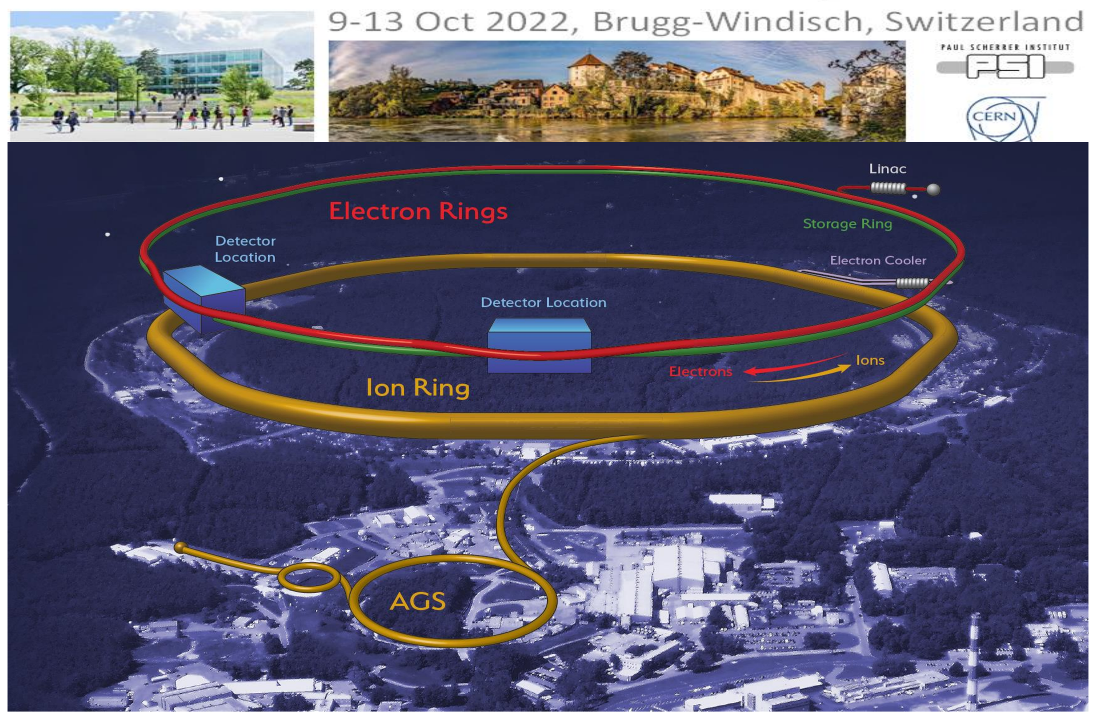
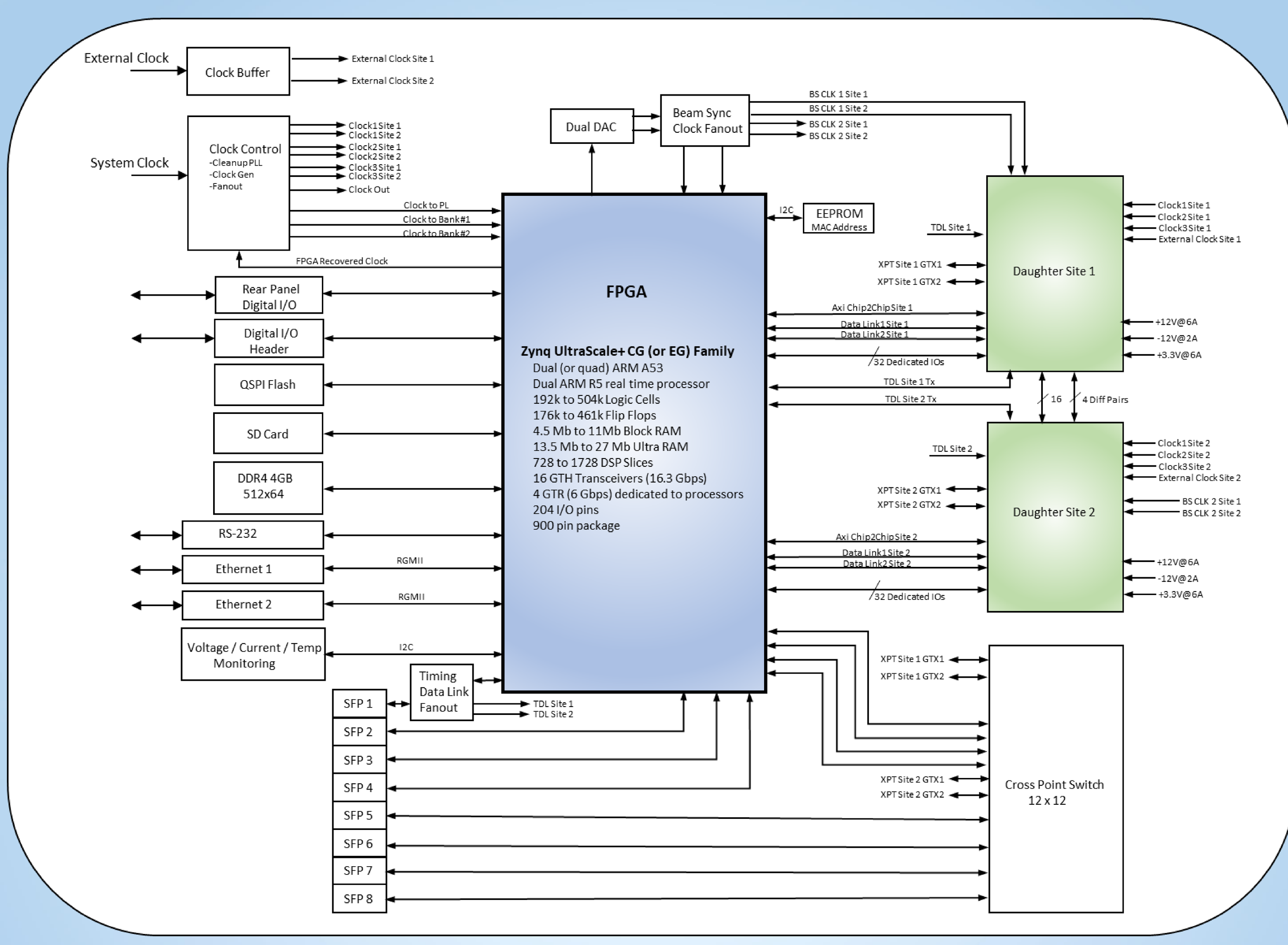


The Electron-Ion Collider (EIC), to be constructed at Brookhaven National Laboratory (BNL), is a roughly 10-year project to design and construct a facility to collide high energy polarized electron beams with polarized proton and heavy ion beams at center of mass energies from 20 GeV to 140 GeV and luminosity up to 10^{34} $cm^{-2}s^{-1}$. The project is a partnership between BNL and the Thomas Jefferson National Accelerator Facility (Jefferson Lab, JLAB).
The EIC Common Platform is an effort to design and implement a flexible, high-performance electronics platform for required Low Level Radio Frequency (LLRF), Timing, Machine Protection, Instrumentation, Power Supply, and general-purpose Accelerator Controls systems. The fundamental architecture of the Common Platform, centered on a Xilinx Zynq UltraScale+ MPSoC-based carrier board and a variety of function specific daughtercards, is an evolution of the LLRF Platform in use at the BNL Collider-Accelerator Department since 2009. The preliminary architectural design of the Common Platform and its application for LLRF controls is described.

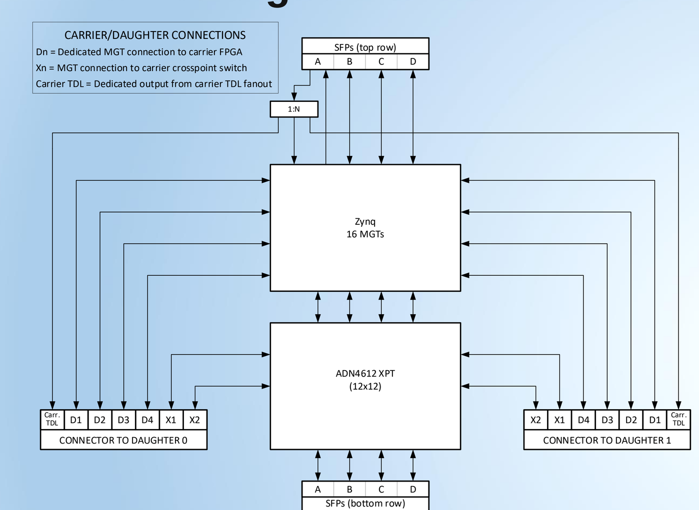
Common Platform Block Diagram



- Dual gigabit ethernet
- 4 GB of DDR4 memory
- 4 SFP+ direct to Carrier FPGA – 1 dedicated to Timing/Data Link
- 4 SFP+ to Carrier crosspoint switch – can route to Carrier FPGA (4) or daughter sites (2 each)
- System clock: external input or recovered from TDL, cleanup PLL
- On board generation of beam synchronous clocks (2)
- SD Card & QSPI Flash configuration memories
- UART interfaces (1 RS-232, 1 via USB)
- Voltage/Current/Temperature monitoring
- Generic Digital I/O

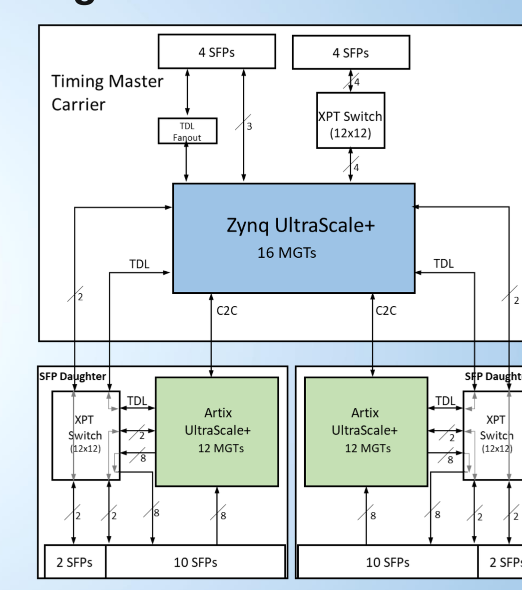
- Two Daughter Sites
  - 4 Multi-Gigabit Serial Links to Carrier FPGA
  - 2 Flexible connections via crosspoint switch to Carrier FPGA, SFPs or other daughter sites
  - Generic I/O connections
  - Real Time and Beam Synchronous Clocks
  - Site to Site Connections

Carrier Gigabit Links



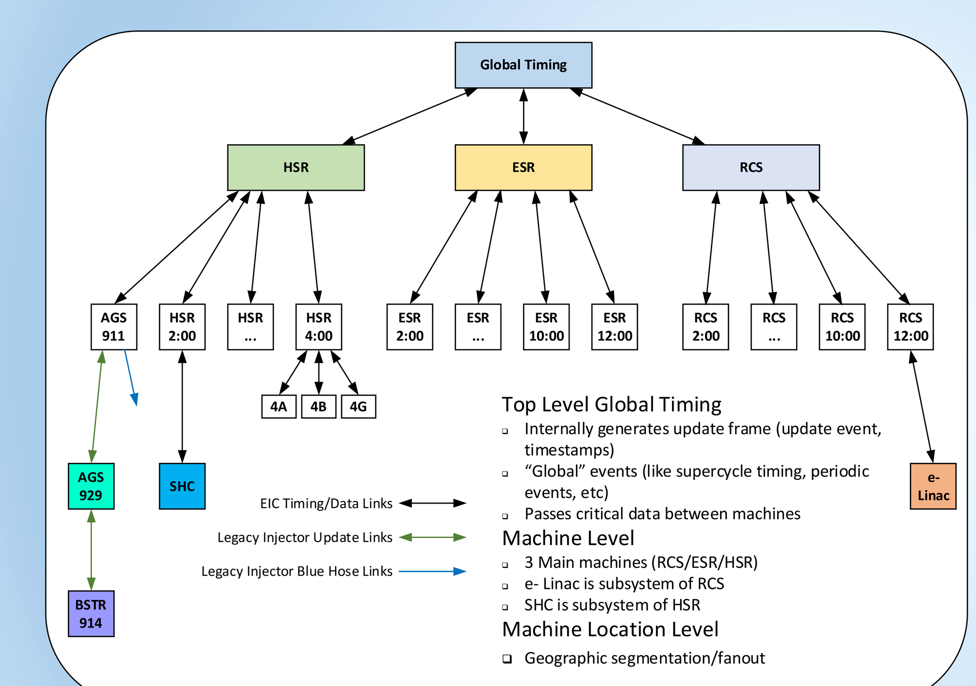
- One carrier / daughter link uses Xilinx AXI Chip2Chip for Control System interface to daughter
- One carrier / daughter link for timing / data link
- SFPs can be used to interface 'remote daughter' with both TDL and C2C (2 SFPs per remote daughter)

Timing Master Implementation Using Common Platform



1 upstream and 31 downstream full-function TDL connections from one chassis

Common Platform Timing / Data Link Distribution Concept



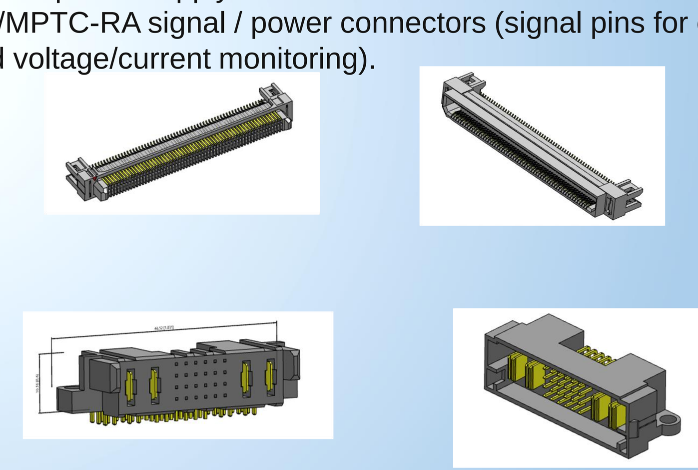
- 8 Gbps deterministic link
- 64-bit words with 8B/10 encoding yields 100E6 words/sec
- 16-bit Packet ID and 48-bit data payload
- Effectively no limit on number of defined events
- 'Update Pulse' at 100 kHz
- Machine reference phases latched and broadcast @ 100 kHz
- Data distributed globally, by machine, or by local area
- Beam synchronous signal based on common clock, common data and deterministic reset signals

Chassis Physical Layout

- Carrier (rear) and two daughtercards (front)
- Separate power input board (rear)
- Supplies +12 V and (optionally) -12 V to carrier
- Carrier does not require -12 V, some daughtercards will
- Supports multiple versions, expect to use low voltage (< 48 V) DC input in most cases
- 12 – 60 VDC single input
- 12 – 60 VDC dual (redundant) input

High Speed Edge Mounted Connectors

- Allows function / filter cards to be accessed thru front panel of chassis
- Carrier/daughter connections use two 120 pin Samtec ERM8-EM/ERF8-EM board edge mount connectors per daughtercard site.
- Carrier/power supply connection uses Samtec MPSC-RA/MPTC-RA signal / power connectors (signal pins for control and voltage/current monitoring).



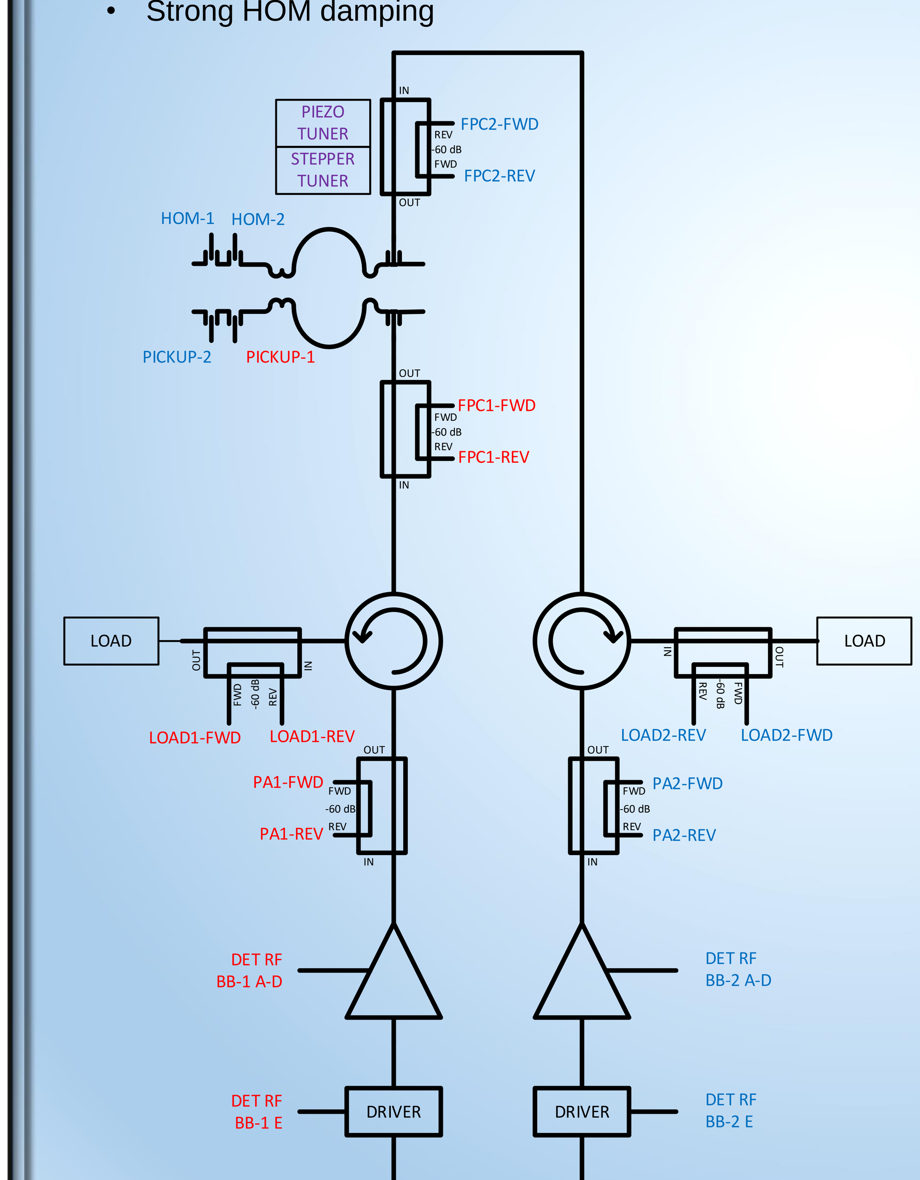
Electron Storage Ring (ESR) - LLRF Design

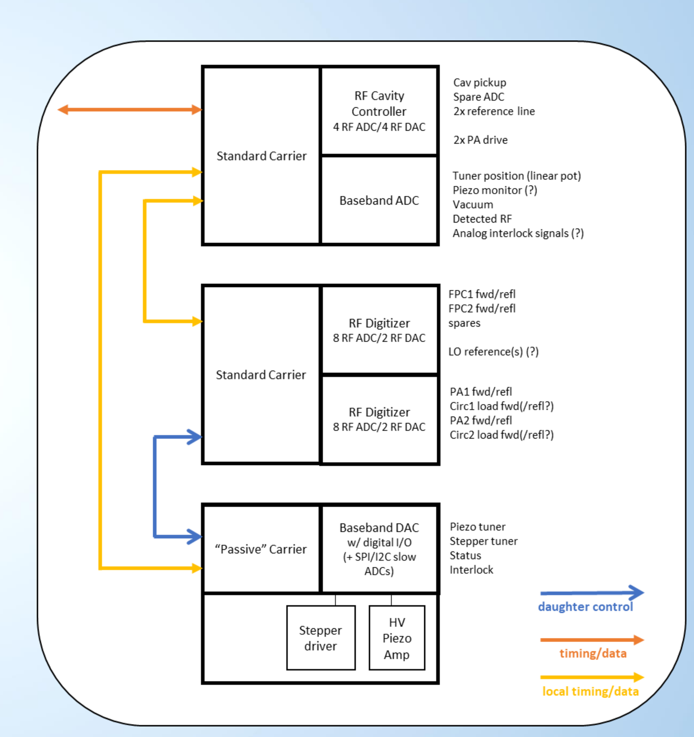
System Specifications

- 591MHz Single Cell Cavity Cryo-Module
- 17 Cavities
- 68MV, 2.5A Beam, 10 MW SyncRad
- Dual 500 kW CW FPCs
- 2x400kW Solid State Amplifiers
- Large tuning range
- Variable FPC Qext using waveguide tuning
- Low R/Q
- Strong coupling
- Strong HOM damping

Cavity Controller Configuration

- Primary chassis
  - RF cavity control daughter (4 RF ADC, 4 RF DAC)
  - Baseband ADC daughter (16 CH)
- Secondary chassis
  - RF digitizer daughter (8 RF ADC, 2 RF DAC)
  - RF digitizer daughter (8 RF ADC, 2 RF DAC)
- Remote daughter chassis
  - Baseband DAC (16 CH) plus digital I/O





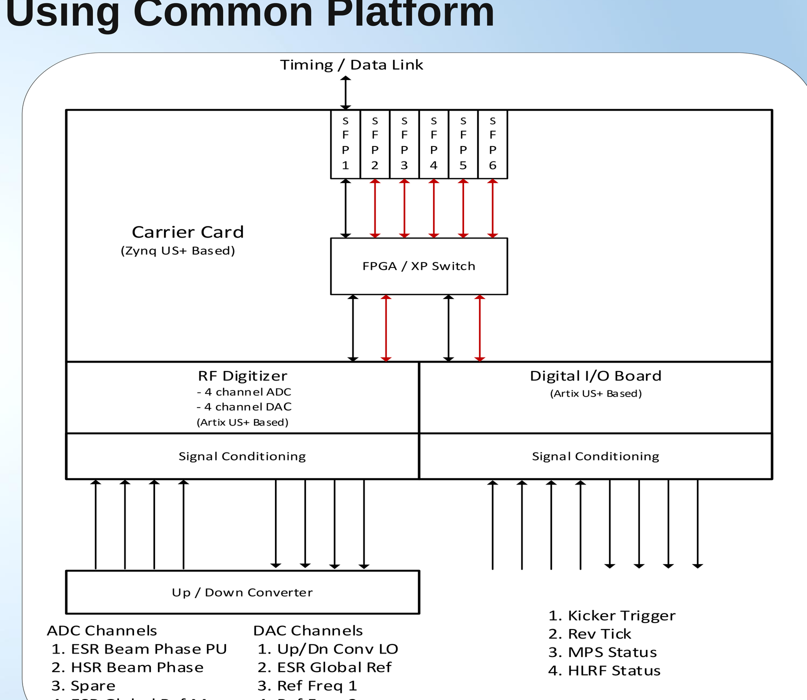
Carrier Options

- Standard carrier can include timing / data link hub functionality to create a local timing / data link for data isolation.
- 'Passive' carrier (or remote daughter) provides basic carrier/daughter interface functions without an FPGA on carrier.

System Specific and Generic Daughter Cards

- Digital I/O – provides real-time and beam synchronous timing
- Baseband ADC – 16 Channel, 1 MSPS
- Baseband DAC – 16 Channel, 1 MSPS
- RF ADC / DAC – 8 ADCs @125 MSPS, 2 DACs @500 MSPS
- SFP+ breakout – 12+ SFPs – ARTIX UltraScale+ based
- RF Cavity Controller – 4 ADCs @ 125 MSPS, 4 DACs @500 MSPS
- BPM Processor
- Power Supply Controller Interface

System / Cavity Controller Implementation Using Common Platform



References:

Electron-Ion Collider RF Systems
Kevin Mernick (BNL)

Ultra Low Noise Clock Distribution for Electron-Ion Collider Common Platform
Freddy Severino (BNL)