Ultra Low Noise Clock Distribution for the Electron-Ion Collider Common Platform

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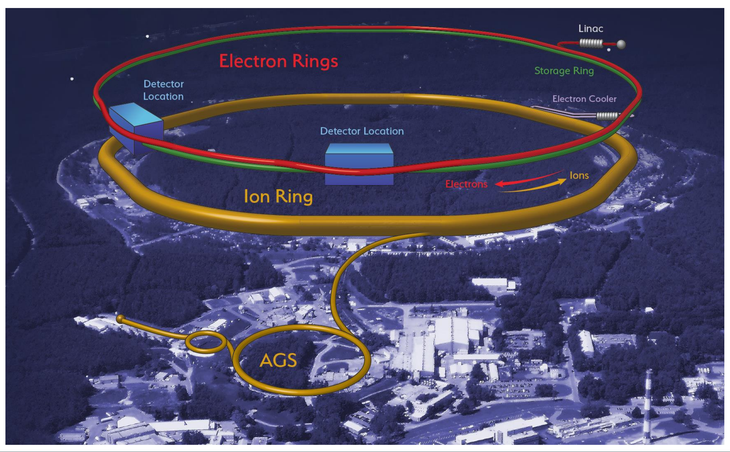
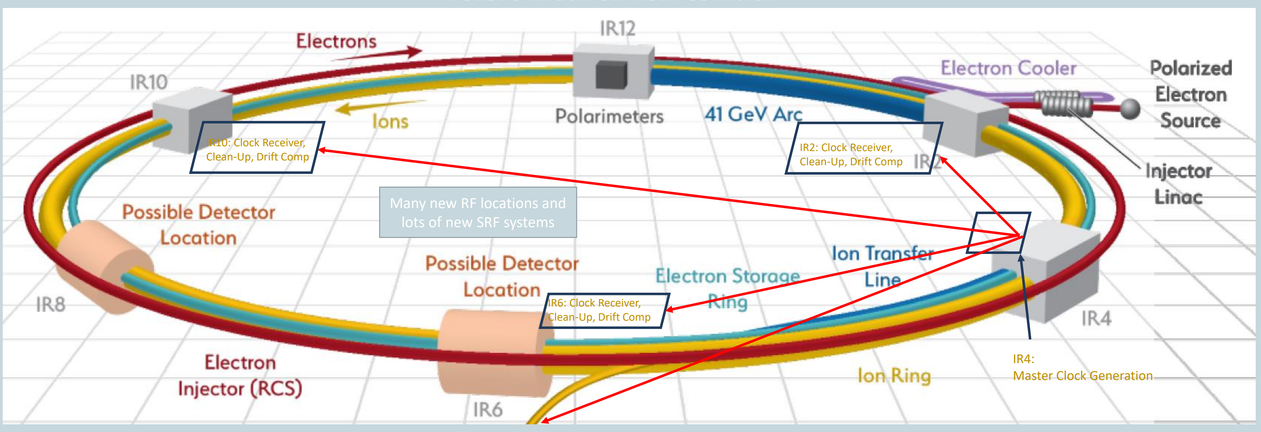


The Electron-Ion Collider (EIC), to be constructed at Brookhaven National Laboratory (BNL), is a roughly 10 year project to design and construct a facility to collide polarized high energy electron beams with polarized proton and heavy ion beams at center of mass energies from 20 GeV to 140 GeV and luminosity up to 10^{34} $cm^{-2}s^{-1}$. The project is a partnership between BNL and the Thomas Jefferson National Accelerator Facility (Jefferson Lab, JLAB). The EIC Common Platform (CP) is an effort to design and implement a flexible, high-performance electronics platform for required Low Level RF (LLRF), Timing, Machine Protection, Instrumentation, Power Supply, and general-purpose Accelerator Controls systems. The EIC CP, like its predecessor, the LLRF Platform used at BNL Collider-Accelerator since 2009, will rely on a common ultra-low-noise 100 MHz system clock for operation. We will be presenting the preliminary design work for clock generation, distribution and clean-up while paying special attention to the most challenging phase noise requirements of the EIC hadron storage ring (HSR) and crab cavities.

Common 100 MHz System Clock

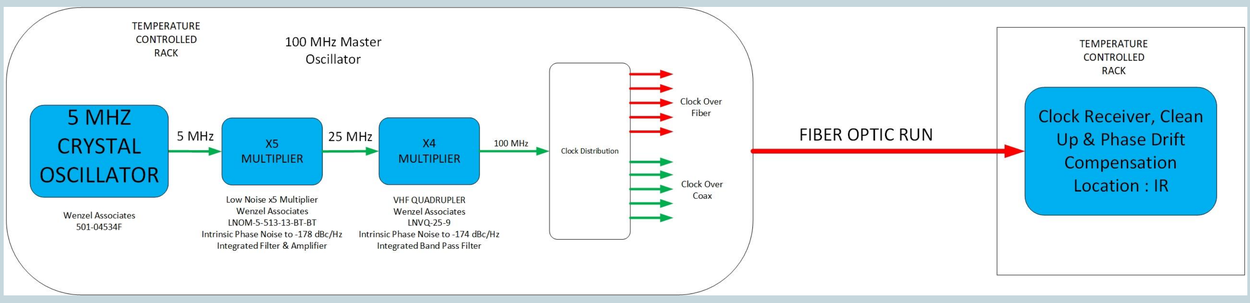
The EIC Common Platform will rely on a common ultra-low-noise 100 MHz system clock for operation. The 100 MHz system clock becomes the common reference (master oscillator) for all LLRF systems, and in concert with deterministic data-timing Link ensures a repeatable, deterministic relationship between all parts of the distributed LLRF system. The EIC LLRF like its predecessor, the RHIC LLRF, was designed to used fixed frequency sampling clock for the RF ADCs & DACs. This means, the system clock becomes the source for generating high-speed sampling clocks used within the LLRF Controllers and hence any noise on the system clock directly translates to the output of the RF DAC or RF ADC noise performance.

Future Electron-Ion Collider



Clock Distribution

The ultra low noise 100 MHz system clock, generated in the RF control room located at the machine interaction region 4 (IR4), will be distributed over fiber to each other IRs where the low-level controllers will reside.

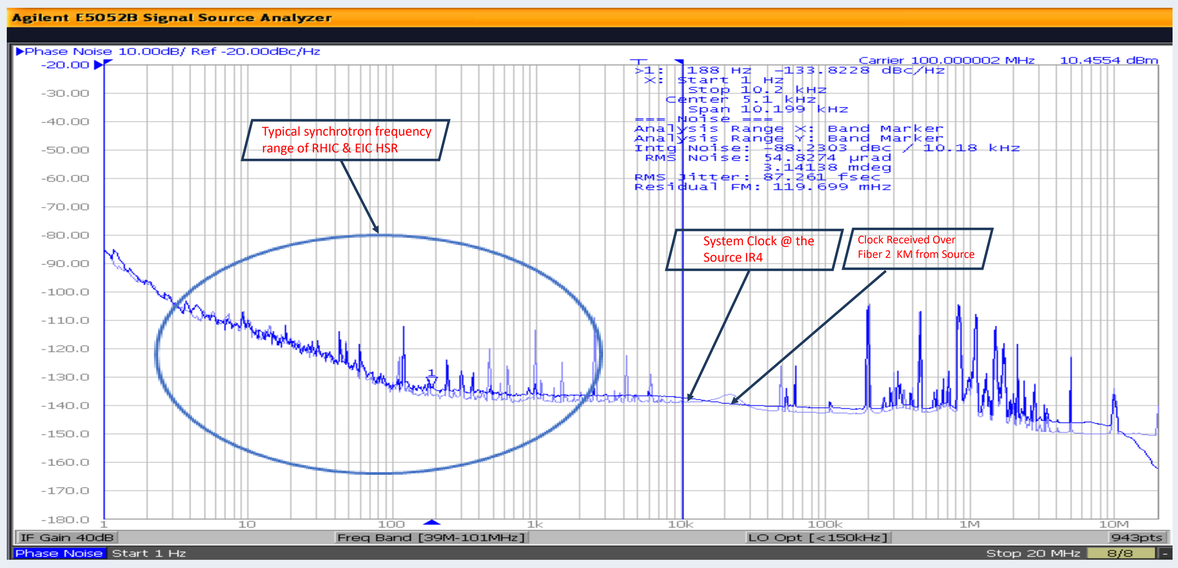


Master Oscillator Generation

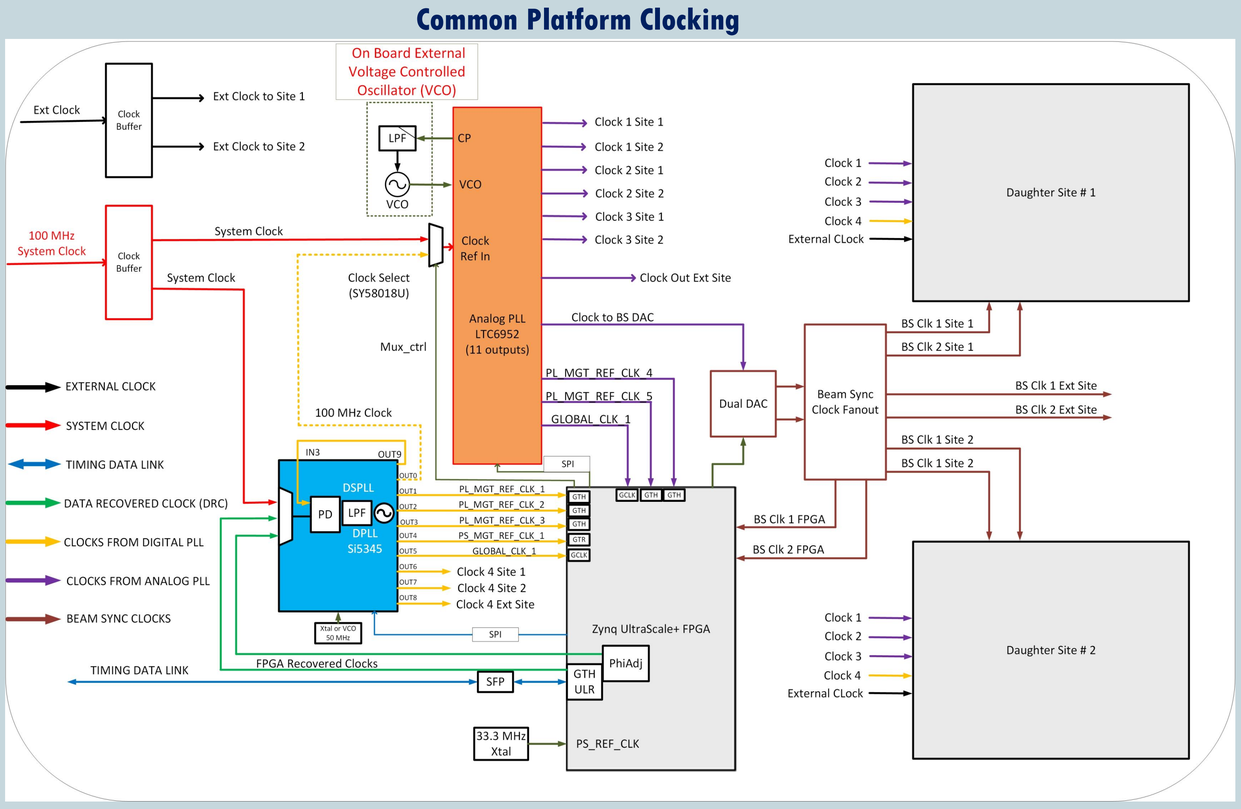
A 5 MHz Quartz Oscillator from Wenzel Associates was chosen as the main source for generating the system clock for RHIC since this offered the best close-in phase noise performance below 10 kHz. Any noise from the RF systems at the RHIC synchrotron frequency induces undesired beam emittance blow-up and de-bunching during the 12 hours RHIC stores. The final 100 MHz system clock was generated from the 5 MHz source using low noise frequency multipliers.

Generated System Clock Phase Noise

- ~ 87 fsec RMS Jitter (close-in phase noise 1Hz to 10 kHz)(RHIC synchrotron frequency range)
- -90 dBc/Hz @ 1 Hz , -110 dBc/Hz @ 10 Hz, -135 dBc/Hz @ 100 Hz,
- Clock distribution over fiber optic preserved close-in phase noise performance.
- Clean-Up PLL will be added at receiver end to clean noise above 10 kHz.



Common Platform Clocking



Common Platform Clocking Features

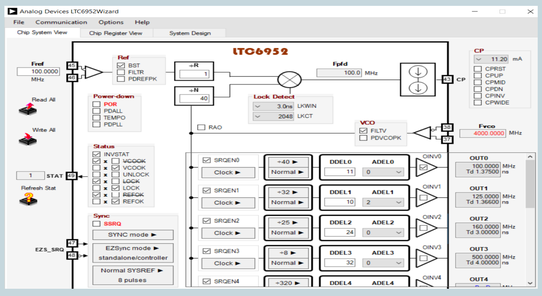
- System clock, External Clock
- Digital PLL for data clock recovery based on Si5345.
- Clean-Up PLL based on LTC6952
- PLL programming from FPGA over SPI
- On board generation of beam synchronous clocks (2)

Si5345 DPLL Features

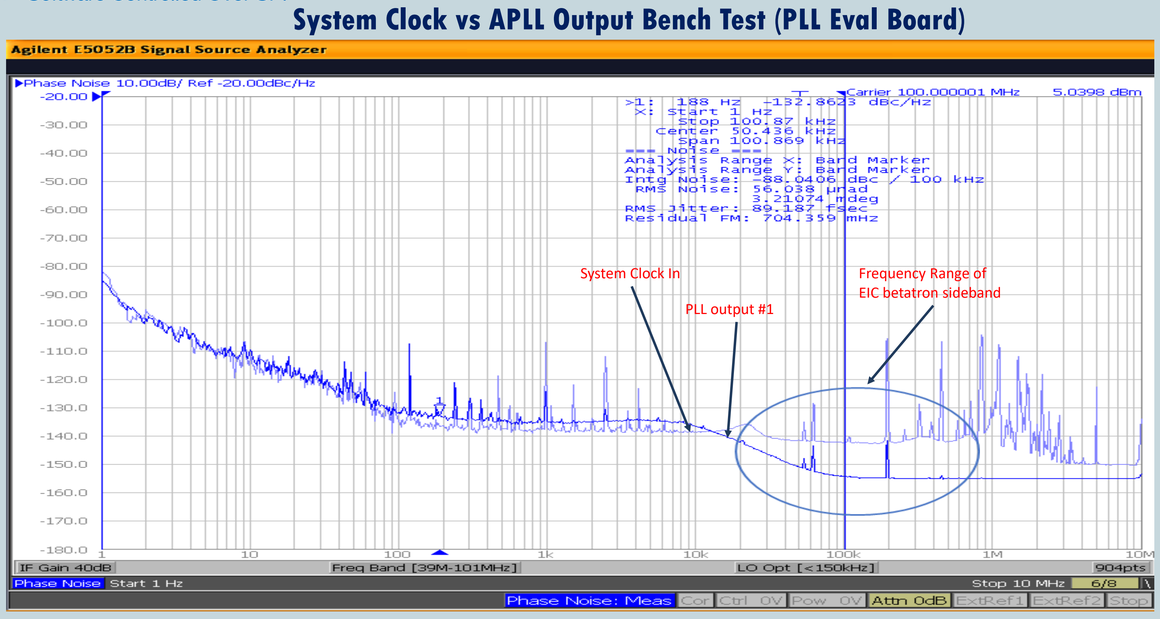
- Free-run and holdover modes
- Hitless input clock switching: automatic or manual
- Zero delay mode (data clock recovery)
- Ultra-low jitter of 90 fs rms (12 kHz to 20 MHz)
- Generates any combination of output frequencies from any input frequency, 156.125 MHz to support 10 Gb Ethernet.
- Software Controlled Over SPI

LTC6952 PLL Features

- Low Noise Integer-N PLL
- Additive Output Jitter < 6fs RMS (Int. BW=12kHz-20MHz)
- Additive Output Jitter 65 fs RMS (ADC SNR Method)
- -229dBc/Hz Normalized In-Band Phase Noise Floor
- -281dBc/Hz Normalized In-Band 1/f Noise
- Eleven Independent, Low Noise Outputs with Programmable Coarse Digital and Fine Analog Delays
- Synchronized and precise phase alignment to reference clock
- External VCO support with VCO frequency up to 4.5 GHz
- VCO & External low-pass filter provides low noise, very flexible clocking schemes
- Selectable Loop Bandwidth
- Software Controlled Over SPI



System Clock vs APLL Output Bench Test (PLL Eval Board)



EIC Crab Cavities RF Noise

The system clock for the EIC will need to maintain very low RF noise levels at the betatron sidebands for the RF system driving the crab cavities. Any noise introduced by system clock to the crab cavities RF systems will generate transverse emittance growth and potentially limit luminosity lifetime. Current estimates of phase noise requirements for the crab RF systems requires keeping phase noise below -150 dBc/Hz in the betatron frequency range (> 20 kHz) [1].

Current & Future Developments

- Finish common platform carrier board design
- Implementation of Cable drift compensation
- Add GPS discipline to System Clock Generation

REFERENCES

[1] K. Smith, T. Mastoridis, et al, "EIC Transverse emittance growth due to crab cavity RF noise: Estimates and mitigation", BNL-222748-2022-TECH, EIC-ADD-TN-026, Feb 02, 2022.

Other EIC RF Presentations:

Talk:
"Electron-Ion Collider RF Systems", Kevin Mernick (BNL)

Poster:
"Electron-Ion Collider Common Platform System Architecture", Geetha Narayan (BNL)

Low Level RF Workshop 2022
9-13 Oct 2022, Brugg-Windisch, Switzerland

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Electron-Ion Collider

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