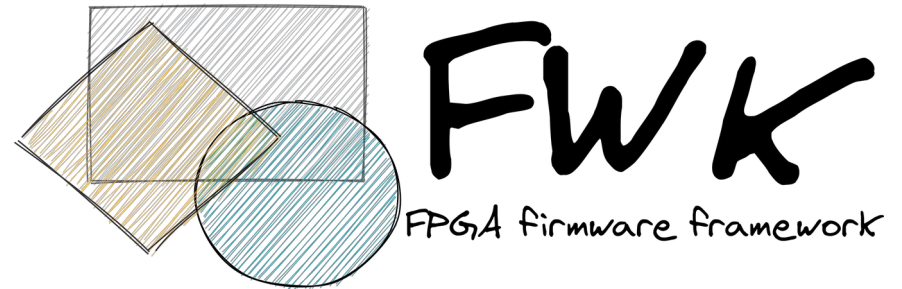


# DESY FPGA Firmware Framework

Open Source



**Lukasz Butkowski**

MSK (Machine Beam Control Group) Firmware Team, DESY

LLRF 2022, Breeg, 12.10.2022

# Overview

- Short history
- Framework overview
- Framework structure
- Address space generation
- Open Source License

# FPGA Firmware Framework

## Background

### Started in 2013 for LLRF

- Currently it is used to provide firmware for:
  - LLRF Regulation of many facilities in and outside of DESY: EuXFEL, FLASH, TARLA, HZDR, HZB, REGAE...
  - Laser Synchronization in EuXFEL
  - Special Diagnostics in EuXFEL, FLASH
  - Cavity Tuning (Motors and Piezo) in EuXFEL
  - ...
- Allowed to manage ~100 projects with 500 000 lines of VHDL code base and 45 contributors.
- Problem: everything in mono repository – easy to maintain but difficult to share, reuse and distribute

### 2019 decision:

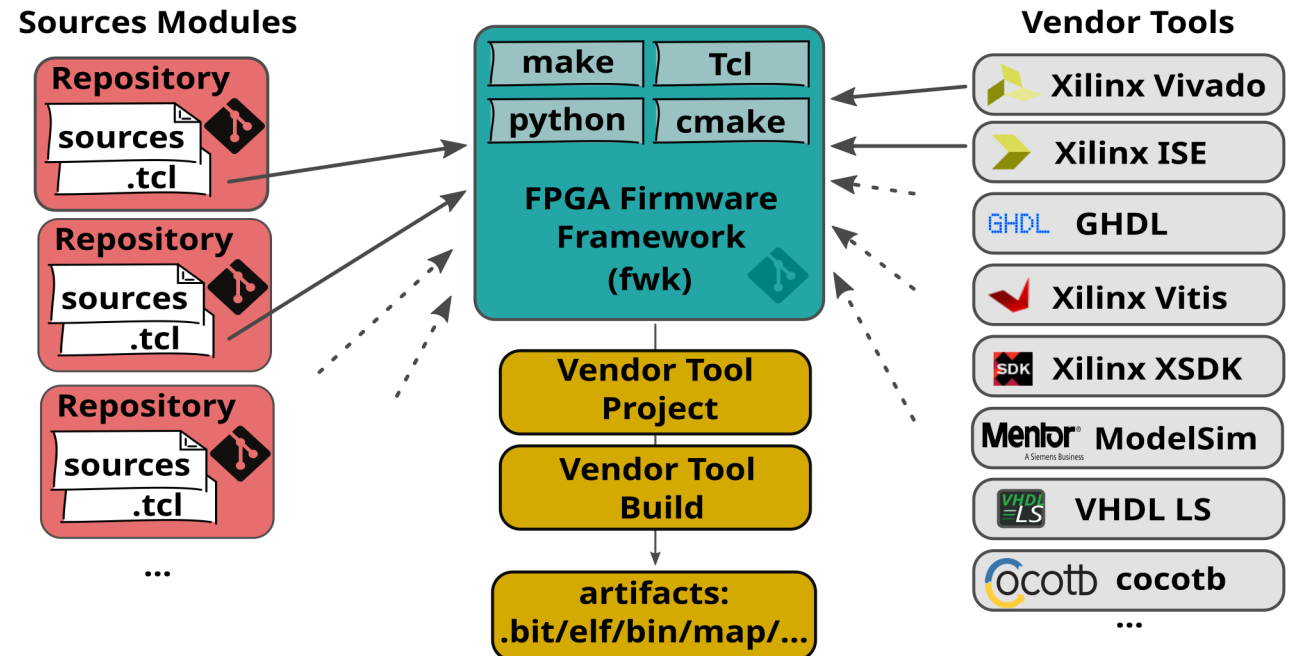
- decouple framework from the code base and make it open source
- restructure, improve and make more modular

# Firmware Framework Structure

- Firmware framework (FWK) is a set of rules, structures, script and tools that give an abstraction layer.
- It is based on Tcl scripts with backend for each vendor. Makefile as a start point. python as extensions
- Each source module is a separate git repository with source files and FWK defined Tcl script.

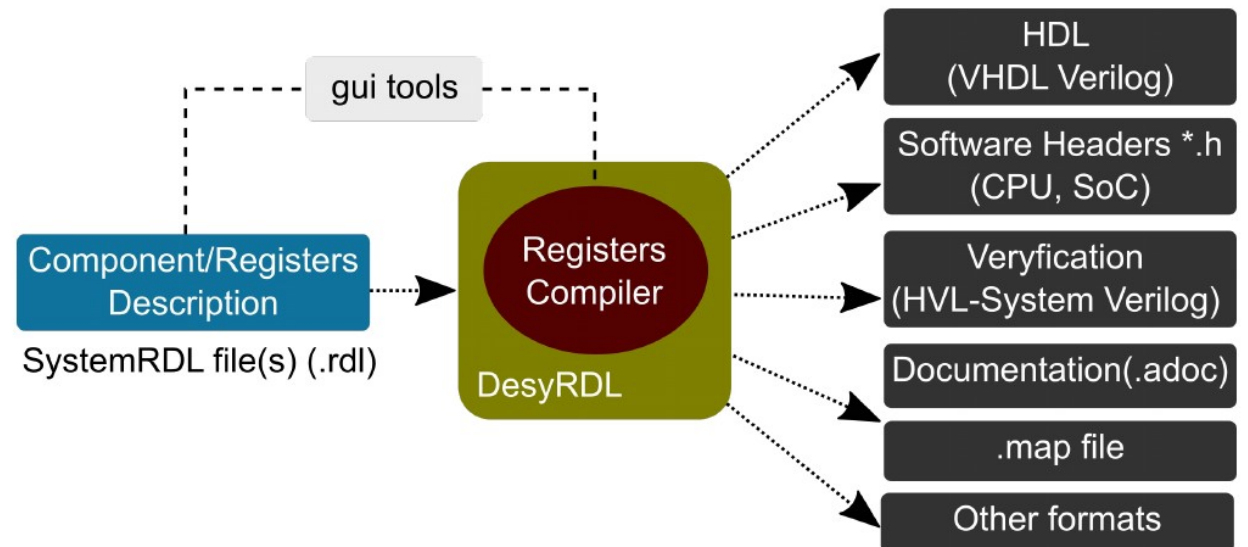
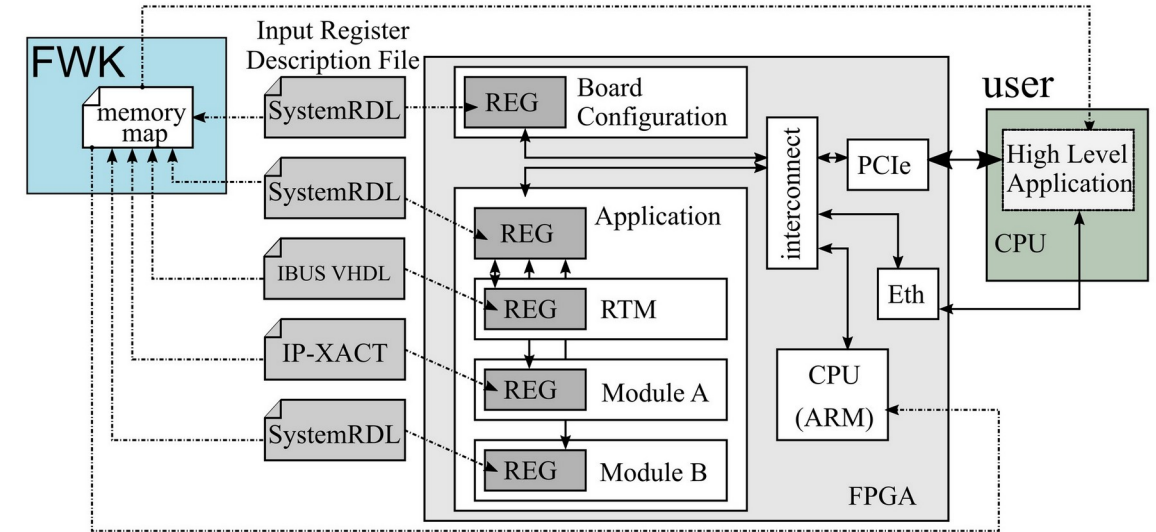
The main features of the framework :

- Multiple vendor tools support
- The same way of building the firmware
- Allows easy regeneration of projects
- Constructs an address space for the SW (also link with software : ChimeraTK)
- Generates documentation
- Integrates HW and SW part of the FPGAs
- Automated versioning
- Continuous integration ready (Jenkins, Gitlab CI)
- ...



# Address Space Generation

- **SystemRDL** is an open source industry standard for register description. It is the main register and address space description format in framework.
- **SystemRDL-compiler** open source compiler written in python (available on pip)
- **DesyRDL** is the open source tool that uses SystemRDL compiler to produce the output artifacts such as VHDL code, documentation, map file. (available on pip)
- Framework supports various address space formats which are converted to SystemRDL and then compiled
- It is possible to use other address space tool backend



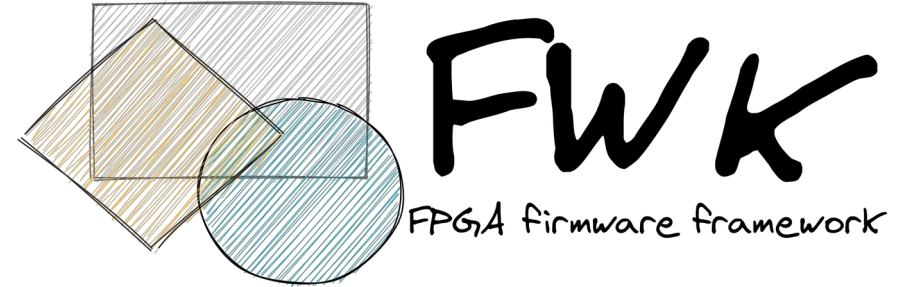
# Open Source

- Why we want open source
  - Make the collaboration easier
  - Get wider feedback on our work
  - Promote our work
  - Try to not “reinvent the wheel”
- Problems
  - Where to publish
  - Which license to pick
  - How to get outside work back
  - How much manpower to assign

# Open Source

## Firmware

- Firmware framework published at DESY Gitlab in Feb. 2022
  - Exact location not fully decided, might change in future.
- Plan to publish all board support packages (BSPs), libraries and example designs
- Main repository: <https://gitlab.desy.de/fpgafw/fwkw>
- Documentation page: <https://fpgafw.pages.desy.de/docs-pub/fwkw/index.html>
- License, tools and frameworks: [Apache-2.0](#)
- License: HDL code: [CERN-OHL-W-2.0](#)



## Software

- Software framework available on github since 2013  
<https://github.com/ChimeraTK>
- License: LGPL-3.0



# Thank you

## Contact

Deutsches Elektronen-  
Synchrotron DESY

[www.desy.de](http://www.desy.de)

Lukasz Butkowski  
MSK (Machine Beam Control group) DESY  
[lukasz.butkowski@desy.de](mailto:lukasz.butkowski@desy.de)