

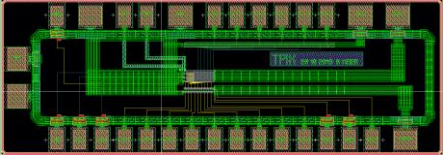
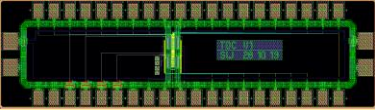
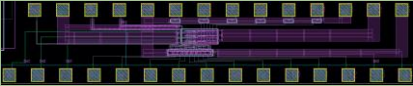
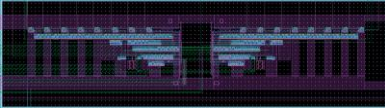
PAUL SCHERRER INSTITUT



Beat Meier :: Paul Scherrer Institut

# TDC Development at PSI and UZH

Chip Design Meeting 20. Juni 2022

		TPIX Analog Ring Readout <i>Layout: Beat Meier</i> <i>Test: Matías Senger, Beat Meier</i>	TDC Digital Ring Readout <i>Layout: Stephan Wiederkehr</i> <i>Test: Matías Senger</i>	ATDC no Ring Readout <i>Layout: Wolfram Erdmann</i> <i>Test: A. Ebrahimi, W. Erdmann</i>
TECHNOLOGY	UMC110			
	LF110			

# Time Resolution Requirements

CMS TEPX timing layer **30 ps**

- Low Gain Avalanche Detectors LGAD preferred
- Project with UZH

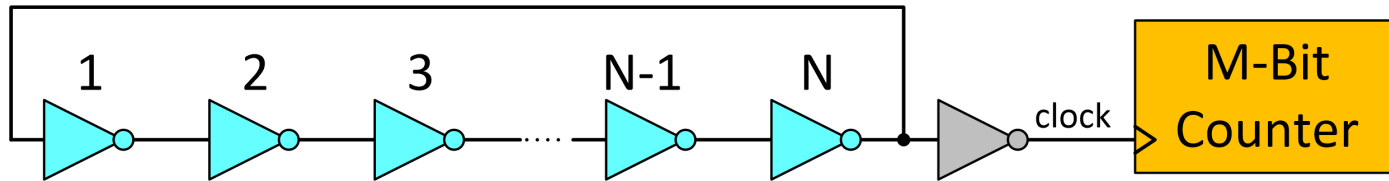
Other Projects: **100 ps**

# TDC Based on Ring Oscillator and Counter

Ring oscillator controlled by

**START** (pixel hit)

**STOP** (reference clock)



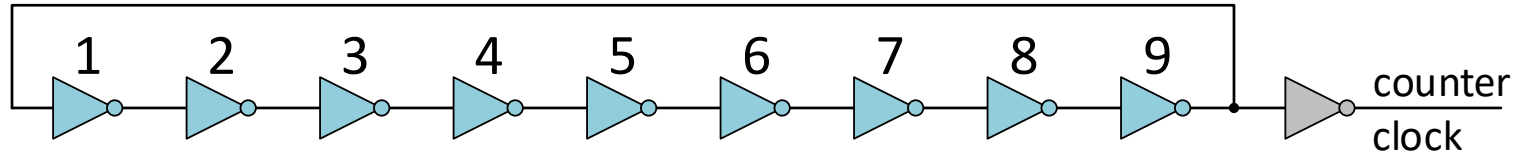
Ring Readout (snapshot)  
**Fine resolution  $> t_{PD}$**

Cycle Counter Readout  
**Coarse resolution  $> 1$  ns**

Example:

- Propagation delay: 60 ps
- $N = 9$ :  $T = 1$  ns;  $f = 1$  GHz

# Ring Oscillator Gate Propagation Delay $t_{PD}$



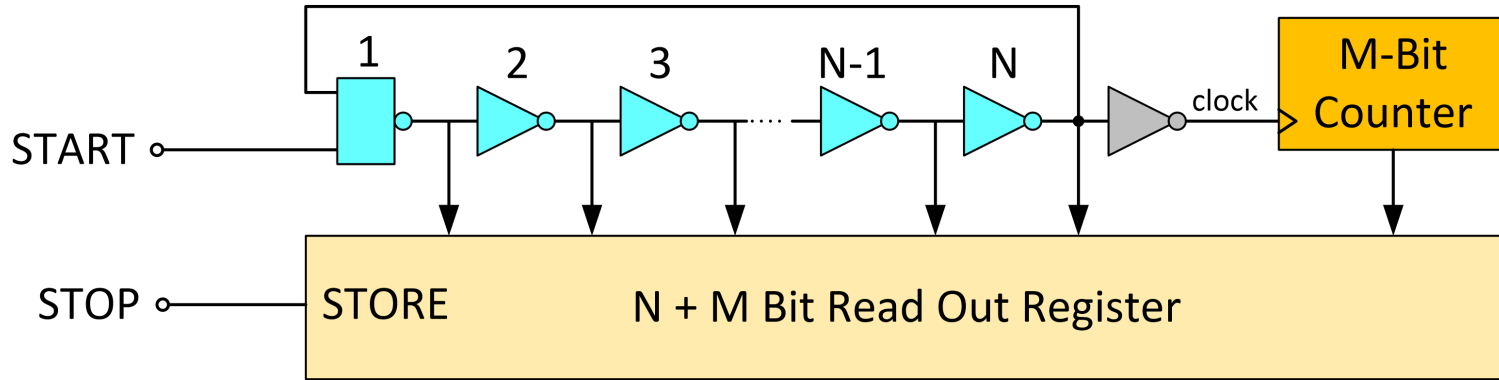
LF		124	114	111	111	110	108	108	113	141	ps
		68	64	48	45	48	45	47	51	100	ps
UMC		114	88	110	109	92	99	98	111	133	ps
		51	37	36	36	35	42	32	29	96	ps

TPIX; enclosed transistors nand gates; VDD = 1.2 V

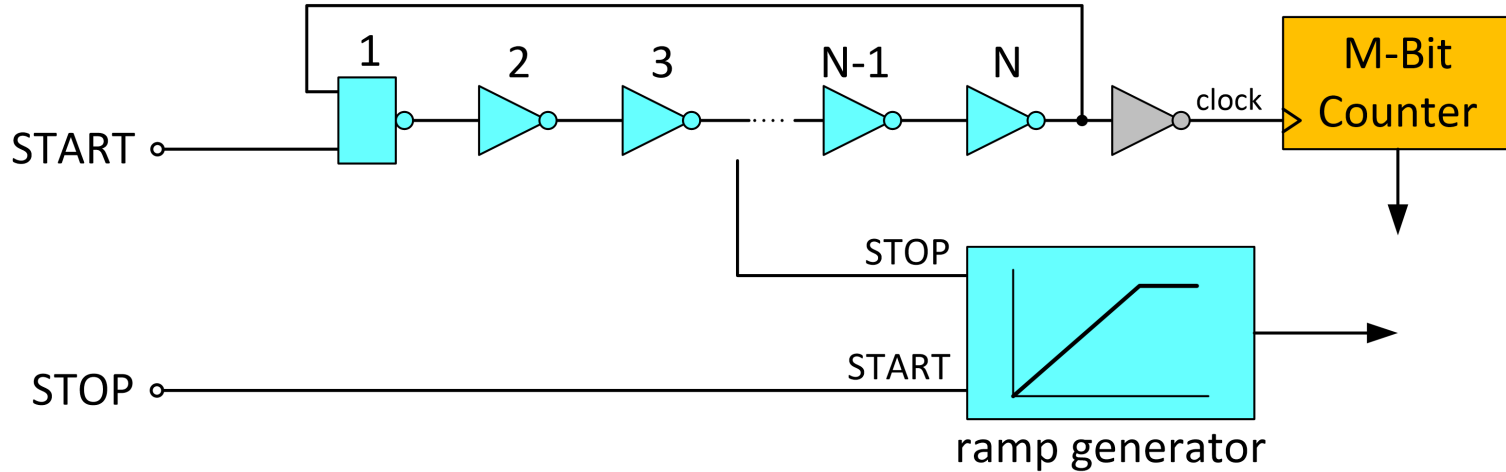
LF110 T = 1550 ps (645 MHz)  $t_{PD} = 86$  ps

UMC110 T = 1350 ps (740 MHz)  $t_{PD} = 75$  ps

# TDC Fully Digital Readout



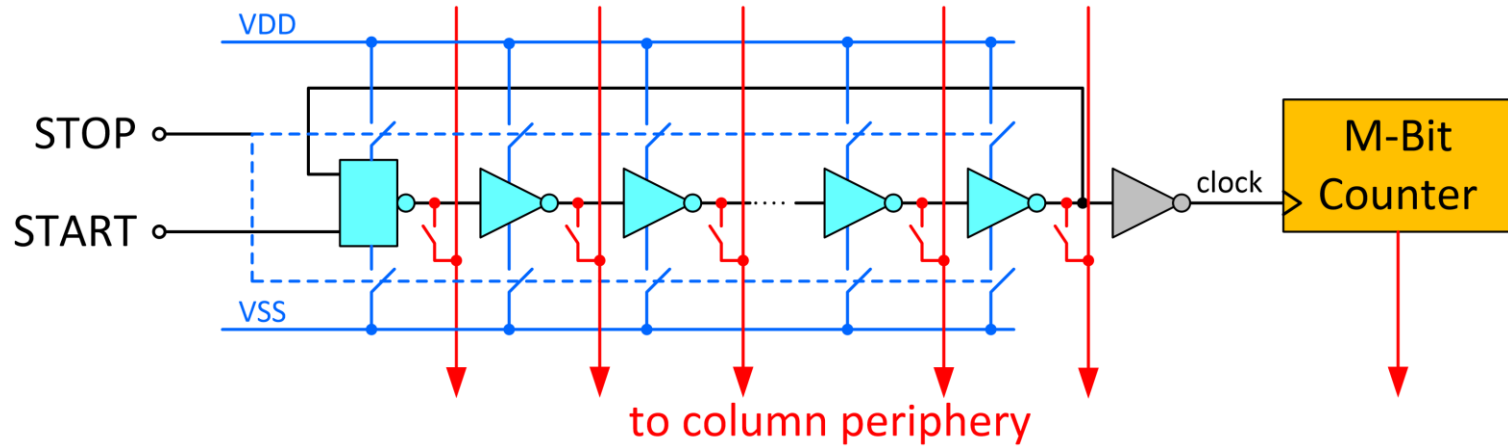
- Easy to read out; fully digital; No ADC needed
- Huge size; only for big pixel or in periphery
- High capacitive load of ring oscillator  $\rightarrow$  high  $t_{pD} \approx 100$  ps
- $t_{pD}$  resolution limit (can be reduced only with another technology)
- common TDC designs



- no ring oscillator readout
- After stop, ring runs to the end
- I-C Ramp generator for sub ns resolution

- no  $T_{PD}$  resolution limit
- time resolution limited by nonlinearity, noise of ramp generator, calibration
- higher resolution ADC for analog read out (6 bit or more)

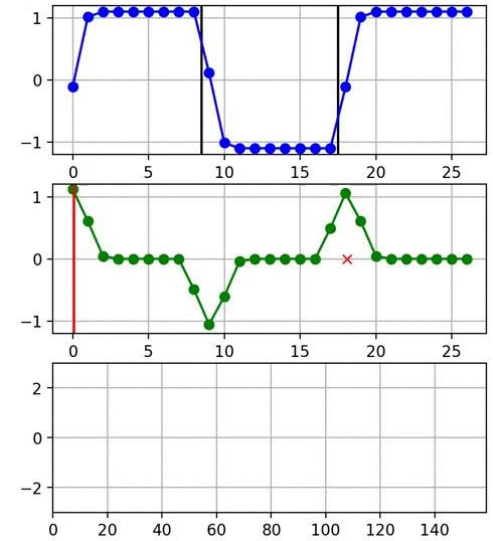
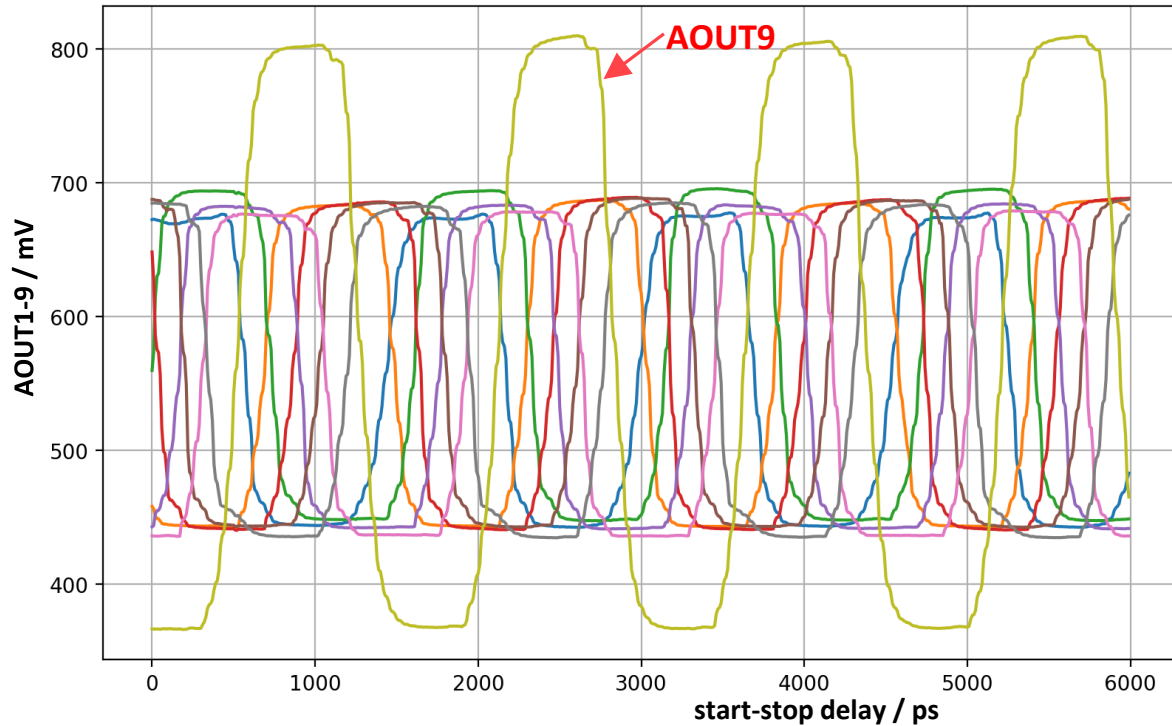
# TPIX: Analog Ring Readout



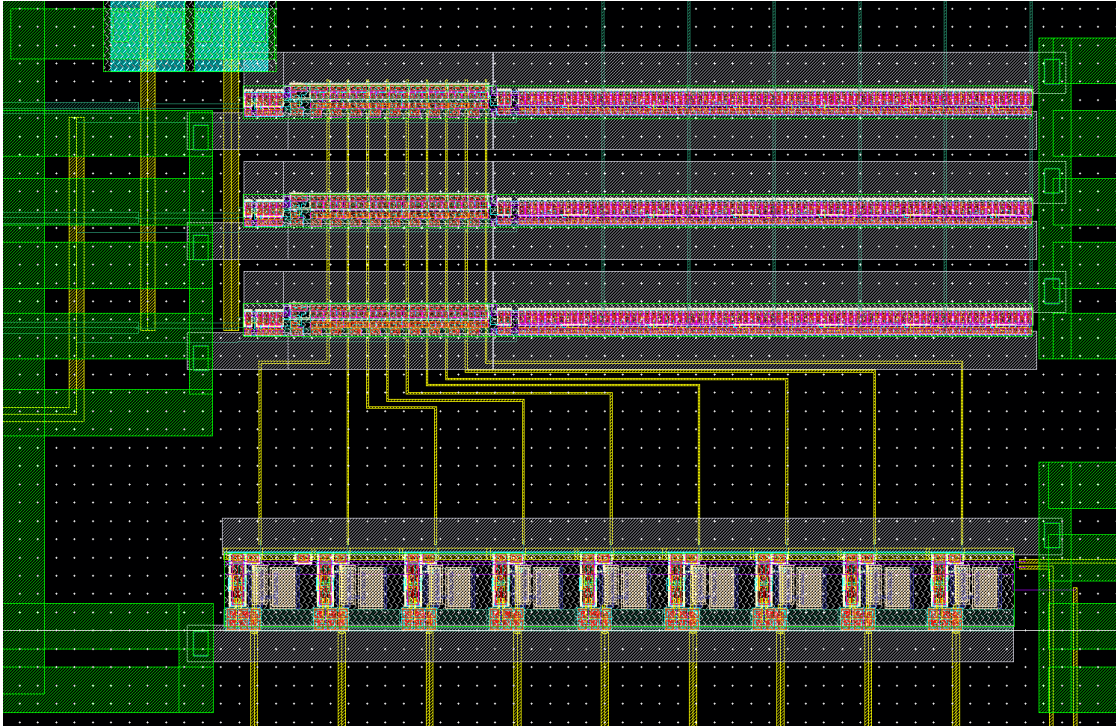
- Charge storage in ring oscillator
- Charge readout of a full column like a analog storage cell
- Minimal circuitry for read out
- minimal size; 50  $\mu\text{m}$  x 25  $\mu\text{m}$
- digital readout:  $t_{pD}$  resolution limit
- analog readout: sub  $T_{pD}$  resolution
- only 2 bit ADC needed
- High effort for analog interpolation in periphery (not yet solved)
- Non uniformity of the ring oscillator



# TPIX: Analog Read Out



# TPIX required Space in Pixel (UMC)



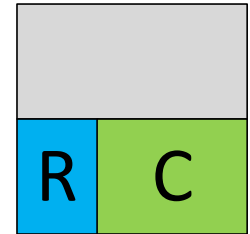
ring stage  $4.86 \times 9.1 = 44.2 \text{ um}^2$   
 ring  $9 \times 44.2 \text{ um}^2 = 398 \text{ um}^2$   
 ring interface  $5.5 \times 9.1 = 50 \text{ um}^2$   
**ring area: 450 um<sup>2</sup> 36%**

counter stage  $21.1 \times 6 = 126.6 \text{ um}^2$   
 counter (6 stages)  $760 \text{ um}^2$   
 counter interface  $8.3 \times 6 = 50 \text{ um}^2$   
**counter area: 810 um<sup>2</sup> 64%**

**Total area: 1260 um<sup>2</sup> 100%**

50 um Pixel

50 x 25 um<sup>2</sup>



So far:

- Isolated test structures
- Ideal START/STOP signals from a test system

MOTIC Chip (*Stephan Burkhalter*):

- MAPS demonstrator, IFoundry
- Full pixel array
- ATDC (with analog readout) per pixel group
- Order of some 100 ps resolution ok. MAPS rather slow

LGAD sensor readout (*Matías Senger UZH*):

- Readout amplifier under test stagnates due to lack of components for the tester
- Test with LGAD + preamp/comp + TDC in Preparation

## Integration in a readout chip: PROC600 with TDC?

- Which readout architecture?
- TDC per Pixel? Per Column? Per Chip?
- TDC architecture is highly dependent on the application
- It is not useful to spend a lot of time in a “fantasy” architecture

Applications  
needed

## Change to 65 nm technology

- for lower  $t_{pD}$
- to reach 30 ps resolution with digital TDC
- no analog readout (ADC) needed with TPIX
- PSI already signed NDAs for TSMC 65nm and UMC 65nm (*Roberto*)
- CERN NDA for TSMC 65nm where I have access

New  
Technology