PAUL SCHERRER INSTITUT

Wir schaffen Wissen – heute für morgen

Paul Scherrer Institut

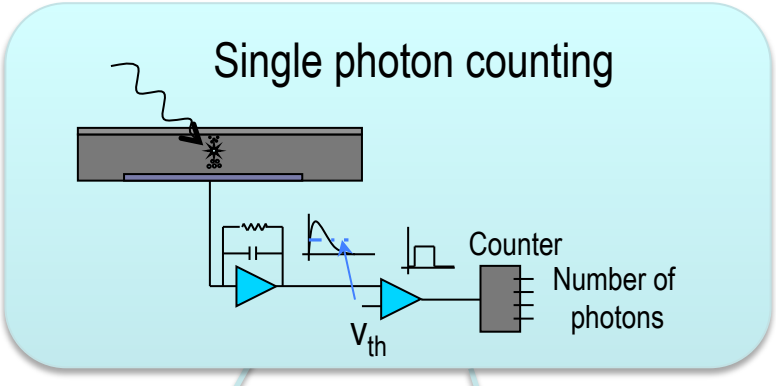
Ian Johnson

SLS Detector group

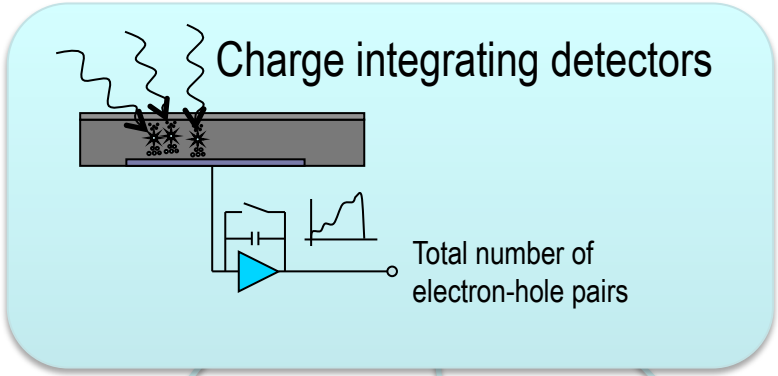
Eiger, a fast framing, large area pixel detector for X-ray applications

Projects within the SLS Detector group

Synchrotron detectors

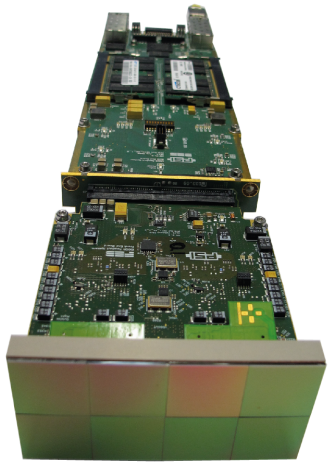


X-ray free-electron laser detectors

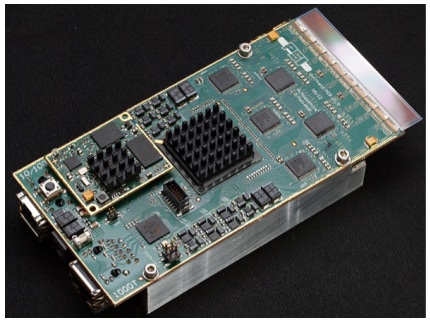


Mythen II

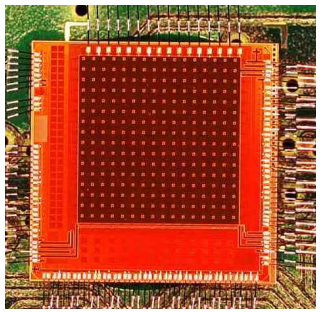
Eiger



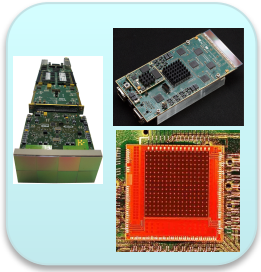
Gotthard



AGIPD



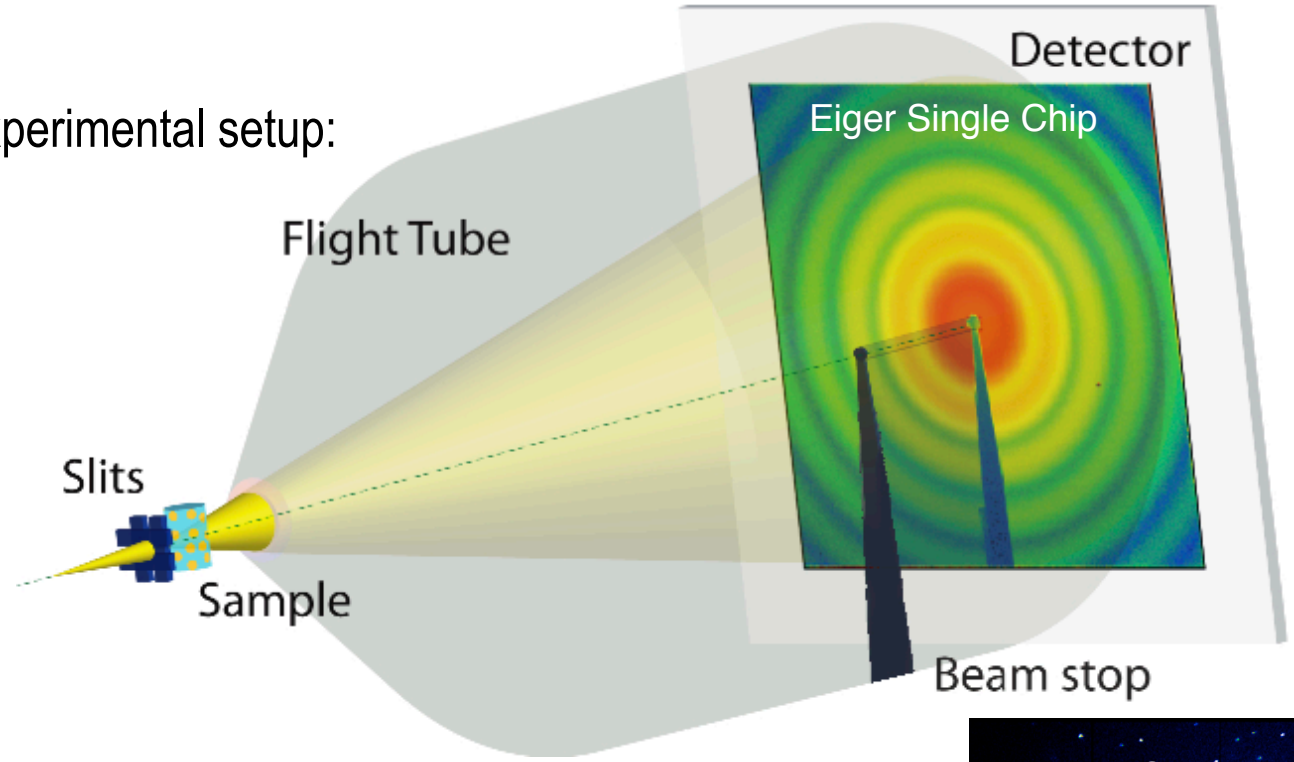
SwissFEL



A. Mozzanica - Charge integrating silicon detectors for SwissFEL (@ 16:25)
J. Becker (DESY) - AGIPD, A 4.5 MHz camera for the European XFEL (@ 15:10)
H. Billich - Data backend system for fast multi megapixel detectors (Sat. 10:30)

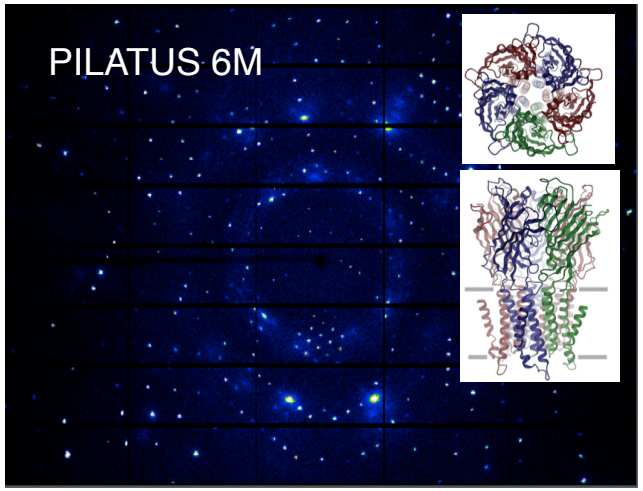
Eiger is aimed towards Diffractive experiments

Typical experimental setup:



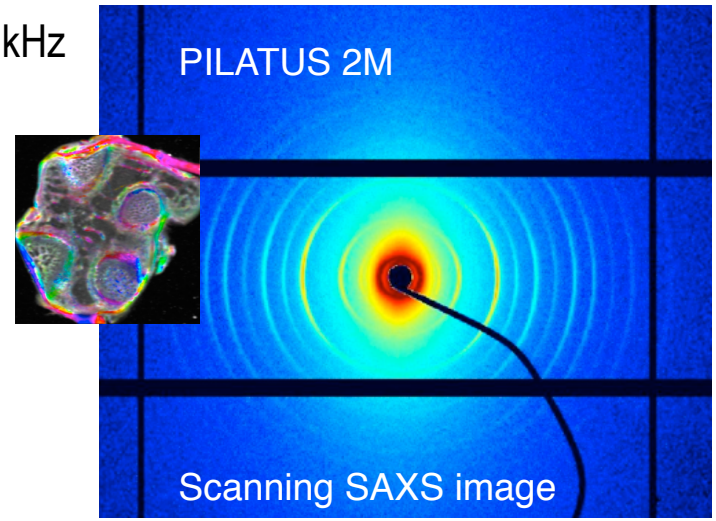
Typical applications:

- Protein Crystallography
- Small Angle X-ray Scattering (SAXS)
- Coherent Diffractive Imaging (CDI)
- X-ray Photon Correlation Spectroscopy (XPCS)



Requirements

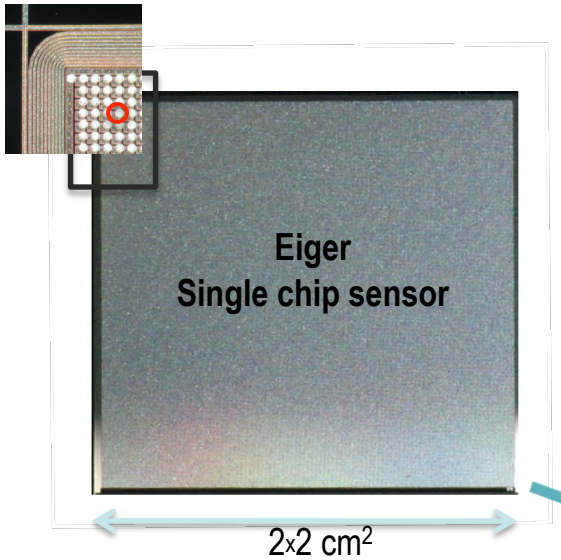
- X-ray sensitive pixels
  - Energy range few keV to 20 keV
- Single photon sensitivity
  - Low to no noise
- Sufficient angular coverage
  - Large area detectors
- Millions of small (75 um) pixels
- High dynamic range
  - Count rates up to 1-2 million counts/pixel/second
- High frame rates
  - Tens of kHz

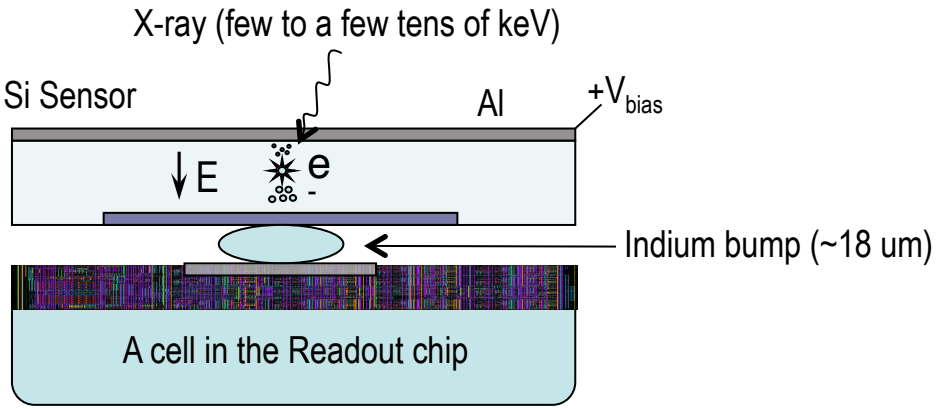


The Eiger chip

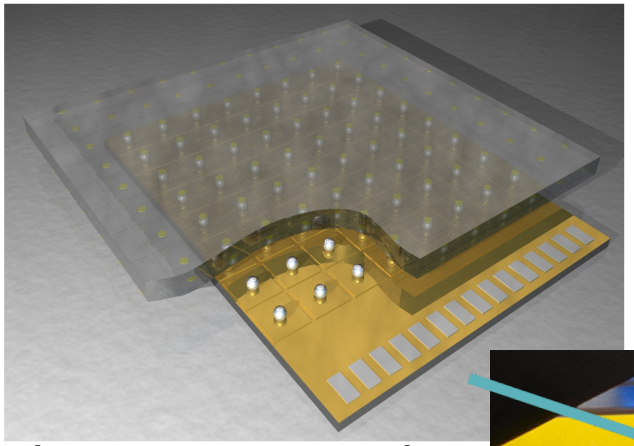
Chip size	19.3 x 20.1 mm^2
Pixel array	256 x 256 = 65536 pixels
Pixel size	75 x 75 μm^2
Analog Parameters (simulated)	30 ns peaking time Timing: 151 ns (Return to 0@1%) Noise: 135 e-rms Gain: 44.6 µV/e- Static Power: 8.8 µW/pixel (0.6 W/chip)
Count rate	10^6 X-rays/pixel/s
Threshold adjustments	Global threshold + 6 Trimbits/pixel
Binary counter	Configurable to 4, 8, and 12 bit with overflow control
Double buffering	Counter values stored in pixel cell Negligible dead time (~ 3 µs)
Frame rates	~23 kHz in 4 bit mode
Technological process	UMC 0.25 µm; Rad tol. Design > 4 MRad
Transistors matrix Periphery Transistor density	28.44 M > 120 000 430/pixel

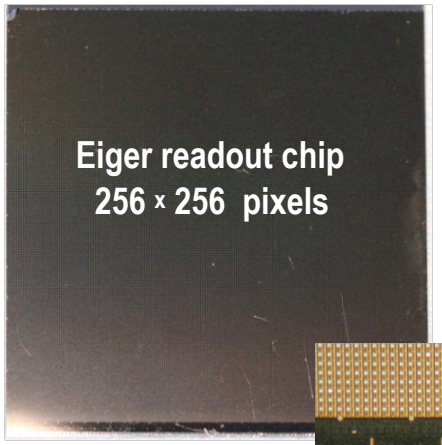
Hybrid pixel detector





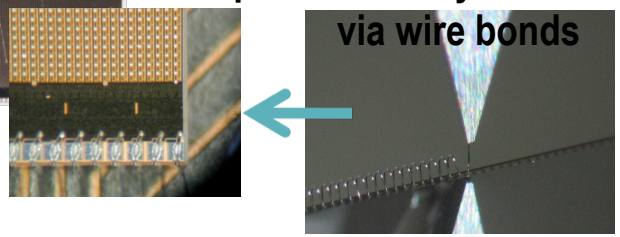
Sensor – Chip connected via bump-bonds



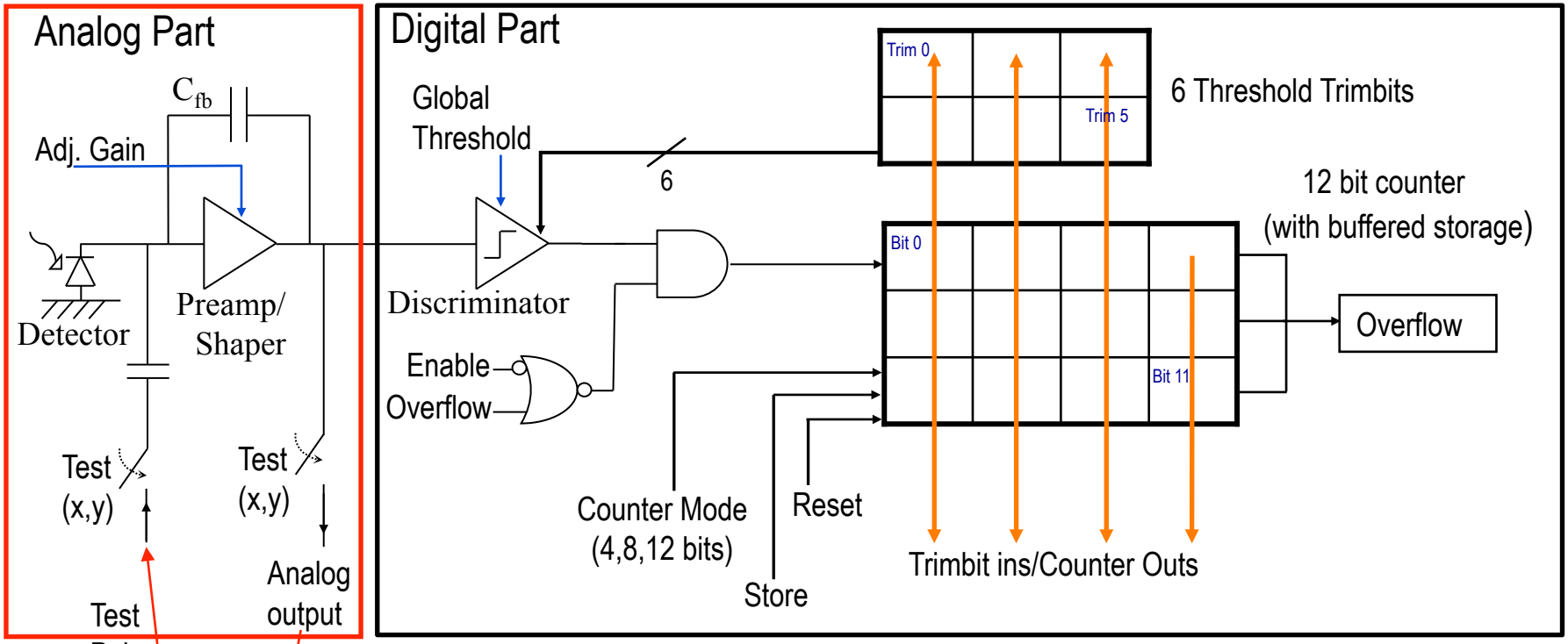


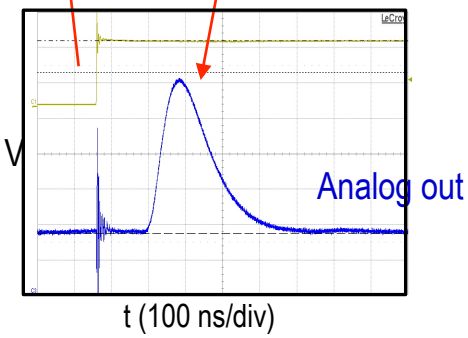
A PSI bump-bonder

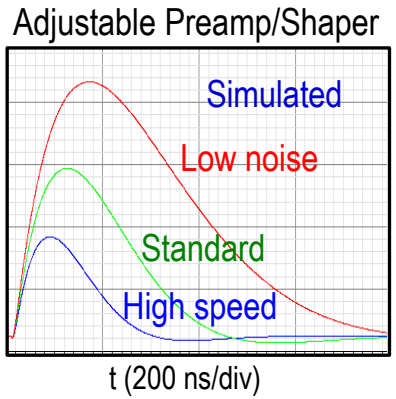
Chip - Readout system connected via wire bonds



Functionality in each pixel

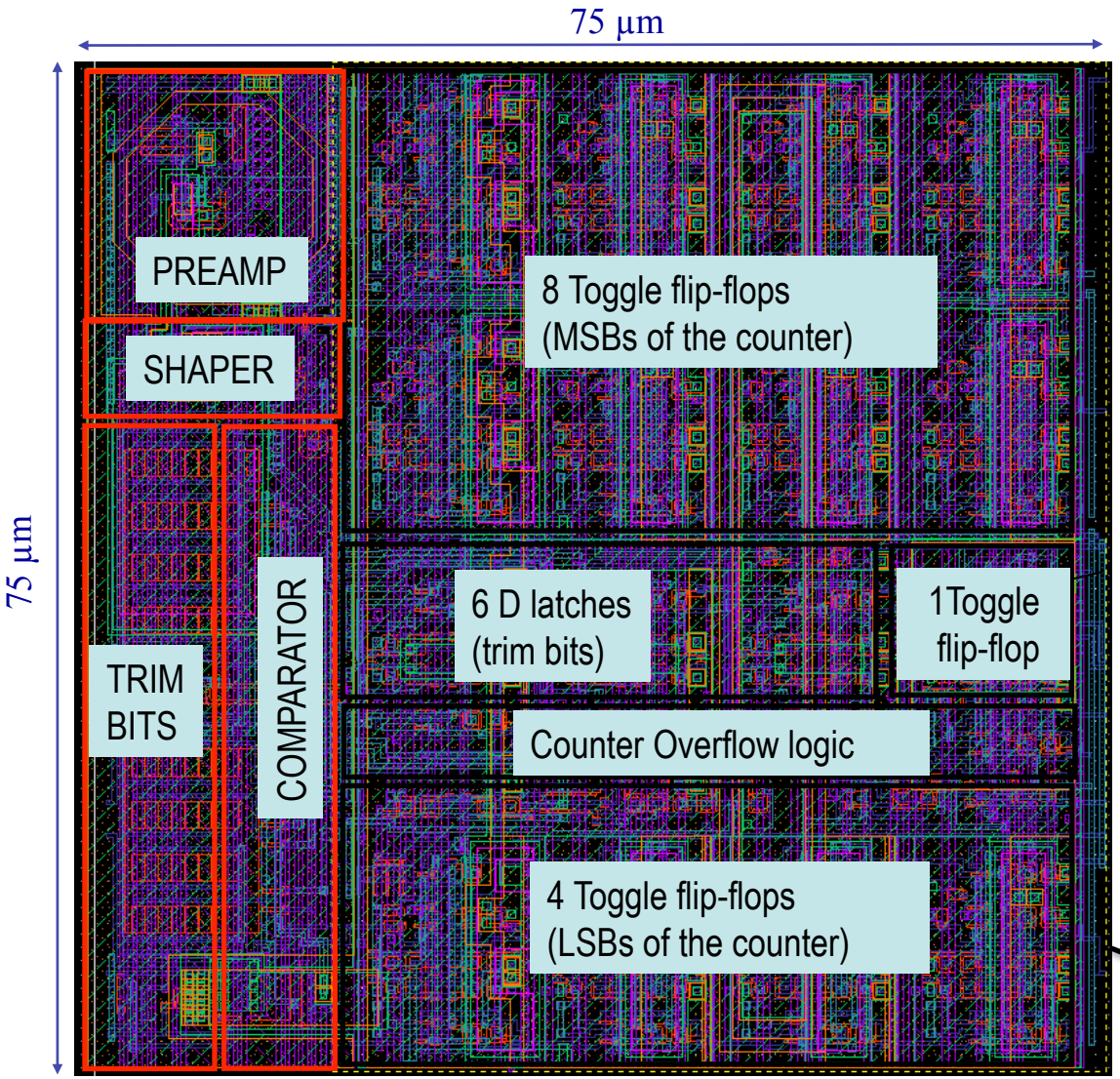






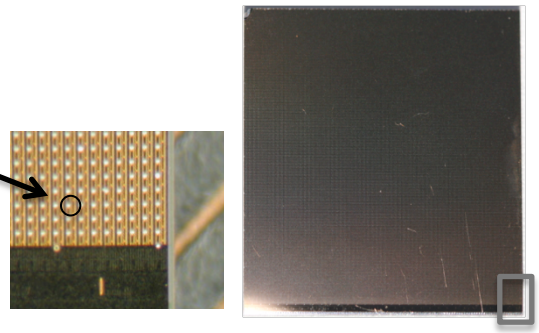
- Global threshold + 6 trimbits
- Adjustable gain

A pixel in Silicon

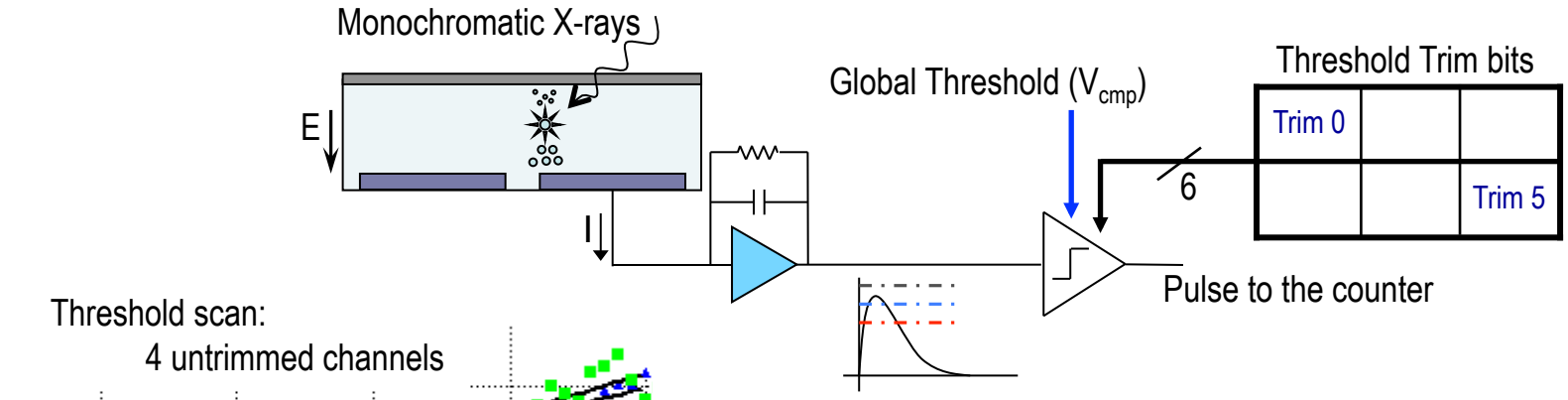


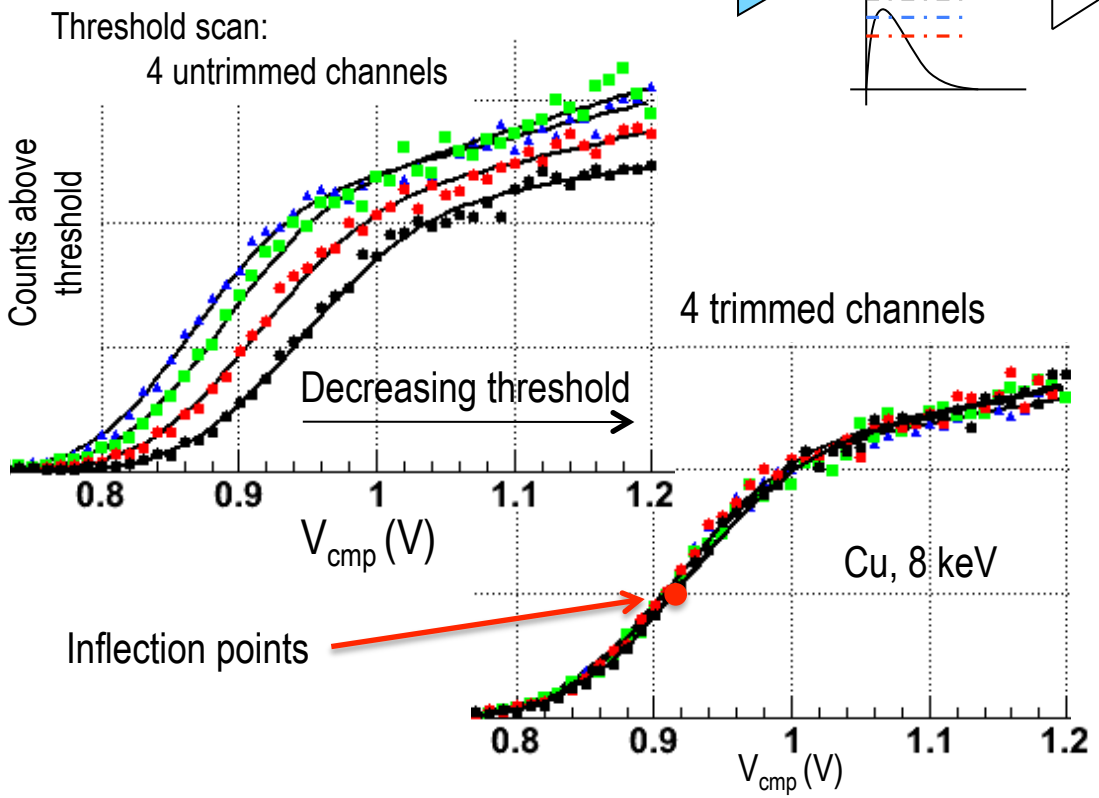
UMC 0.25 µm Technology

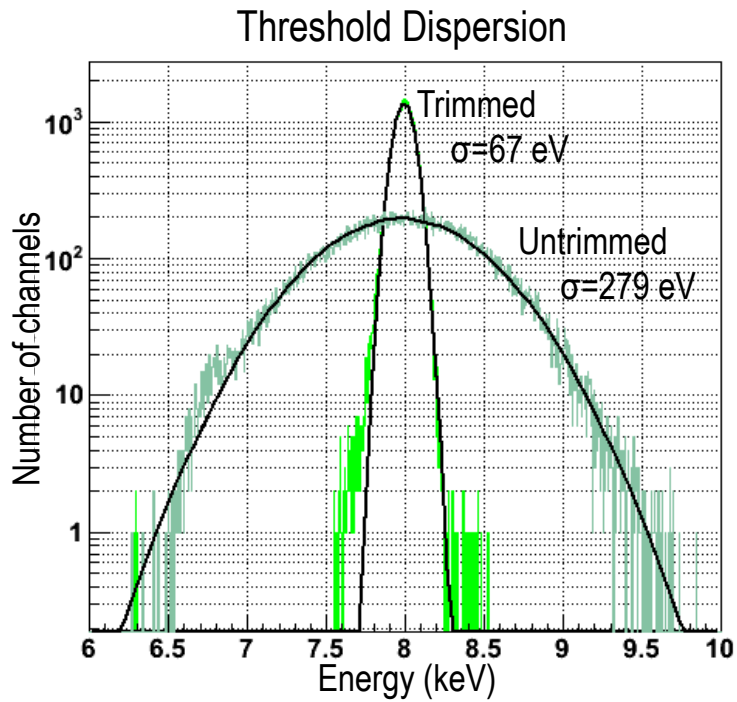
- Bump bond connection
- Preamp/shaper
- Trim Bits
- Comparator
- 12 bit counter
- Counter bit buffers
- Overflow logic



Trimming and Response uniformity

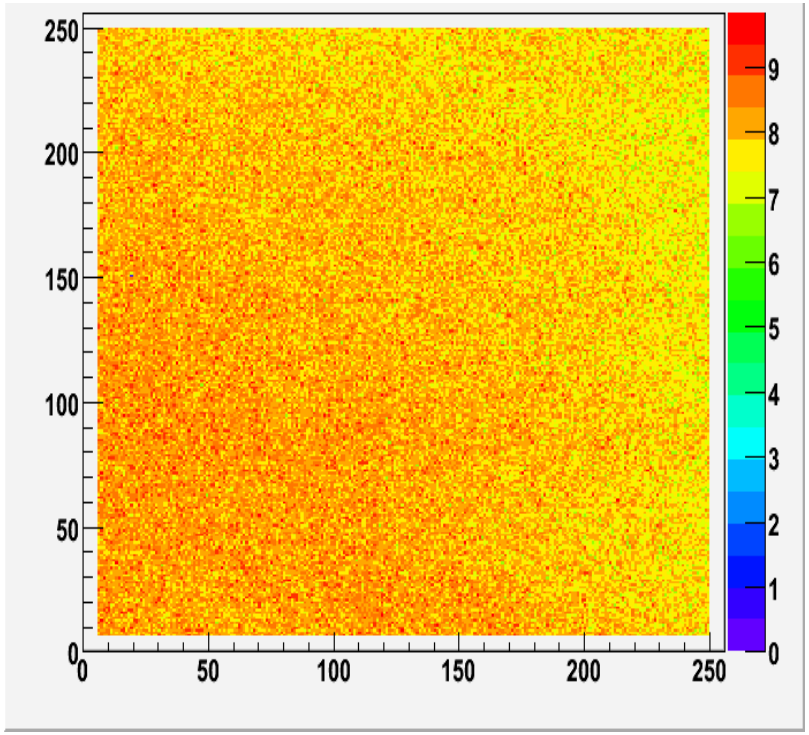




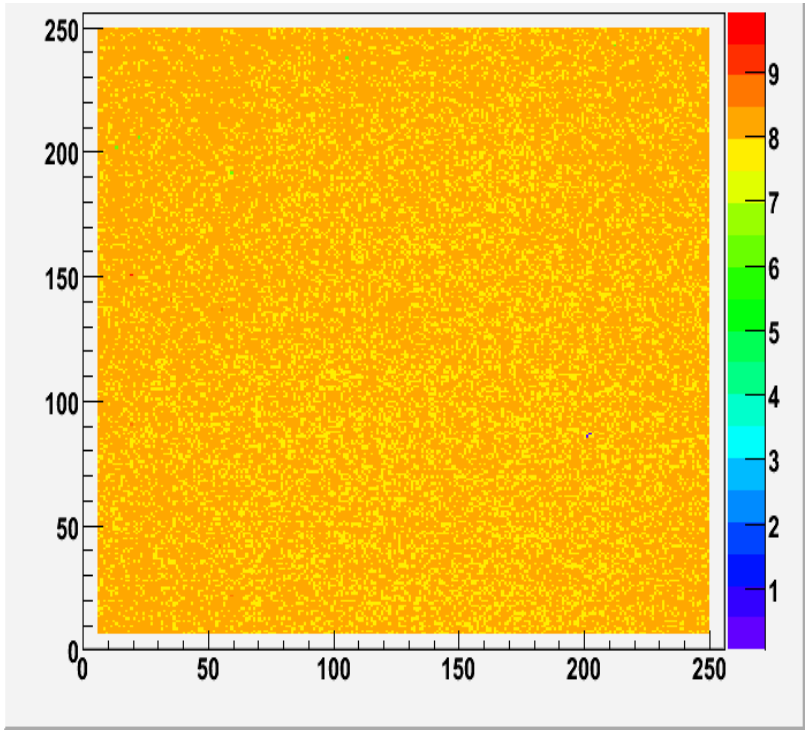


Before and After Trimming

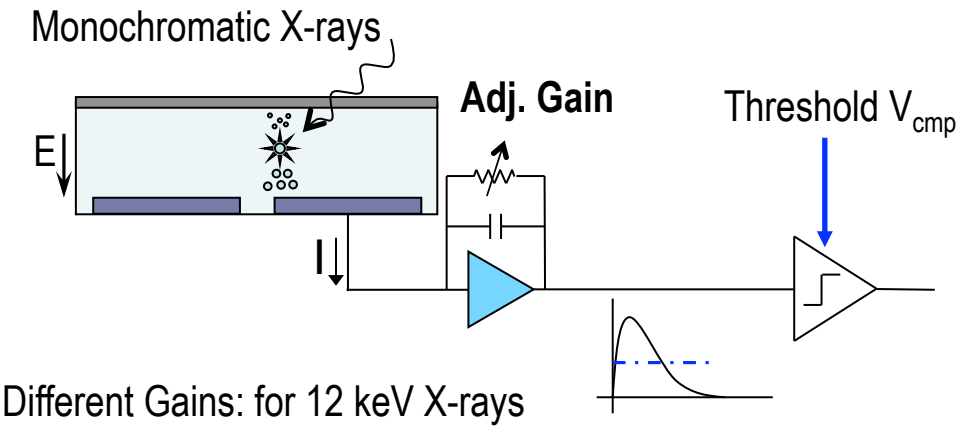
Before Trimming

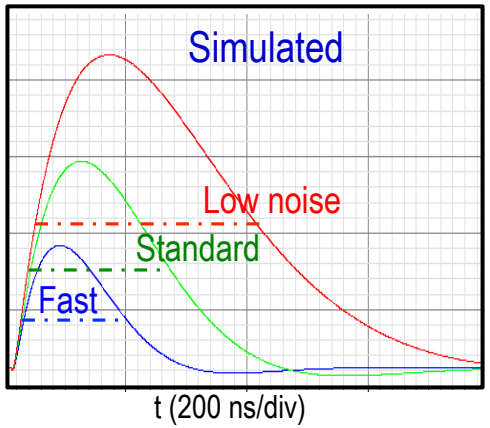


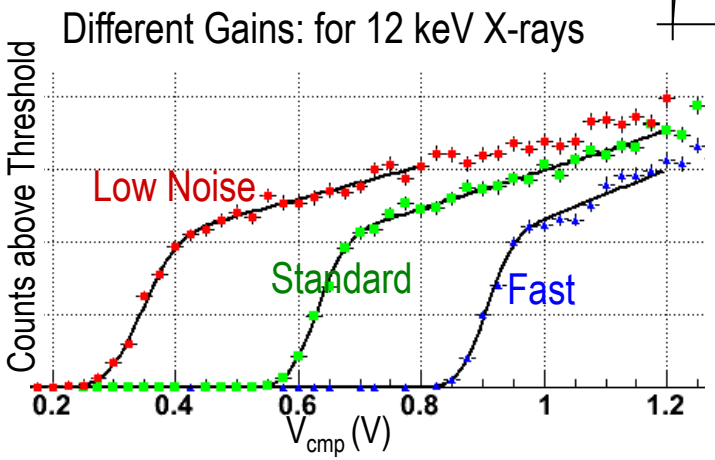
After Trimming

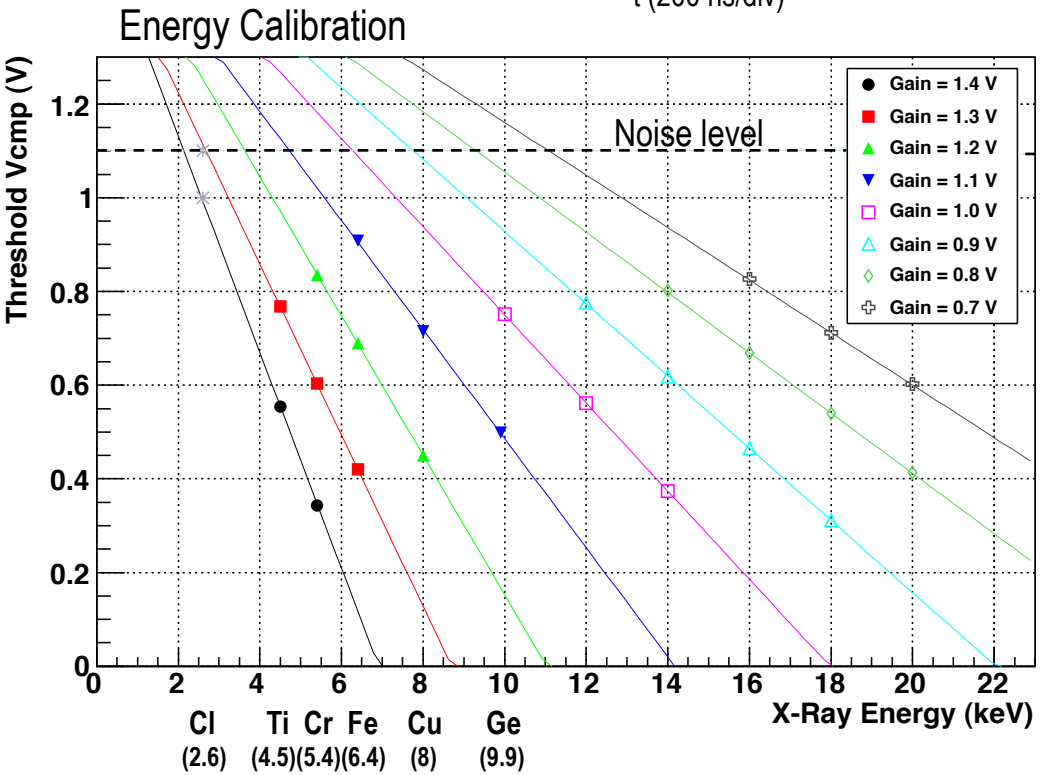


Adjustable Gain and Energy Calibration



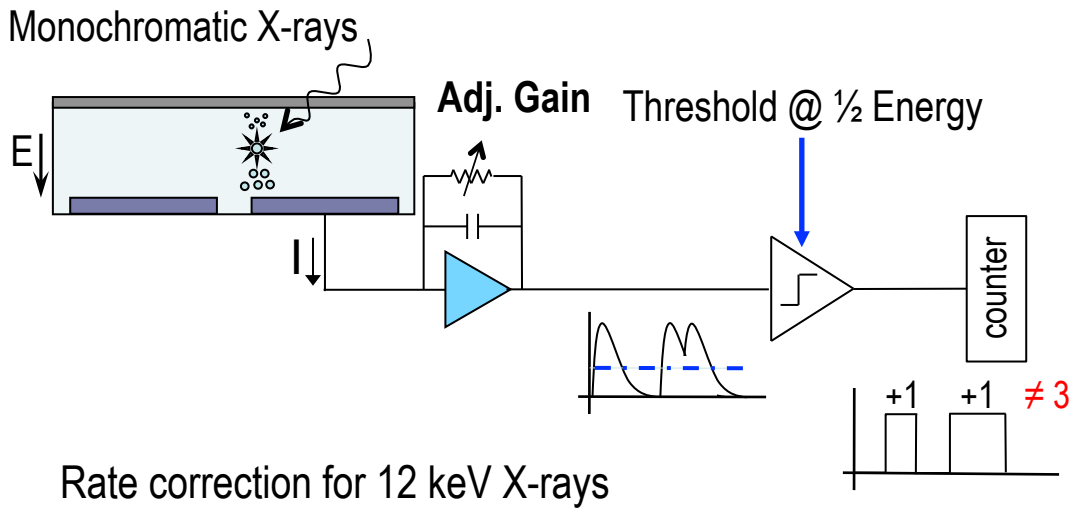


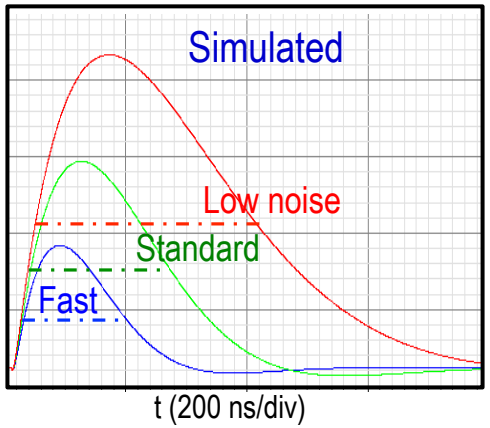


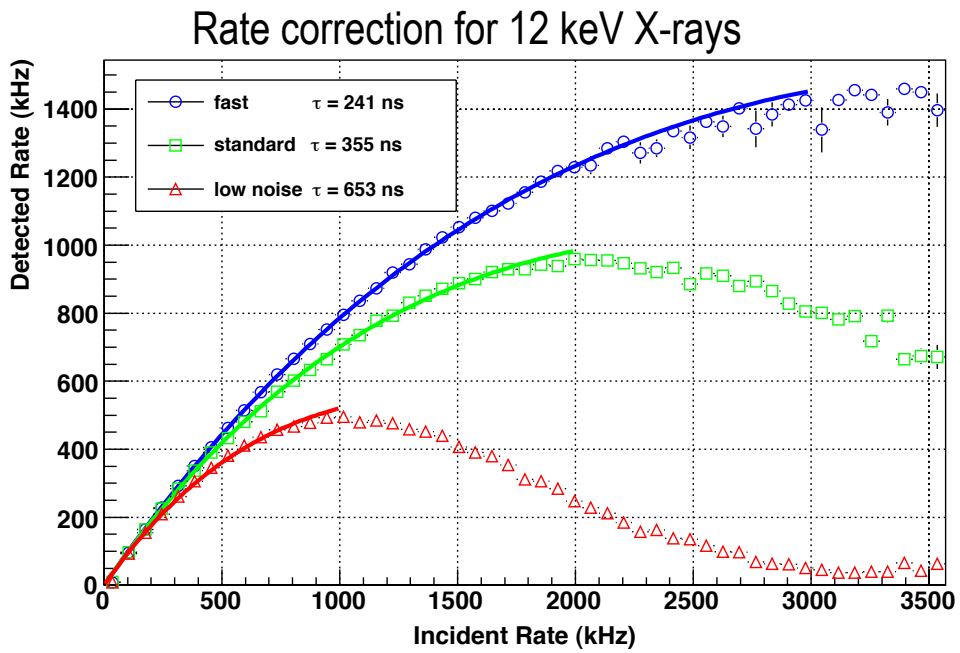


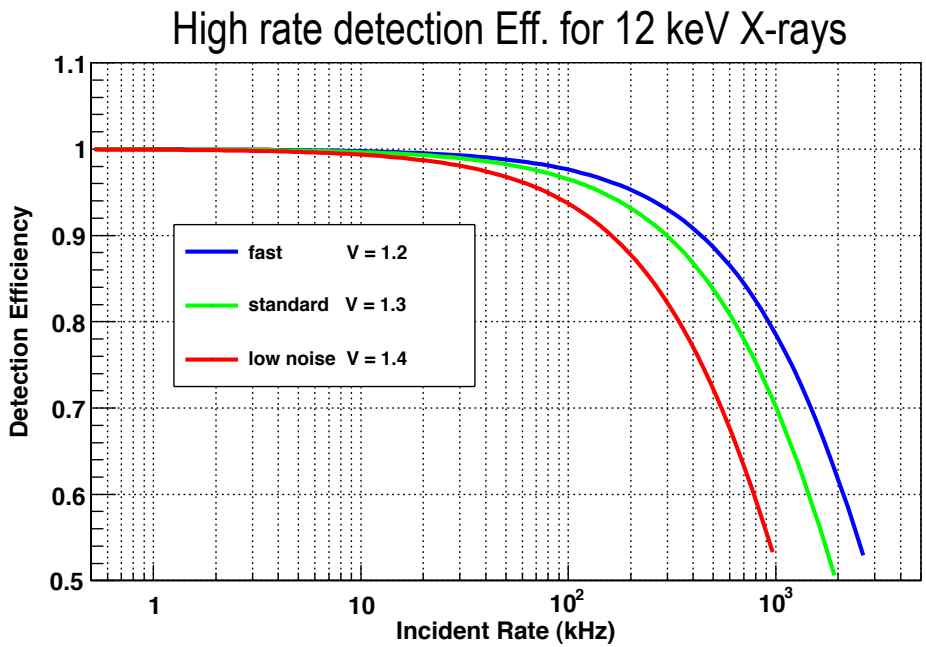
- Noise sigma: ~580 eV or 160 e^-
- Minimum threshold: ~2.5 keV

Rate Capability

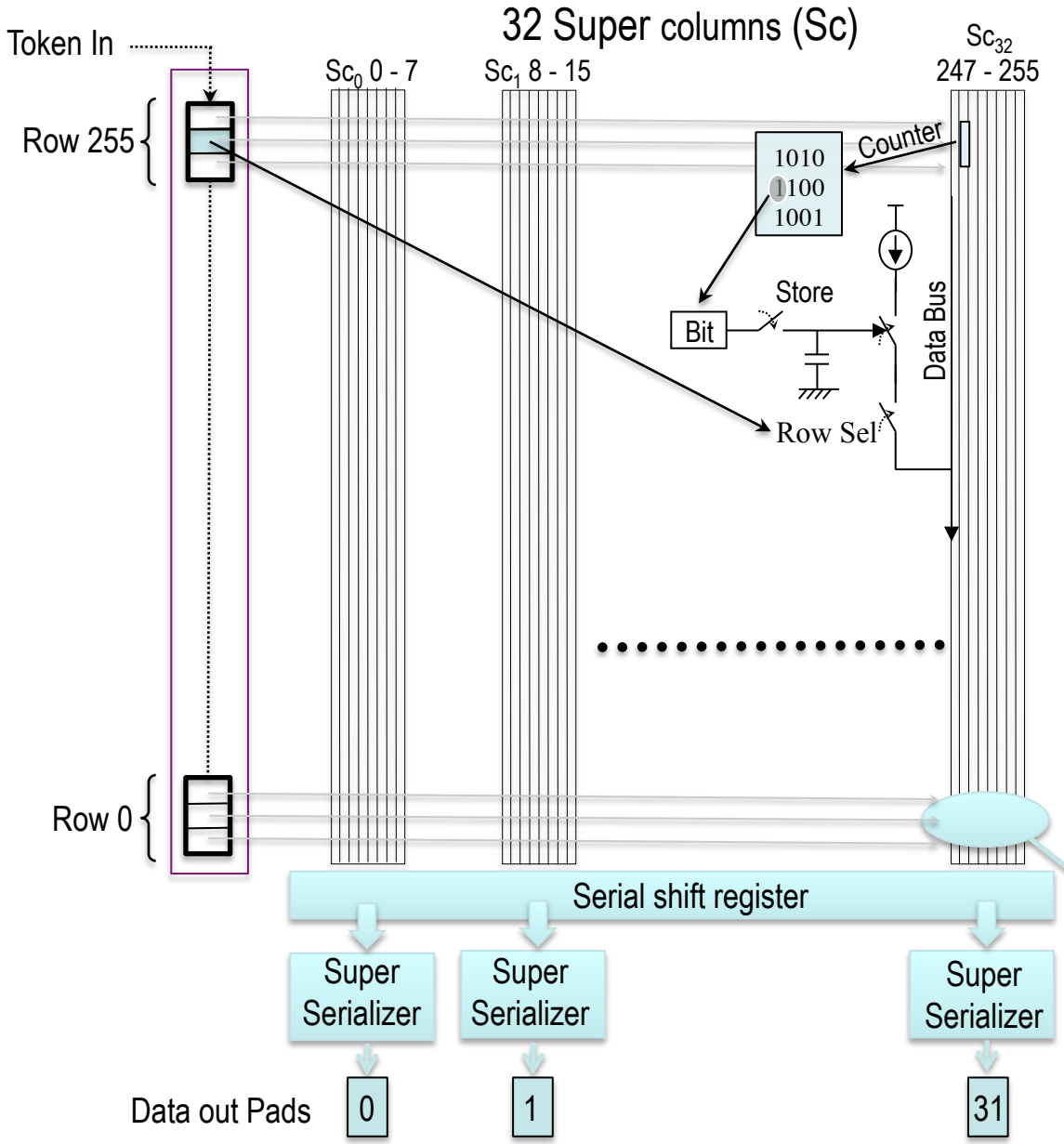




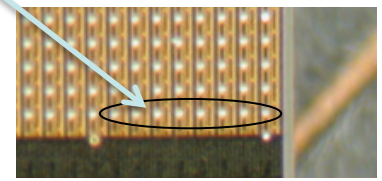




Digital data flow in the chip

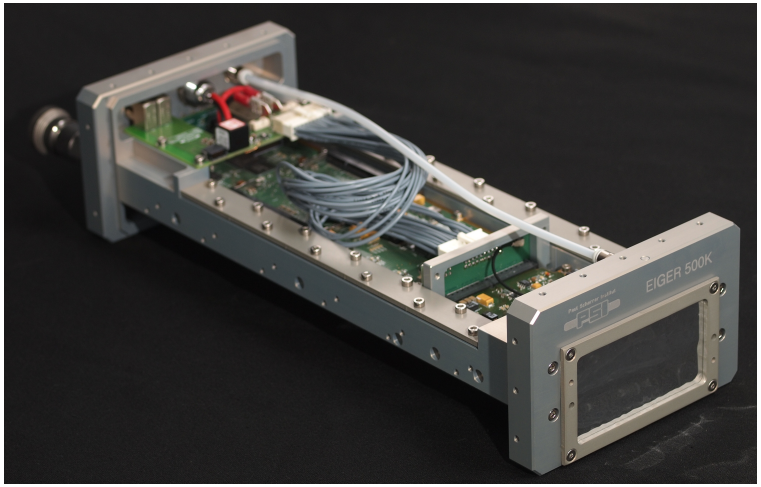


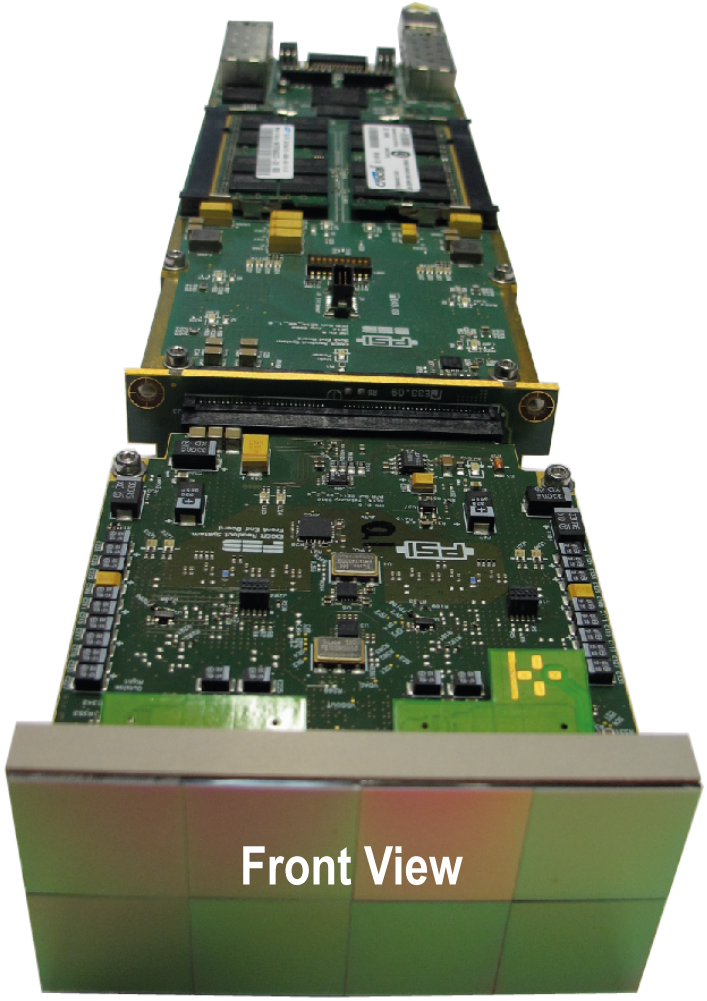
- Pixel array 256 x 256 (65 k pixels)
- Each counter bit has a local buffer
  - Short 3 µs Between frame dead-time
    3 µs -> store and reset the counter
- 32 Super columns
  - 32 bit bus
- Row select (Token shift register)
  - Address 4 bits of a pixel
  - 8 pixels per super column
- 32 Super serializers
  - Serialize the data sent to the pads
- 32 data out pads
  - 100 MHz DDR (6.4 Gbs/chip)

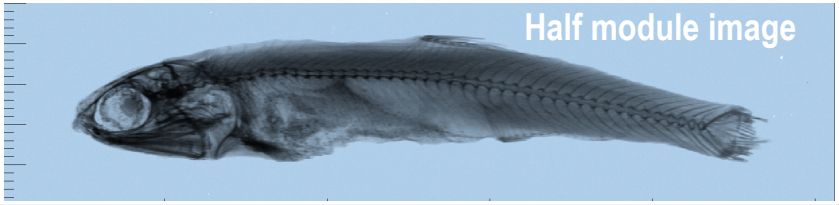


Multi-chip Modules

- Module sensitive area of 38 X 77 mm^2 (~ Pilatus size)
- 524k pixels per module
  - 2 x 4 chip array
- Parallel Half module based readout
- Maximum frame rates
  - 23 kHz in 4 bit mode
  - 12 kHz in 8 bit mode
  - 8 kHz in 12 bit mode
- Maximum data rates on the readout boards
  - 25 Gb/s for a half module
  - 50 Gb/s for a module
- On board in hardware data processing
- 8 GB of memory on a module
  - four - 2 GB RAMs per module
- Two 10 GbE data links per module

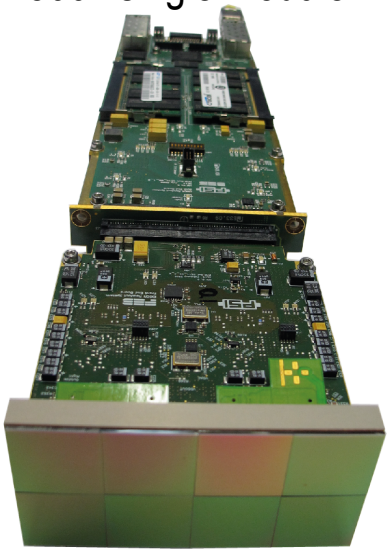


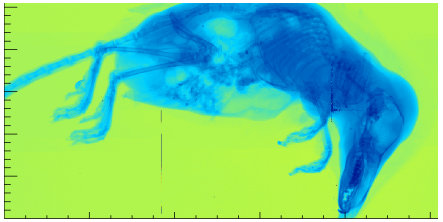




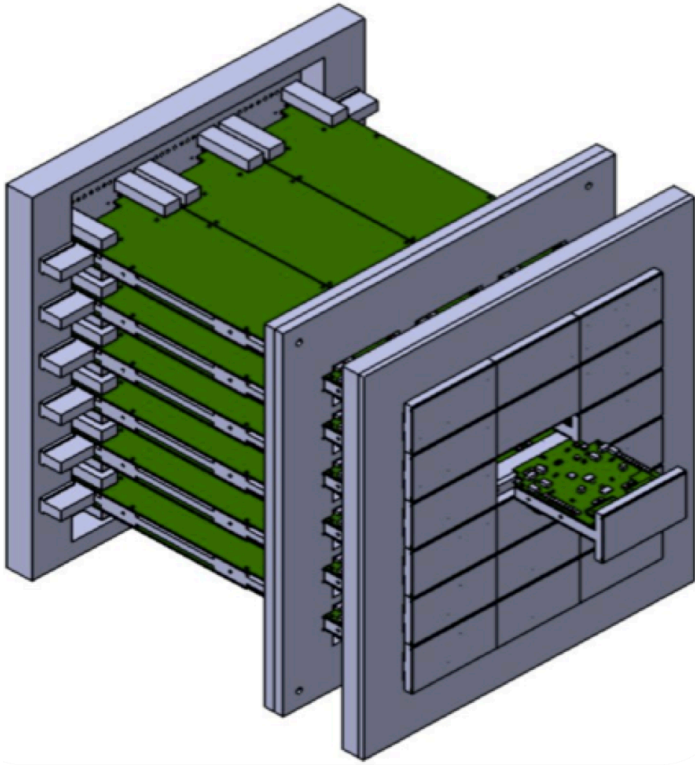
Eiger systems

500k single module





Multi-module detectors



	Number of pixels	On board storage (frames/4 bits)	Data rate[1] @ 12 kHz	Data rate[2] @ 1kH	Data rate[3] @ 100 Hz	Data rate[4] @ 10 Hz
Module	524 k (512 x 1024)	~32,740	50.3 Gb/s	6.29 Gb/s*	839 Mb/s*	168 Mb/s*
9M Detector	9.44 M (3072x3072)	~32,740	906 Gb/s	113 Gb/s	15.1 Gb/s*	3.02 Gb/s*

1) 8 bit, equivalent to ~4@23 kHz and 12@8 kHz. 2) 12 bit. 3) 16 bit. 4) 32 bit. *) Foreseeable continuous storage rates (~20 Gb/s).

On board Intelligence

Data buffering

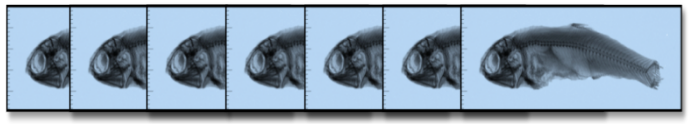
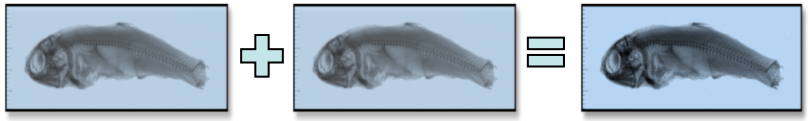
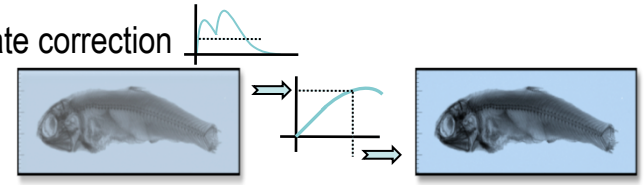


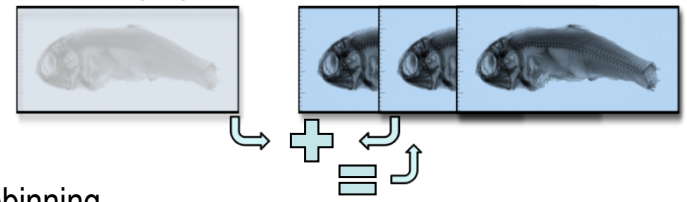
Image summation



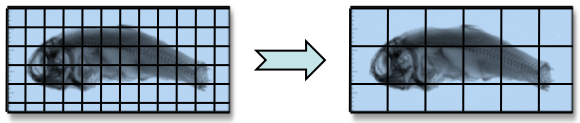
Rate correction



Series averaging



Rebinning



- On board (in firmware) data processing
  - real-time
  - parallel on multi-module systems
  - independent of the detector size
  - reduces a modules tens of Gb/s at the source
  - or a 9Ms, hundreds of Gb/s at the source
- Data buffering
  - on board memory for 32 k frames per 4 counter bits
- Image summation
  - extends the dynamic range from 4096 to 4×10^9
  - 2 ms sub frames (2 M counts/pixel/s)
  - makes long (minutes) high flux data taking possible
  - reduces the quantity of data at the source
  - transparent to the user
- Rate correction
  - performed on the sub-frames
  - more precise, less sensitive to rate fluctuation
  - real-time processing
- Pump and probe series averaging
  - high frame rate exposure series summing
  - alternating pumped and un-pumped
  - no data transfer dead time between series
  - huge reduction of the quantity of data at the source
- Data reduction
  - 2 x 2 pixel rebinning
  - SAXS ring intensity averaging (planned)
  - data compression (in thought, question of HDF5 compatibility)

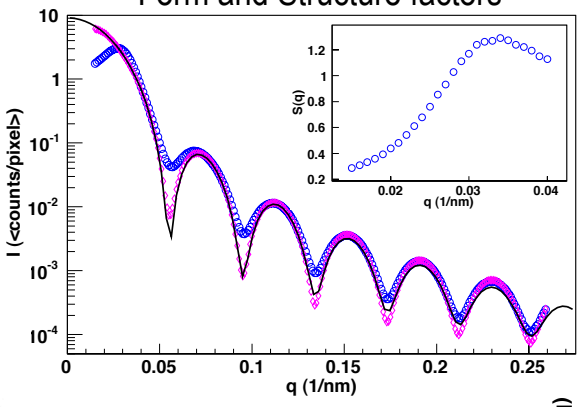
High frame rate experiment

Studied the dynamics of a colloidal suspension

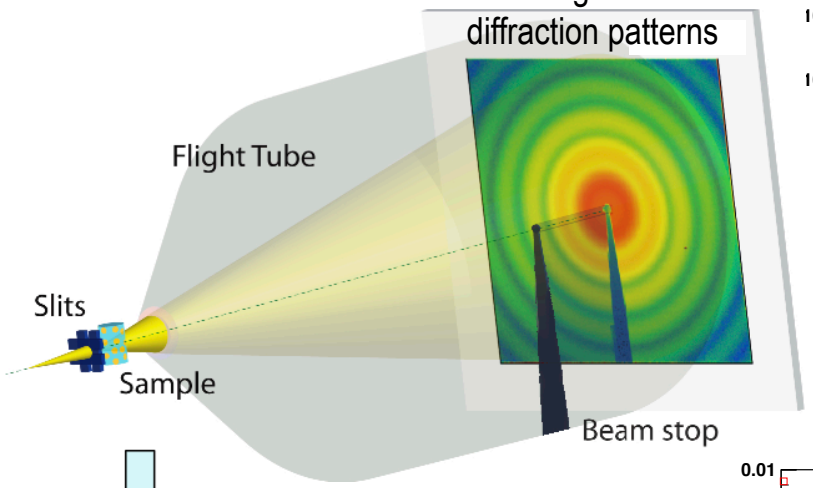
50,000 diffraction patterns in 2.5 seconds,
20 kHz, 45 µs exposure and 5 µs dead-time.

Eiger Single Chip Development system

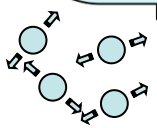
Form and Structure factors



Average of the diffraction patterns



Dynamic



Relative motion between the scatterers (82 nm radius silica colloids)

Intensity Autocorrelation function

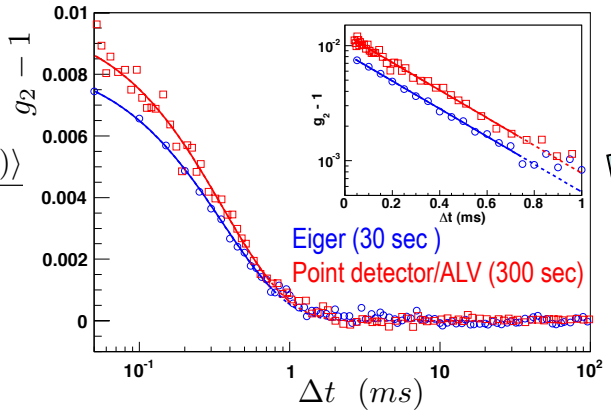
$$g_2(q,\Delta t) = \frac{\langle I(q,t)I(q,t+\Delta t)\rangle}{\langle I(q,t)\rangle^2}$$

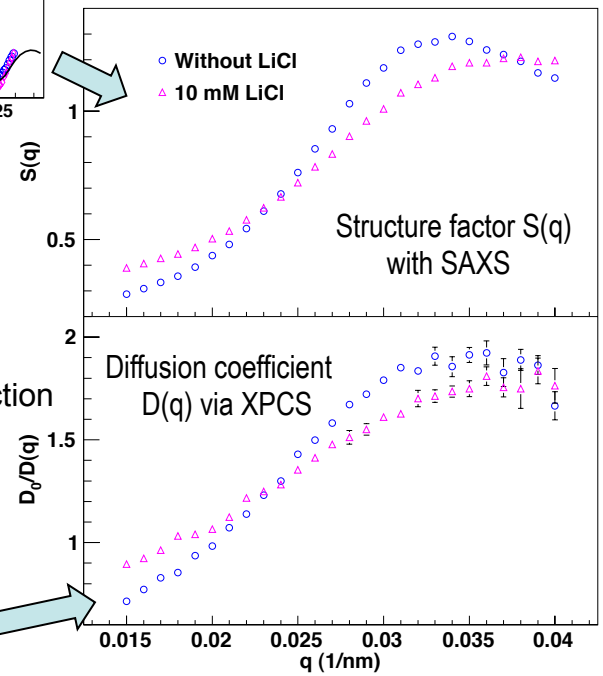
Siegert relation,

$$g_2(q,\Delta t) = 1 + \beta |g_1(q,\Delta t)|^2$$

Normalized field correlation function

$$g_1(q,\Delta t) = e^{Dq^2\Delta t}$$

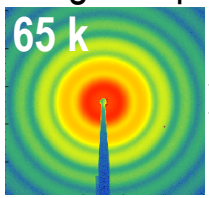




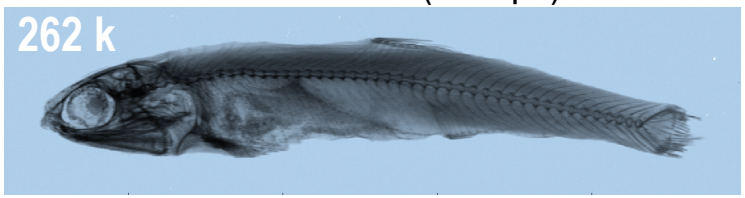
"Capturing dynamics with Eiger, a fast framing X-ray detector"
I. Johnson et al., Submitted to the JSR

Summary

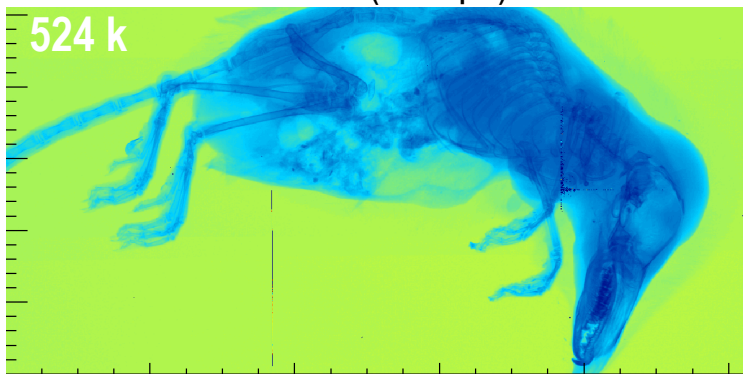
Single chip



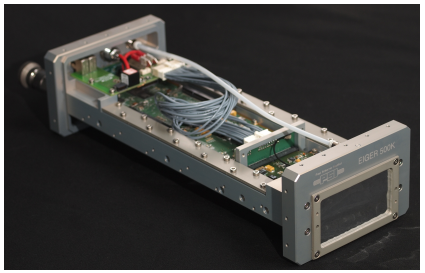
Half module (4 chips)

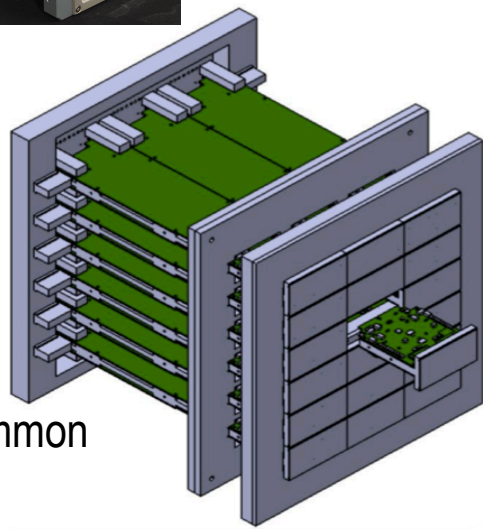


Module (8 chips)



- Results
  - Characterization of the chip
  - High frame rate demonstration experiment
- We are working towards 2 x 4 chip modules
- Single module systems @ the SLS
  - Coherent Small Angle X-ray Scattering Beamline (cSAXS)
  - Surface diffraction station (Material Science)
- High performance 9M Eiger @ cSAXS
  - 288 GB of on board memory or 2.5 sec @ highest data rates
  - >100 Hz continuous operation and data to disk
- The chip has been licensed to Dectris
  - many systems around the world
  - 16M Eiger for the Protein Crystallography Beamline (PX)
- Collaboration with the ESRF
  - Single module systems
- We (AIT, Dectris, SLS Detector group) working together to develop a common file structure (HDF5)





SLS Detector Group