Silicon-On-Insulator Photon-Imaging Array Sensor (SOPHIAS) for X-ray Free-Electron Laser Experiments

Takaki Hatsui
on Behalf of SOPHIAS collaboration
RIKEN SPring-8 Center
Collaborators

- **RIKEN, JASRI**
  All members of SACLA members, especially,
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- **Univ. of Hyogo**
  Takeo Watanabe, Tetsuo Harada, Hiroo Kinoshita

- **KEK**
  Yasuo Arai, and SOIPIX collaboration

- **Academia Sinica**
  - Minglee Chu, Chih Hsun Lin, Shih-chang Lee

- **Private Sector**
  - Yokogawa Digital Computing, sgi

- **Advisory Committee Members**
  - Peter Denes (LBNL), Yasuo Arai (KEK), Andrew Holland (The Open Univ.), and Grzegorz Deptuch (Fermilab)
(Hard) X-ray 2D Detectors for XFEL and SR

Observables
- Intensity
- Position or scattering angle
- Photon Energy (wavelength)
- Arrival Time
- …

Fast Signal Readout
- In-pixel processing
- Periphery or frontend IC processing
- Off-sensor module processing

3D photodiode by TSV
3D integration with micro bump

thick pn diode
Silicon

VLSI circuitry inside pixel

SOI Pixel Technology
Advantages Summarized by KEK

- Bonded wafer → Thick High Resistivity Sensor + CMOS
- Monolithic Detector → High Density, Low material
- Standard CMOS → Complex functions in a pixel
- No mechanical bump bonding → High yield, Low cost
- Small input capacitance → ~10fF, High conversion gain, Low noise
- Based on Industrial standard technology → Cost benefit and Scalability
- No Latch Up, Low SEE
- Low Power
- Operate in wide temperature (4-570K) range.

RIKEN joined SOIPIX collaboration from the end of 2007
2007 when RIKEN joined SOIPIX collaboration

- Back-gate effect

Handle wafer resistivity was low after CMOS process.

  - \( \sim 400 \text{ ohm/cm} \)

Small sensor chip size compared to other technology

  - 20 mm x 20 mm

Devices were for digital, not for analog circuitry.

X-ray Radiation hardness was not evaluated.
Back-gate effect

- Bias beneath of BOX layer acts as another gate
- Use for in-pixel circuit will increase the input capacitance

SOPHIS Implementation

- Peripheral circuit
  - BPW is used
- No BPW is used for in-pixel circuit
  - Design circuit taking back-gate effect into account by experiments
Critical Achievements in Process Technologies for XFEL applications
8 Inch FZ SOI wafer for full depletion of 500 um

<table>
<thead>
<tr>
<th>SOI wafer fabrication</th>
<th>Conventional Process</th>
<th>Improved Process</th>
<th>tool</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td><img src="image1" alt="Conventional Process" /></td>
<td><img src="image2" alt="Improved Process" /></td>
<td>KLA Tencor SP-1</td>
</tr>
</tbody>
</table>

| Pixel detector fabrication | | | X-ray Topography |
|----------------------------| | | |
Critical Achievements in Process Technologies for XFEL applications
Backside processing

Backside Processing
- CMP
- Wet etching
- Implant
- Laser annealing
- Al deposition

Device Simulation Results

Inverse current

- w/o Al
- with Al

Charge

Depth from back side (um)

0.3 um

V_{in}

X-ray Detectors for Synchrotron Applications

T. Hatsui, RIKEN
◆ Stitching Sequence

◆ Mask Layout

◆ Lithography Layout

Courtesy of Lapis Semiconductor

July 6, 2012

X-ray Detectors for Synchrotron Applications

T. Hatsui, RIKEN
**Stitching Process: Intermediate Observation**

- Stitching Layers: guard rings, M1
- Pixel Gap by Stitching is designed to match to the pixel size of 30 um
- Stitching error in X/Y directions < 0.025 um

Courtesy of Lapis Semiconductor
Device/Process Introduction Critical for SOPHAS

- Buried Well
- MIM Cap. onto 3M
- PCell for temp. sensor/circuitry
- Diode

Introduction of I/O Tr for Vdd=2.5 V Operation

*3D view is created by google sketchup 6

Courtesy of A-R-Tec
1/f Noise Suppression

- Fully Depleted SOI Transistor (FD-SOI Tr):  
  - Body Floating Tr  
    - Large 1/f noise due to body floating  
  - Source Tie/Body Tie Tr Pcell has been introduced.  
  - 1/f noise simulation environment has been successfully introduced.

[Diagram showing different transistor configurations: Body Floating, Source Tie (Type 1), Source Tie (Type 2), Body Tie.]

Courtesy of A-R-Tec
1/f Noise: Simulation and Measurement by Test Chip

SOPHIAS

Test Chip MIVAPIX2

DN^2/Hz

10^4

10^3

10^2

0.001

0.01

0.1

Hz

64.8mm

30mm

7.5mm

15.4mm
2007 when RIKEN joined SOIPIX collaboration

Current Status
- Buried P-well proposed by KEK, and now extensively used.
- New Developments
  - Nested well proposed by Fermilab
  - Double SOI proposed by KEK
- FZ with > 3 kohm/cm
- Stitching
  - 66 mm x 30 mm achieved
  - 130 mm x 130 mm is possible
- 4M to 5M, MIM Cap onto 3M
- 1/f noise suppression by Source-tie and body-tie Tr.
- Simulation environment improvement.
- Currently upto 150 krad for Tr. → SOPHIAS is for < 7 keV with back-illumination
- Systematic study of the radiation damage has been started
  - new process,
  - prediction by radiation damaged device models

Back-gate effect
Handle wafer resistivity was low after CMOS process.
- ~400 ohm/cm

Small sensor chip size compared to other technology
- 20 mm x 20 mm

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SOPHIAS Pixel Layout by Multi-Via Concept

High gain

Low gain

Low Gain Via : 4

High Gain Via : 24

30 µm pixel

X-ray

SiO₂

Sensor

p⁺

Via

X-ray Detectors for Synchrotron Applications

T. Hatsui, RIKEN
SOPHIAS
In-pixel Schematics

Gain | Csens [fF] | Via # | Gain [uV/e]
--- | --- | --- | ---
High | 16 | 24 | 7.2
Low | 240 | 4 | 0.15
SOIPHIAS Sensor

All the Periphery Circuit \textit{incl. row registers}

- 30 mm
- 64 mm

- 3-side buttable
- 4-side buttable with steped geometry

Guard Ring
26.7 mm

64 mm

25 msec Exposure Ag 20 keV 0.2 mA
X-ray Image

2 mm
1st Submission of Full Sensor Chip
Cosmetic Quality Evaluation by Optical Light

He-Ne Laser Spot

719 x 3 = 2157 pixel (64.77 mm)

File name explanation: X-Y.bmp
- X: Shot No.
- Y: Left or Right

インピーダンスの整合をとった。
縦筋が目立たないように画像取得した。

July 6, 2012
1st Submission of Full Sensor Chip Offset Variation

Data taken by Test Camera
- Dead pixel: 0
- Readout port: 6
- Readout Speed: 25 MHz/pixel equivalent to
  60 frame/sec with off-chip Digital CDS
  120 frame/sec without off-chip digital CDS

Dead Pixel: None
Defect Pixel defined as offset > 200 meV
  ratio 2.7 x 10^-5
  53 pixels /1.9 Mpixel
1st Submission of Full Sensor Chip Gain Responsively

- Design guideline of SOPHIAS pixel
  - Calibration easy pixel
    - Identical behavior against pulse and cont. X-ray sources
  - linearity of raw signal is not mandatory

Qualitatively consistent with physical model
Calibration algorithm is now under progress
Data Processing and Detector Release

**Vacuum**

- **Dual-Sensor Detector**
  - Released to user operation in 2014
  - 30 frame/sec
  - 4 Mpixel

- **Multi-Sensor Detector**
  - Release target TBD
  - 60 frame/sec
  - max 80 Mpixel
  - with E/O, calibration FPGA, and CLHS

**Diagram:**
- Drive clocks
- 25 MSPS x 12
- 400 Mbps x 12
- 3 Gbps
- Command trigger
- CL HS
- Sensor
- ADC
- Driver
- FPGA
- O/E
- Digital CDS Calibration FPGA

**July 6, 2012**

X-ray Detectors for Synchrotron Applications
# Current Status of SACLA Multiport CCDs

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pixel</td>
<td>50 μm□</td>
</tr>
<tr>
<td>Peak signal</td>
<td>&gt;4.4 Me-</td>
</tr>
<tr>
<td></td>
<td>2700 ph.@ 6 keV</td>
</tr>
<tr>
<td>Noise</td>
<td>&lt; 300 e-rms</td>
</tr>
<tr>
<td></td>
<td>0.18 ph.@ 6 keV</td>
</tr>
<tr>
<td></td>
<td>typ. 130-240 e-rms</td>
</tr>
<tr>
<td>Pixel Number</td>
<td>1k x 512 pixels/sensor</td>
</tr>
<tr>
<td>Array</td>
<td>Currently max 8 sensor array with 4 Mpixels</td>
</tr>
<tr>
<td>Rad. Hardness</td>
<td>&gt;1.6 x10^{14} photons/mm^2@ 12 keV</td>
</tr>
<tr>
<td>Dead Area at Edges</td>
<td>&lt; 300 μm</td>
</tr>
<tr>
<td>Sensitive Layer</td>
<td>50 μm</td>
</tr>
<tr>
<td></td>
<td>to be upgraded to 300 μm in Phase III</td>
</tr>
</tbody>
</table>

- **2k x 2k pixels**

**User Operation**

- 2012A proposal
- 25 proposal selected
- More than half will use MPCCD detector
User Experiment Example
Coherent X-ray Imaging

1 um focused beam

sample  Octal  Single

Coutesy of Prof. Takahashi (Osaka Univ.) Dr. Yamamoto (RIKEN), and Prof. Nakasako (Keio Univ)
Future Applications

- SPring-8 II
  - Coherent flux of source
    - $\times 1000$ in 10 keV region
    - More flux increase at sample position
  - A Target Candidate
    - X-ray Photon Correlation Spectroscopy (XPCS) in nanosecond regime
  - Provisional Demands for Detectors
    - Data frame acquisition at 23.6 nsec interval, (or 1.966 nsec interval at best)

- Medical Applications
  - In collab. with Lapis Semiconductor and Rohm group.
SOI Pixel Detector
Monolithic Si Pixel Sensor with VLSI
Collaboration of KEK, and Lapis Semiconductor, and other institutions

Advantages Summarized by KEK

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Control of charge collection
SOPHIAS

Sample Hold Electronics
With 20 ENC at close to GHz rate

Charge transimpedance amplifier is not needed. Speed and noise is not in trade-off relationship in conventional way.
Noise Performance Demonstration
SOI pixel sensor for future X-ray astronomical satellites

XRPIX

4T type Pixel, -50°C, Single Pixel CDS Readout

~20 ENC is achieved with simple 4T like pixel without CTIA

 Courtesy of Kyoto Univ.

Ryu et al. IEEE TNS Submitted (2012)
Assumed Parameter:
120 \text{um} \square \text{ pixel}, 10 \text{ bit ADC}, \text{Analog: noise 50 e- Peak 100 ke-}

Global Timing Track from upper and lower pads
→ timing delay < 1 \text{nsec}
Design optimization should be carried out.

Technology for 1 \text{nsec framing} will be in our hand.
Readout remain in 10-100 kframe/sec.
Exposure/readout ratio is low.
• Optimized operation,
• In-pixel processing
  • Custom sensor for each application
• Off-pixel processing
  • Integrate new technology, such as 3D integration
SOI Pixel Technology

- Ramping up to real scientific applications.

SOPHIAS

- Peak Signal 7 Me-, Noise 100 e-, Dual gain pixel, 30 um□ pixel, 1.9 M pixel/chip

SOPHIAS status

- Just after 1st run, Testing is underway
- Major tasks
  - Pixel-by-pixel Calibration

Release

- 2014 for Dual-Sensor Detector
- Multi-Sensor Detector is envisaged. Release date is under discussion.

After SOPHIAS

- Low input capacitance
  - Fast shutter in the nanosecond regime