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AGIPD, the Adaptive Gain Integrating Pixel Detector: A 4.5 MHz camera for the European XFEL

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The European X-Ray Free Electron Laser (XFEL) [1,2] will provide ultra short, highly coherent X-ray pulses which will revolutionize scientific experiments in a variety of disciplines spanning physics, chemistry, materials science, and biology.

One of the differences between the European XFEL and other free electron laser sources is the high pulse repetition frequency of 4.5 MHz. The European XFEL will provide pulse trains, consisting of up to 2700 pulses separated by 220 ns (600 μ s in total) followed by an idle time of 99.4 ms, resulting in a supercycle of 10 Hz.

Dedicated fast 2D detectors are being developed, one of which is the Adaptive Gain Integrating Pixel Detector (AGIPD) [3-5]. This development is a collaboration between DESY, the University of Hamburg, the University of Bonn (all in Germany) and the Paul Scherrer Institute (PSI) in Switzerland.

AGIPD is based on the hybrid pixel technology. The current design goals of the newly developed radiation hard Application Specific Integrated Circuit (ASIC) with dynamic gain switching amplifier in each pixel are (for each pixel) a dynamic range of more than 104 12.4 keV photons in the lowest gain, single photon sensitivity in the highest gain, an analog memory capable of storing 352 images, and operation at 4.5 MHz speed. A vetoing scheme allows to maximize the number of useful images that are acquired by providing the possibility to overwrite any previously recorded image during the pulse train.

It is necessary to store the acquired images inside the pixel logic during the pulse train and a compromise had to be found between storing many images, requiring a large pixel area, and high spatial resolution, requiring small pixels sizes. The AGIPD will feature a pixel size of (200 μ m)² and a silicon sensor with a thickness of 500 μ m. The image data is read out and digitized between pulse trains.

A project overview and a performance estimate will be presented as well as results from the current test chips demonstrating the capabilities of the final system.

References

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