PAUL SCHERRER INSTITUT

PSI

Babak Kalantari :: Section Electronics :: AEK/GFA :: Paul Scherrer Institute :: GFA-PSD Seminar

CompactPCI-Serial (CPCI-S) Hardware Toolbox Status & Roadmap

27.02.2023

Purpose and idea of Hardware Toolbox

- Provide **supported** set of electronics to realize systems for applications

- General idea is to consult or get support of AEK experts, who know the tools best, to propose how the system should be realized!

Our Goal:

- Building **maintainable** (hardware, firmware, software) systems by supported tools!
- Maintainable systems mean maintainable machines -> **reliable** operation!

***Supported** Tool -> **maintainable** system -> **reliable** operation*

Purpose and idea of Hardware Toolbox

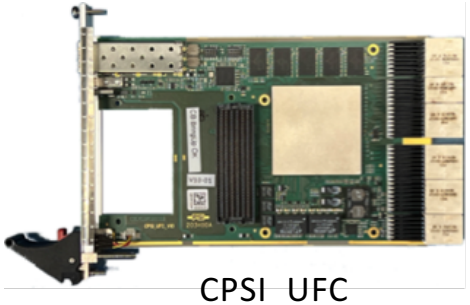
- Check tools' availability (portfolio)
  - https://intranet.psi.ch/en/aek/hardware-toolbox
- Get AEK support
  - https://intranet.psi.ch/en/aek/aek-support-requests

in collaboration with AEK

System
(application)

CPCI-S electronics (Toolbox)

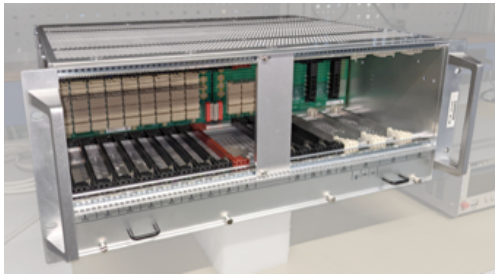
✓ ***Critical* components** have been developed and successfully tested!



CPSI_UFC

CPSI_RTM_DAC

CPSI_CIO

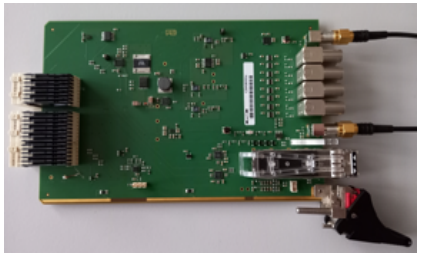


CPCI-S Crate

CPCI-S tool	Functionality	SLS2.0 application	General application	Design / Prototyping	Series Delivery *estimate!*
CPSI_UFC	FMC+ carrier & DSP (parallel and serial I/O)	**LLRF, e-Instrumentation**	High performance, real-time Control & DAQ	**No functionality risk!**	**Q2/2023**
RTM_DAC	Rear Transition Module with 500 MHz DAC & digital I/O	**LLRF**	Low latency, real-time control / feedbacks	**No functionality risk!**	**Q2/2023**
CPSI_CIO	Serial I/O & DSP	**Timing**	Data stream real-time processing, feedbacks	**No functionality risk!**	**Q3/2023**
CPCI-S Crate	Modular bus-system & housing (10 Gbps backplane, redundant PSU)	**Various systems in machine & beamlines**	High performance, real-time Control & DAQ	**No functionality risk!**	**Q2/2023**

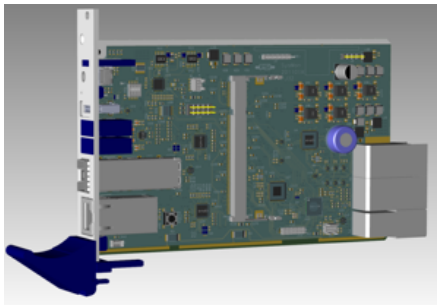
CPCI-S electronics (Toolbox)

➢ ***less-critical* electronics** under design, development or testing

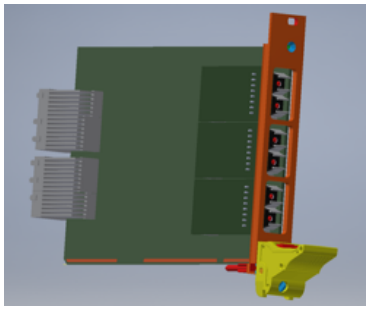


CPSI_RTM_FIO

CPSI_ASC



CPSI_MON



CPSI_RTM_MIO

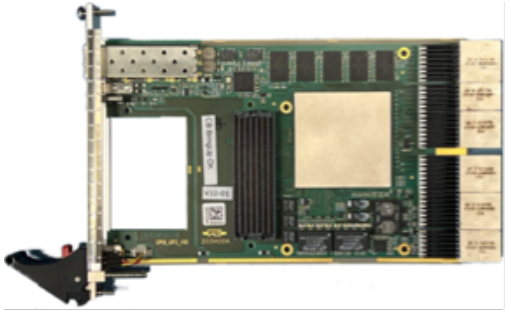
CPCI-S tool	Functionality	SLS2.0 application	Design status	Series Delivery estimate
CPSI_RTM_FIO	Transition board with Fixed I/O	**Timing EVM/EVR/Fanout**	prototype tested, in procurement	**Q3/2023**
CPSI_ASC	Analog Signal Conditioning	**e-Instrumentation PCT/ICT/LLM/FPM**	Specification	**Q4/2023-Q1/2024**
CPSI_MON	System monitoring	**Remote Monitoring/control of CPCI-S systems**	Started	**Q4/2023-Q1/2024**
CPSI_RTM_MIO	Transition board with Modular I/O	**Timing EVR**	Started	**Q4/2023-Q1/2024**

Toolbox Workhorses

Two powerful, complementing platforms for building control/DAQ systems

CPSI_CIO https://i.psi.ch/G9Dcf

- Serial data processing & communication I/O
- Gigabit interconnect via front & backplane
- Cost optimized, uses commercial SoM



CPSI_UFC https://i.psi.ch/0O614

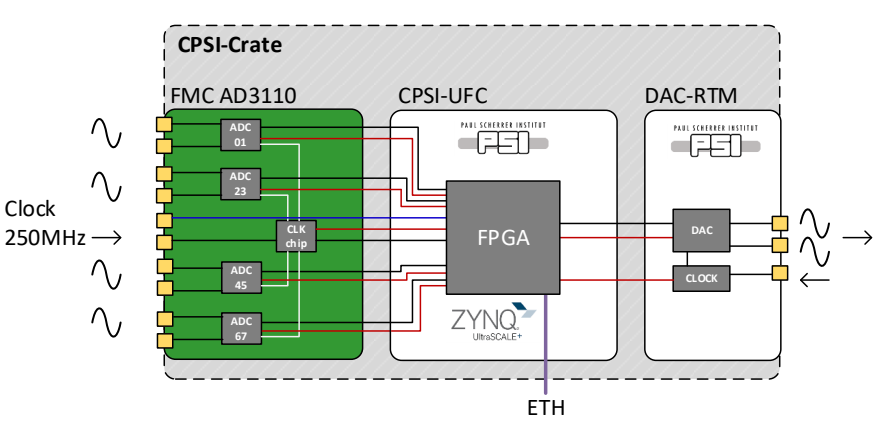
- integrates commercial I/O modules, FMC+/FMC
- Gigabit interconnect via backplane, front and rear
- Very high performance on-board MPSoC

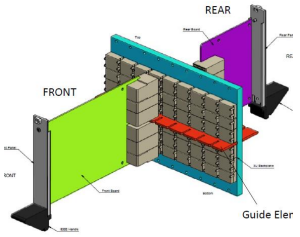
Commons

- Zynq UltraScale+ arch with AEK supported FW/SW & EPICS/Linux infrastructure
- Enable complete, standalone processing and DSP system
- Sharing key components (clocking, uC) allowed parallel prototype validation/debugging
- Same Pinout definition (OpenCPSI) allows sharing RTM's between boards

SLS2.0 LLRF using CPSI_UFC

- SLS2.0 LLRF: accelerator RF phase & amplitude stabilization
  - Low latency feedback loops
  - IN/OUT propagation 112 ns
  - ADC: 16-bits @250 MHz (FMC)
  - DAC: 16-bits @500 MHz (RTM)

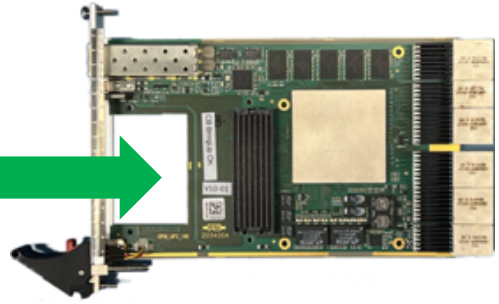




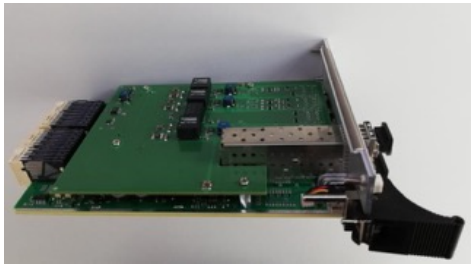
✓ Phase (limited BW): 4x better than requirement
✓ Amplitude (limited BW): 8x better than requirement

Performance charachterization in the lab:
https://indico.psi.ch/event/12911/contributions/38354/

250 MHz ADC
(FMC module)



CPSI_UFC

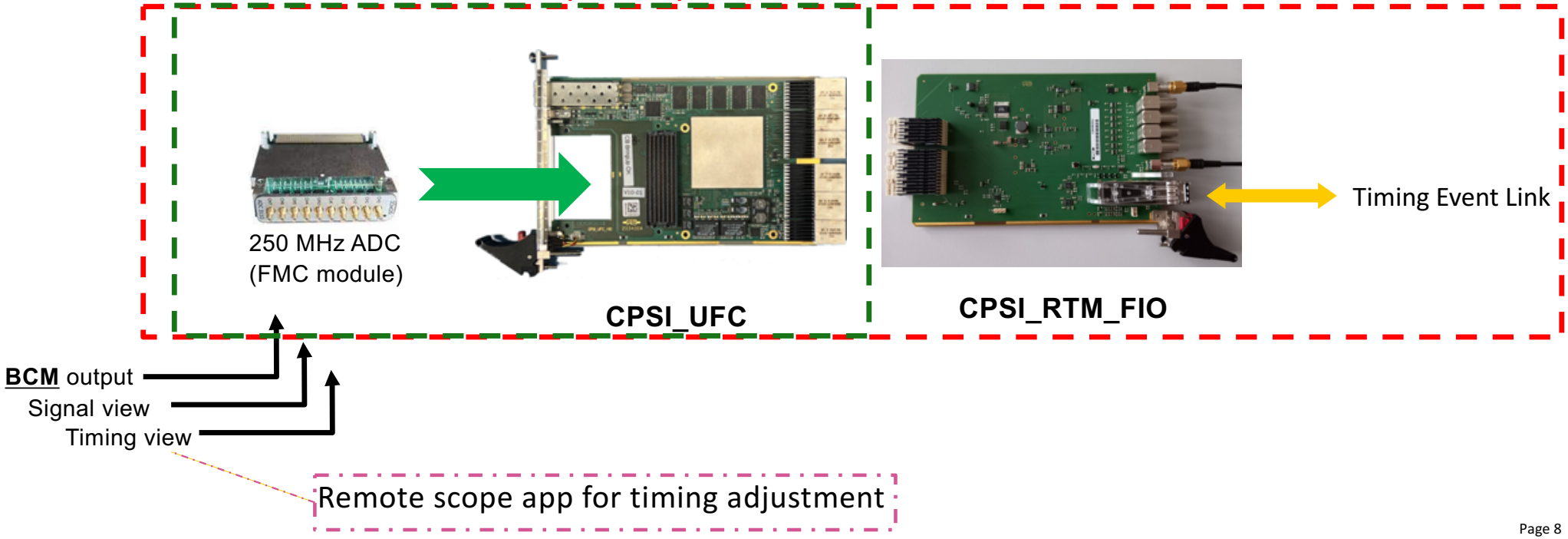


CPSI_RTM_DAC
(500 MHz DAC and interlock)

SLS2.0 e-Instrumentation
LLM/BCM/(N)PCT

- Reusing same building block as in LLRF
  - Signal acquisition and remote scope (signal view) by **CPSI_UFC**, **FMC ADC**
  - Timing interface and digital I/O (interlock, etc.) by **CPSI_RTM_FIO**

This block will be reused for LLM/NPCT/BCM



Fast Digitizers & Analog I/O

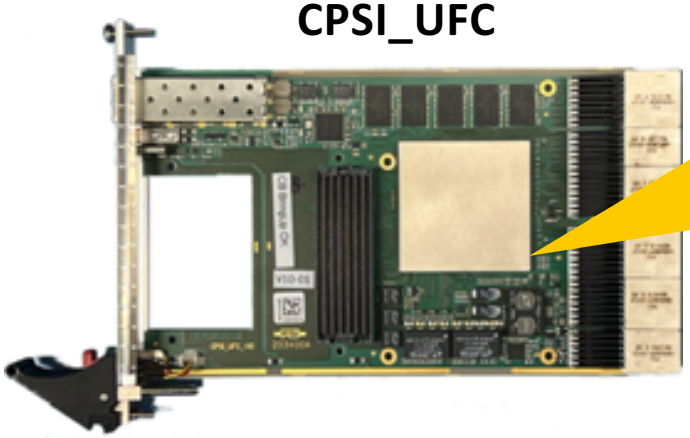
- Applications
  - Fast digitizer, high-end DAQ with custom signal processing
  - Fast, real-time feedback loops (sensor-actuator)
- **FMC217**: 2xADC 12-bit @ 6.4 GSPS, 1xDAC 16-bit @ 12 GSPS, BW 6 GHz (just joining portfolio)
- **FMC231**: 4xADC 16-bit @ 1.0 GSPS, 4xDAC 16-bit @ 2.8 GSPS (**support Q3/2023** -> student work)
- **ADC3110**: 8xADC 16-bit @ 250 MSPS (supported)

FMC217 Vadatech

ADC3110 IOxOS

FMC231 Vadatech

CPSI_UFC



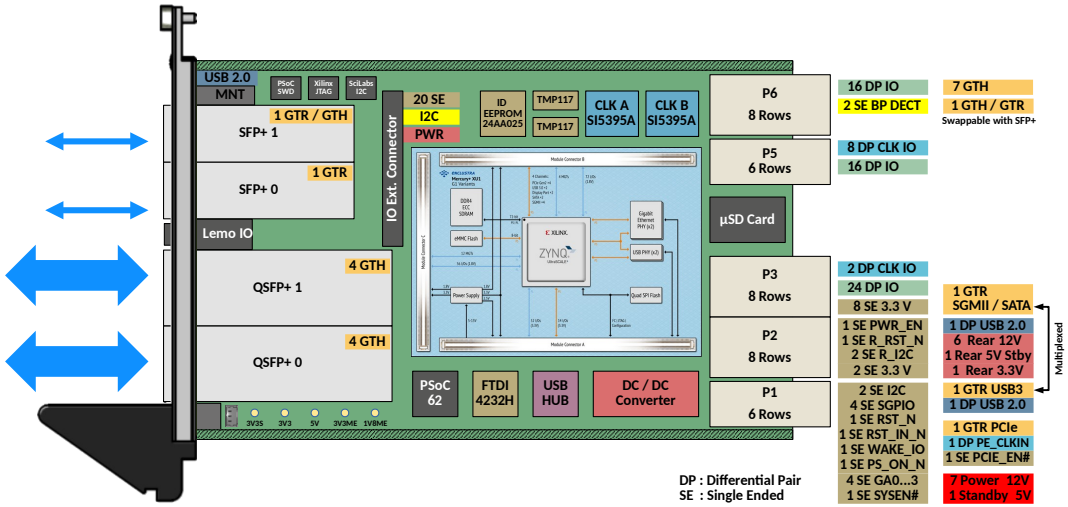
*FMC carrier provides common platform that allows sharing **FW/SW infrastructure** which significantly reduces required effort and time to deliver!*

CPSI_CIO applications

- Data stream processing & communication
- Global feedbacks
- Generic I/O with appropriate RTM
- Data concentration

CPSI_CIO

10x optical links (10 Gbps)



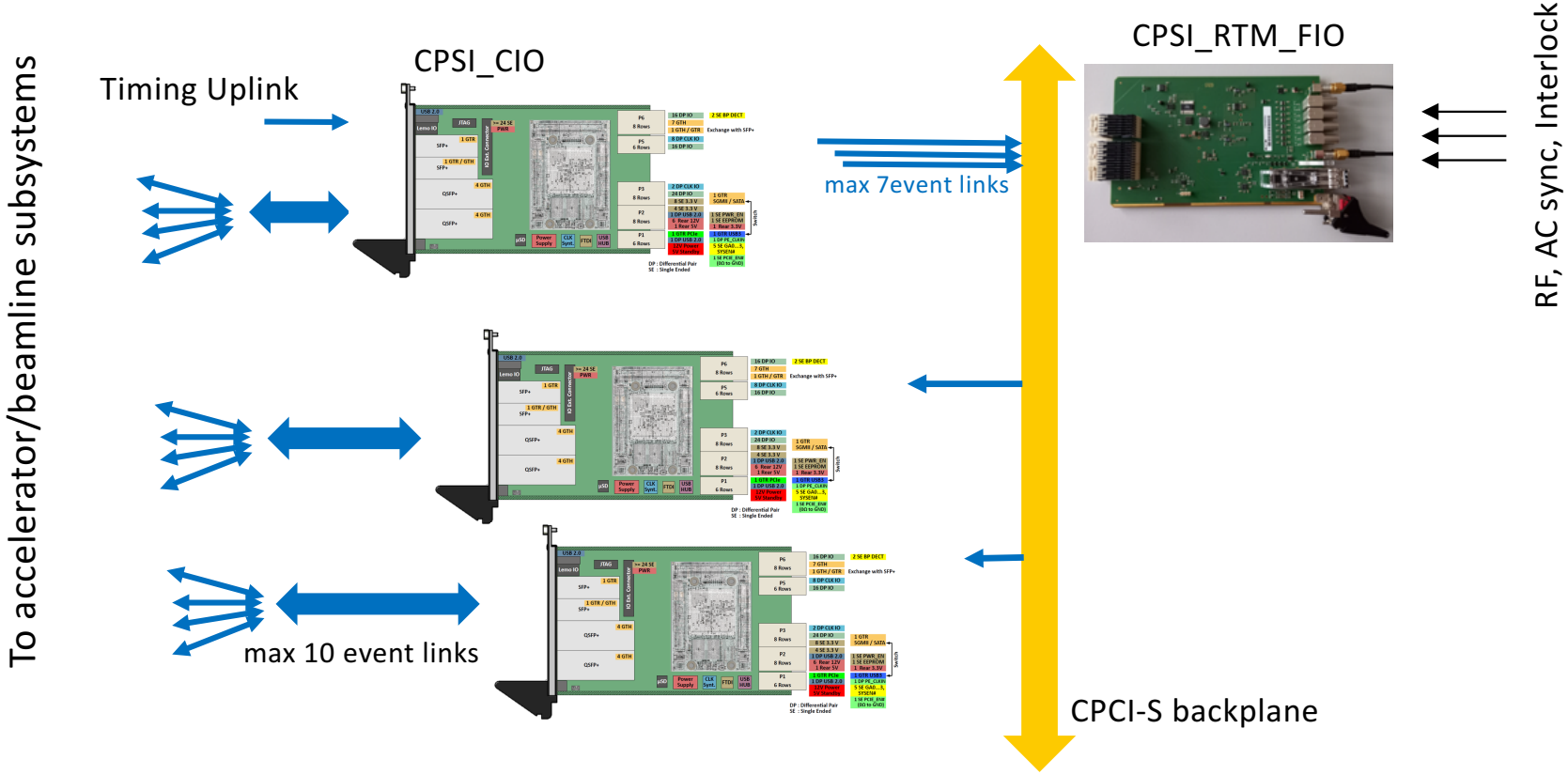
Full-Mesh backplane interconnect (incl. 10 Gbps links)

Rear I/O (via RTM)

System CPU interconnect (PCIe, USB, SATA)

SLS2.0 Timing System using CPSI_CIO

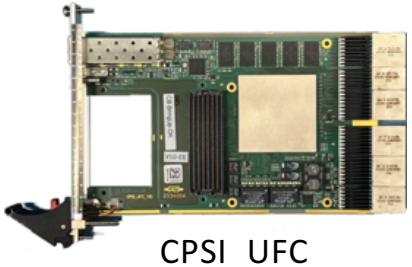
Event Master, Distribution, Receiver



Example: timing master/distribution system within one CPCI-S crate.
Timing network comprises multiples of demonstrated system.

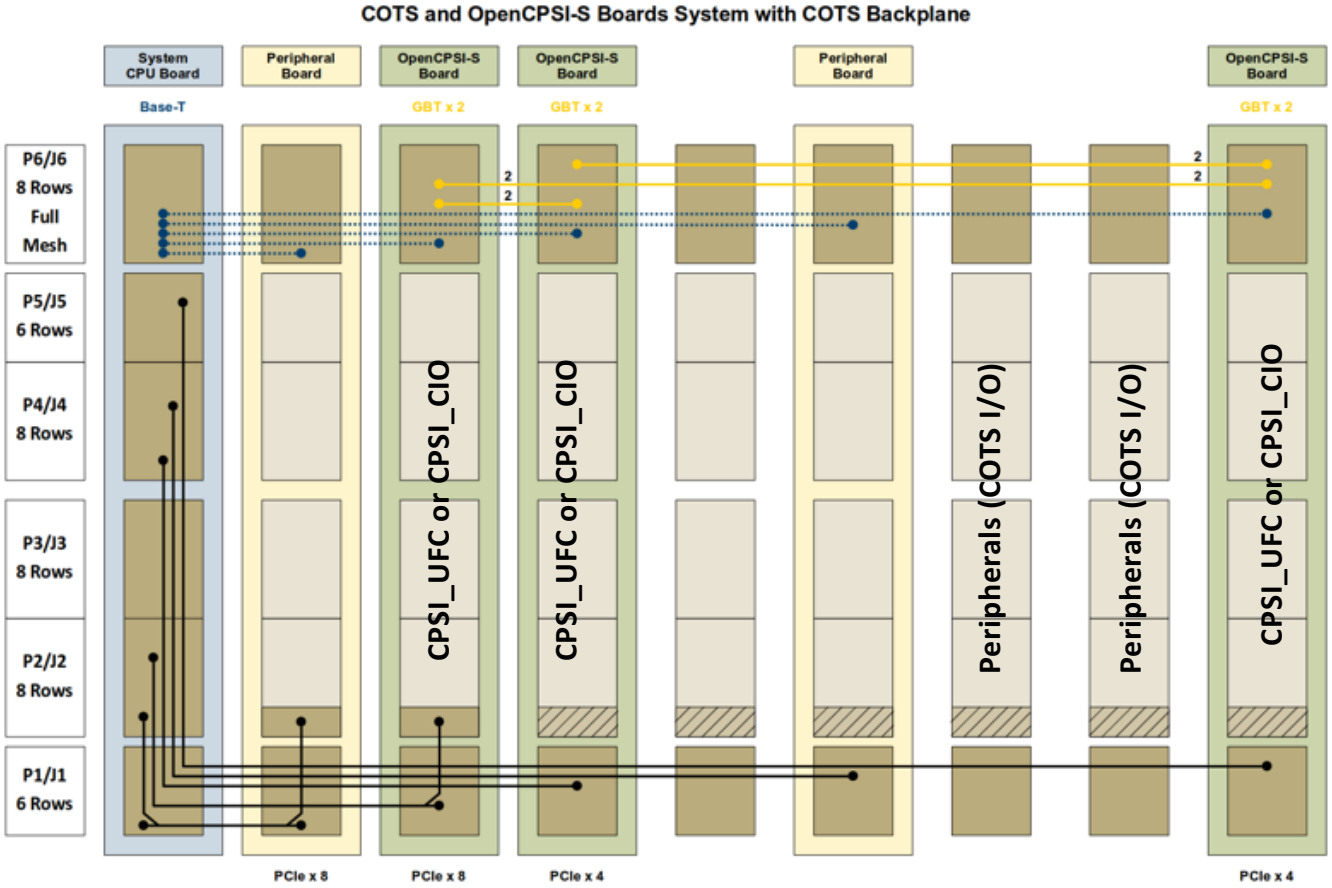
Topologies on Backplane: CPU-centric System

System CPU



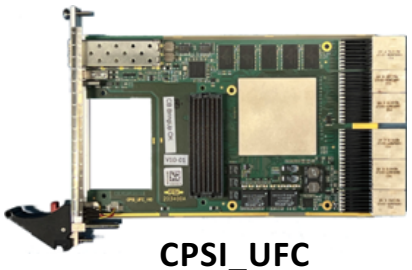
CPSI_UFC

CPSI_CIO

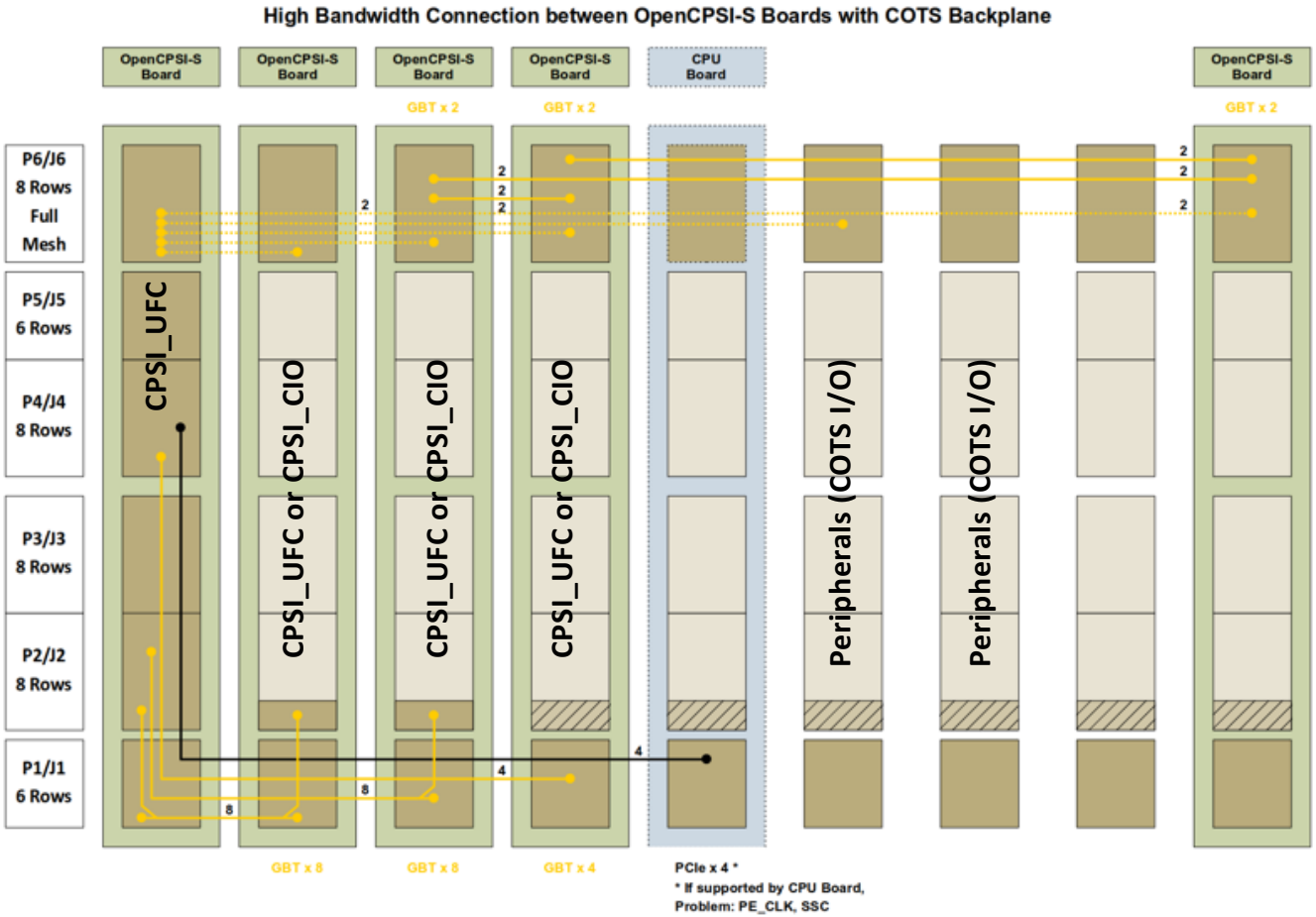


Topologies on Backplane: FPGA-centric System

System CPU



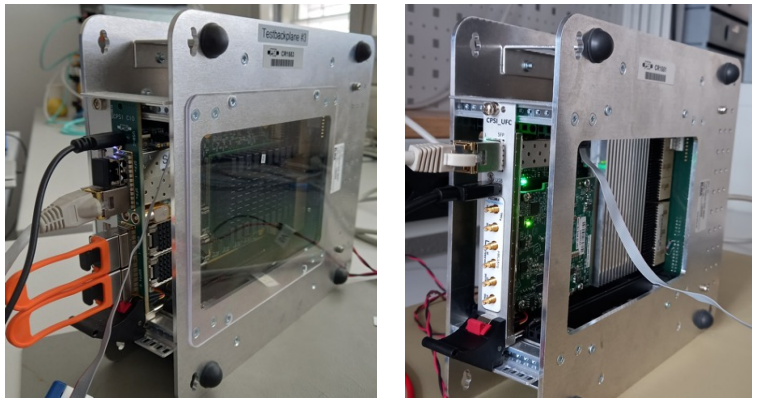
CPSI_UFC



Firmware & Embedded Software aspect

Test Framework and BSP (UFC, CIO)

- HW Prototype validations
  - CPCI_UFC, CPSI_CIO and Crate



Hardware test frame for CPSI_UFC/CIO

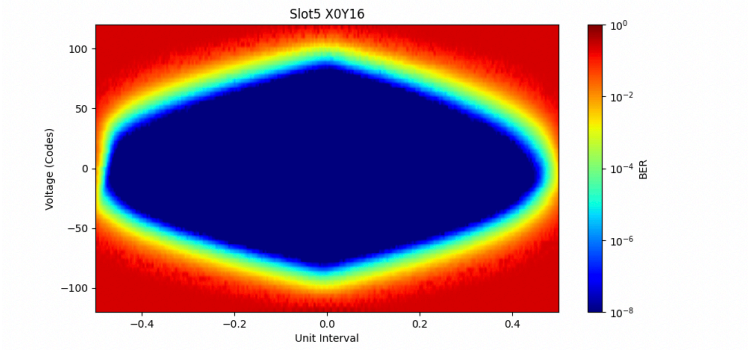
- **Test Framework**
  - Available in Git: https://git.psi.ch/GFA/Libraries/Sw/python/report_creator
  - Applied for testing the UFC, CIO and RTM_FIO boards

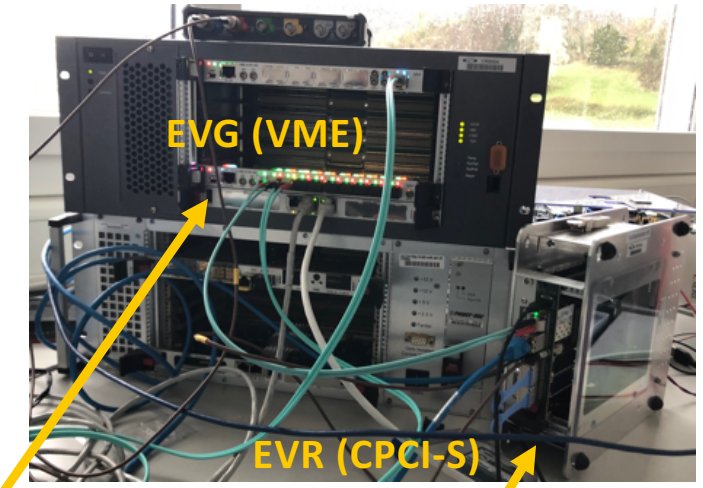
- **Board Support Package (BSP) repository**
  - Available in Git: https://git.psi.ch/GFA/Libraries/BoardSupport/zynqmp_common/linux_bsp
  - Supports: Vivado reference project, Vitis, DeviceTree generation, U-boot compilation, BOOT.BIN generation

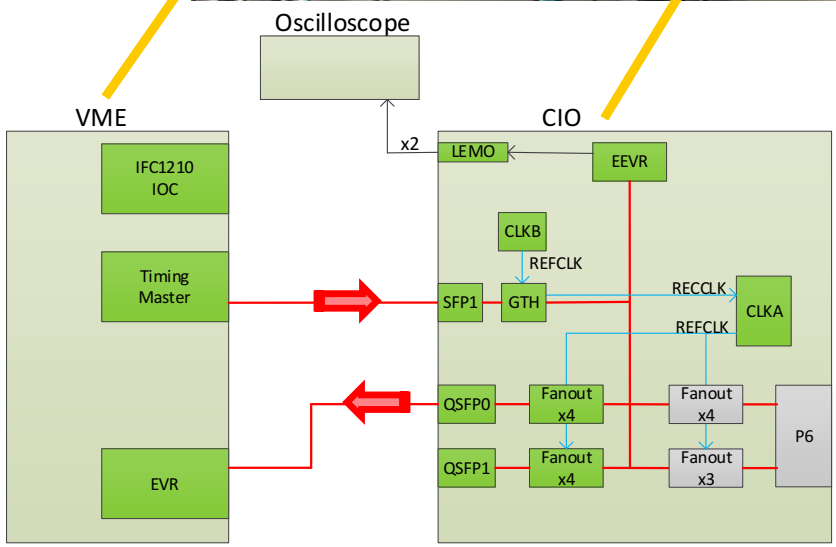
Firmware & Embedded Software aspect

Timing functionality, backplane performance

- CPCI-S Backplane: high speed serial link signal integrity test
- Timing EVR and Fanout tests: 1 uplink and 15 downlink







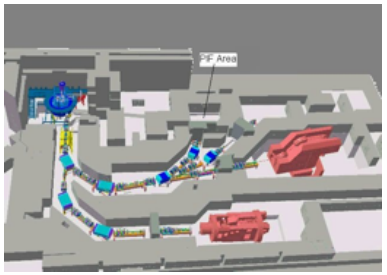
Outlook, how it will go on?

Expert groups (systems)

Feedback systems FOFB, MBFB	LLRF, RF systems	e-/p+ Diagnostics (BCM, ICT, BLM, FP)	Timing, Laser, Interlock, etc.	Controls & DAQ (machine/beamlines)

Facilities

- under upgrade commissioning 2025
  - SLS(2)
  - SwissFEL
  - Proscan
  - HIPA
- upgrade 2025+



Outlook, how it will go on?

- We still have several other important projects to work on in parallel (major ones):
  - SLS2.0 BPM System (large scale and complex)
  - HIPA Electronics upgrade (large scale and complex, various systems)
  - SwissFEL: Digital Laser Synchronization (DLL) system

- We cannot afford to start complex new developments in the next 2-3 years

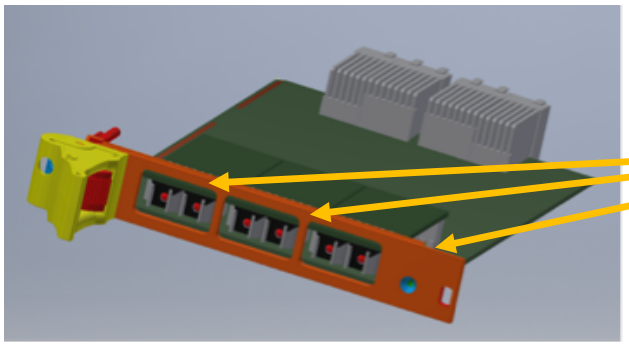
- ***Efforts will move to make developed CPCI-S generic tools fit to applications***
  - Generic tools are made to solve various problems -> might not be **exact fit** to every problem!
  - Understanding this fact & accepting compromises! (manpower <-> work relation, costs)

Outlook, how it will go on?

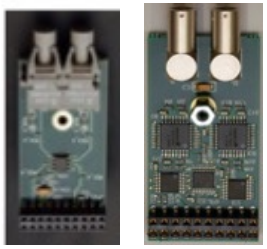
- Procurement and test infrastructure
  - Managing electronics productions, automated test/validation upon deliveries
- Enhancing CPCI-S toolset
  - adding missing functionalities/tools/interfaces
- facilitate system integration
  - defining mechanisms/procedures for configurations (in collaborations with controls)
  - improving documentation

Outlook, making tools fit for apps

- Proper I/O interfacing
  - can be complex or simple RTM's or even Front boards
  - Analog Signal Conditioning board
  - New FMC modules depending on requirements



RTM for CPCI_CIO board



Modular I/O of various signal types can be fit

2x DAC's
2x SFP+
2x Clocks

RTM for CPCI_UFC board

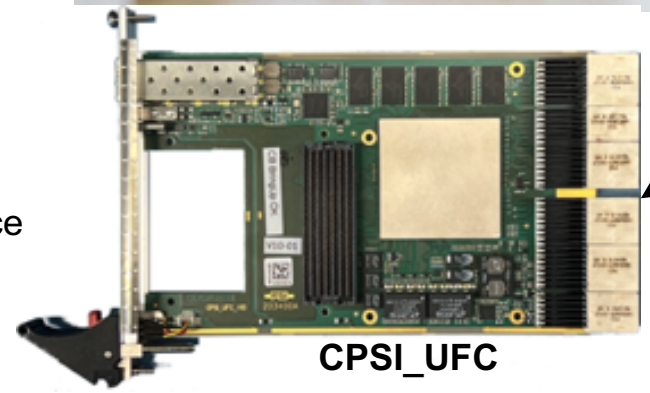
Outlook, I/O interface interoperability

- Example: Rear Transition Module (RTM) with Fixed I/O
  - TTL 4 inputs/4 outputs; clock 1 input/1 output, 1 SFP+ connector

Exanple:Timing master
(event generator)

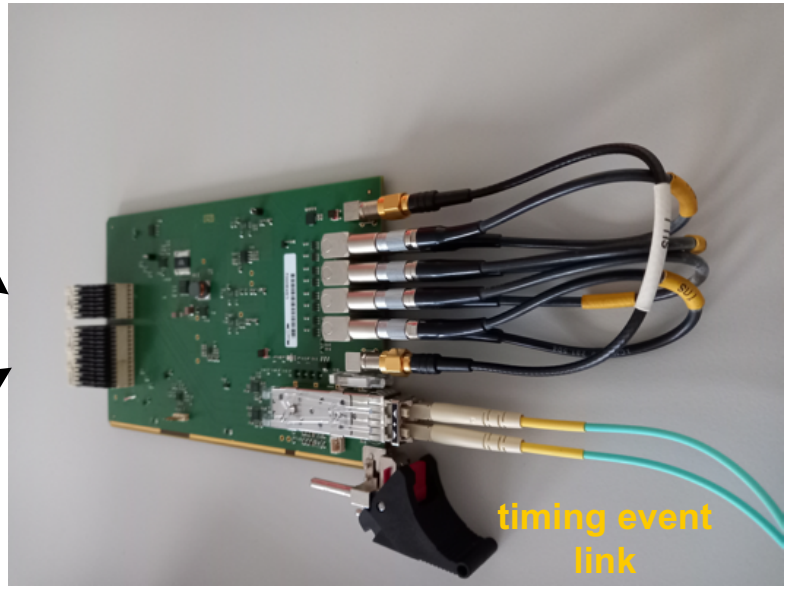
Fast DAQ/Control with
timing & interlock interface

CPSI_CIO



CPSI_UFC

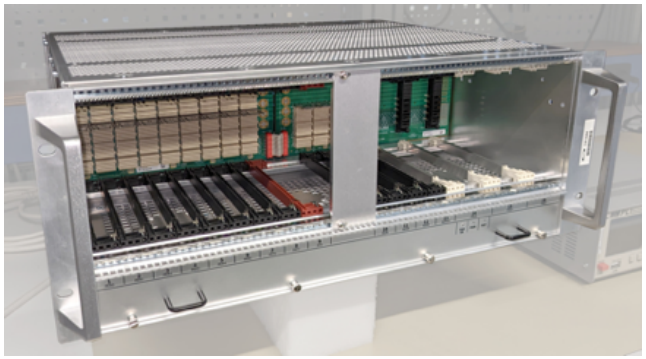
CPSI_RTM_FIO



Outlook, make the toolbox more flexible

- **CPCI-S crate**: adding an economy option with limited features to our portfolio

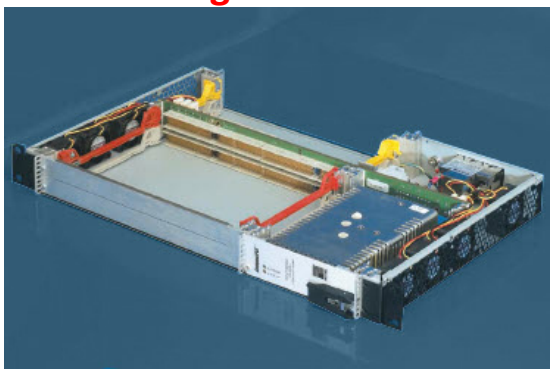
In portfolio



Scalability, extendibility, reliability

- Redundant PSU (3x), 1x SysMon
- 9x CPCI-S slots, 3x utility slots
- 3U (height)
- 160 mm RTM

Being considered

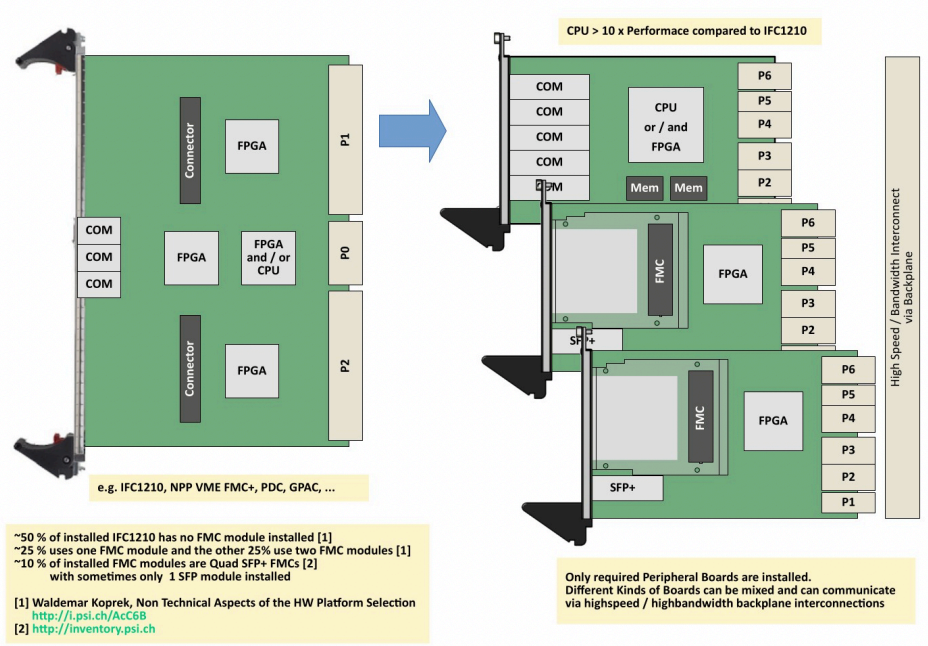


Cost optimized, limited features, compact

- 2x CPCI-S slots
- 1U (height)
- 160 mm RTM
- Requires very small space

Mind changing the technology!

- Change from our long lived **VME** to **CPCI-S**
- Form-factor: 6U to 3U
- Interconnect: parallel to **serial** point-to-point



- ***we need to practice & get used to problem solving with the CPCI-S platform***

Networking

- **CPCI-S mini Workshop (2022)**
  - 4 institutes: ESRF, CERN, STFC-UK and PSI, slides: https://i.psi.ch/gKJRG
  - Goal: resuse of hardware (or designs), Know-How exchange
  - Potential of collaboration with **ESRF** and **STFC-UK**

- **LLRF & TWEPP Workshops (2022)**
  - CPCI-S Based Generic and Modular Processing Platform at PSI https://indico.psi.ch/event/12911/contributions/38356/
  - RF Performance Charachterization of SLS2.0 LLRF Prototype https://indico.psi.ch/event/12911/contributions/38354/
  - Development of a CPCI-S Hardware Toolbox for SLS-2.0 https://indico.cern.ch/event/1127562/contributions/4904878

- Planned in **2023**
  - Follow up workshop with ESRF and STFC-UK
  - TWEPP, ICALEPCS

My thanks go to

- Colleagues in Electronics
- AEK Controls
- NUM Electronics
- GERTS